EMR

710-02

GENERAL
INFORMATION

PCM DECOMMUTATOR

FOX RIVER BOND

25% COTTON

GENERAL INFORMATION

GENERAL
INFORMATION

INSTRUCTION MANUAL

EMR MODEL 710-02
PCM DECOMMUTATOR
(REV. B)

38073

SANGAMO WESTON
Schlumberger

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TABLE OF CONTENTS

SECTION	TITLE	PAGE
1	GENERAL DESCRIPTION	1-1
	1.1 Introduction	1-1
	1.2 Functional Description	1-1
	1.3 Physical Description	1-4
2	SPECIFICATIONS	2-1
	2.1 General	2-1
	2.2 Electrical Specifications	2-1
	2.2.1 Frame Synchronizer	2-1
	2.2.2 Subframe Synchronizer	2-2
	2.2.3 Word Select and Display	2-2
	2.2.4 Simulator	2-2
	2.2.5 Programming	2-3
	2.2.6 Power Requirements	2-3
	2.3 Mechanical Specifications	2-4
	2.4 Environmental Specifications	2-4
3	INSTALLATION AND OPERATION	3-1
	3.1 Installation	3-1
	3.2 Operation	3-8
	3.2.1 General	3-8
	3.2.2 Local Mode of Operation	3-44
	3.2.2.1 Local Program Setup Procedure	3-44
	3.2.2.2 Program Verification Procedure	3-45
	3.2.2.3 Word Select and Display Procedure	3-46
	3.2.3 Computer Setup Mode	3-47
	3.2.4 Card Reader Setup Mode	3-47
4	THEORY OF OPERATION	4-1
	4.1 General	4-1
	4.2 Frame Synchronizer	4-1
	4.2.1 Keyboard Entry, Local Setup Stores, and Cursor Control	4-4
	4.2.1.1 Keyboard Entry	4-4
	4.2.1.2 Local Setup Stores	4-4
	4.2.1.3 Cursor Control	4-4

SECTION	TITLE	PAGE
4 (Cont'd.)	4.2.2 Address Decode, Bus Buffering and Static Stores	4-6
	4.2.3 Input Select Polarity Control, Main Shift Register and Patterns Comparator Circuits	4-8
	4.2.3.1 Input Select	4-8
	4.2.3.2 Auto Polarity Control	4-8
	4.2.3.3 Main Shift Register and Patterns Comparator	4-8
	4.2.4 Pattern Polarity Detection and Selection	4-10
	4.2.5 Error Compare and CP Generation	4-12
	4.2.6 Missed CP Logic	4-14
	4.2.7 Mode Control Logic	4-14
	4.2.8 C Line Generation	4-16
	4.2.9 Window Generation	4-17
	4.2.10 Slip Detect Logic	4-18
	4.2.11 FAC Control FF	4-18
	4.2.12 Display Error Selection	4-19
	4.2.13 Error Display Logic	4-20
	4.2.14 Frame Sync Initialize and Reset Logic	4-22
	4.3 Word Select and Display Card	4-23
	4.3.1 Address Decode and Static Stores	4-25
	4.3.2 Serial-to-Parallel Converter and Transposer	4-25
	4.3.3 Alternate Word Length Control	4-28
	4.3.4 EOW, EOF, EOSF Timing Generation	4-29
	4.3.5 Word/Frame and Frame/Subframe Counters	4-31
	4.3.6 Display Strobe Generation	4-33
	4.3.7 Word Select Keyboard Control and Display Word, Frame, Interval Enable and Store	4-35
	4.3.8 Upper/Lower Display Drive Select	4-37
	4.3.9 Parity Control Circuits	4-39
	4.4 Data Entry Card	4-41
	4.4.1 Computer Interface	4-41
	4.4.2 Card Reader Interface	4-44
	4.5 Subframe Synchronizers	4-47
	4.5.1 Address Decoder, Data Buffers, and Static Stores	4-47
	4.5.2 Subframe Window Generation	4-50

TABLE OF CONTENTS (CONT'D.)

SECTION	TITLE		PAGE
4 (Cont'd.)	4.5.3	Segment Sequence Counter	4-50
	4.5.4	Segment Sequence Counter Functional Block Diagram	4-52
	4.5.5	Recycle EOP Generation	4-53
	4.5.6	Recycle Pattern Correlator	4-54
	4.5.7	Recycle S.F. Correlation Generator	4-56
	4.5.8	Subframe Patterns Count/Compare	4-58
	4.5.9	Subframe Mode Logic	4-59
	4.5.10	ID Pattern Correlation	4-61
	4.5.11	ID Mode Logic	4-61
	4.5.12	Frame N Generation	4-64
	4.5.13	SF1/SF2 Display Control Select	4-65
	4.6	PCM Simulator	4-66
	4.6.1	Program Control and Static Stores	4-68
	4.6.2	VCO/Clock Generator	4-68
	4.6.3	Pseudo-Random Generator	4-71
	4.6.4	ID Word Generator	4-72
	4.6.5	Word and Frame Location	4-74
	4.6.6	Word Enable Strobe Generation	4-76
	4.6.7	Bits/Word Control and EOW Generation	4-77
	4.6.8	EOF and EOSF Timing Circuits	4-78
	4.6.9	Data Stores and Parallel-to-Serial Conversion	4-78
	4.6.10	Output Polarity Control	4-80
	4.6.11	Data Merging, Code Conversion and Output Amplifier	4-80
	4.7	Variable Word Length Card	4-82
	4.7.1	General	4-82
	4.7.2	Block Diagram Description	4-82
5	MAINTENANCE		5-1
	5.1	General	5-1
	5.2	Trouble Shooting	5-1
	5.2.1	Special Tools and Test Equipment	5-1
	5.2.2	Visual Inspection	5-2
	5.2.3	Power Circuits Checkout Procedures	5-2
	5.2.4	Operational Checkout Procedures	5-3
	5.2.5	Variable Word Length Memory Checkout Procedure	5-9

TABLE OF CONTENTS

SECTION	TITLE	PAGE
6	SCHEMATIC/LOGIC DIAGRAMS	
	6.1 General	6-1
	6.2 Schematic/Logic Diagrams	6-1
7	WIRING DIAGRAMS/CONNECTOR LISTS	
	7.1 General	7-1
	7.2 Wiring Diagrams/Connector Lists	7-1
APPENDIX A	LIST OF MNEMONICS	
APPENDIX B	SAMPLE WORKSHEETS	

LIST OF ILLUSTRATIONS

FIGURE NO.	TITLE	PAGE
1-1	Model 710-02 PCM Decommutator, Block Diagram	1-2
1-2	Model 710-02 PCM Decommutator Variable Chart	1-7
3-1	Model 710-02 Rear Panel Connectors	3-2
3-2	Model 710 Front Panel Controls, Indicators and Test Points	3-9
3-3	Front Panel Program Mode Display	3-10
3-4	Frame Synchronizer Programming Worksheet	3-17
3-5	Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively Programming Worksheet for URC and FCC Modes	3-26
3-6	Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Program Worksheet for SFID Mode	3-30
3-7	Simulator, Module Address 4, Programming Worksheet	3-33
3-8	Simulator, Module Address 5, Programming Worksheet	3-39
3-9	Variable Word Length Module Address 0, Programming Worksheet	3-42
4-1	Overall Block Diagram	4-2
4-2	Frame Synchronizer Block Diagram	4-3
4-3	Keyboard Entry, Local Setup Stores and Cursor Control	4-5
4-4	Address Decoders, Static Stores, and Bus Buffers	4-7
4-5	Input Select, Polarity Control, Main Shift Register and Pattern Comparator Circuits	4-9
4-6	Pattern Polarity Detection and Selection Circuits	4-11
4-7	Errors Compare and Correlation Pulse Generator	4-13
4-8	Missed CP Logic Circuit	4-14
4-9	Mode Control Logic Circuit	4-15
4-10	C Lines Generator	4-17
4-11	Window Generator	4-17
4-12	Slip Detect Logic Circuit	4-18
4-13	FAC Control Logic Circuit	4-19
4-14	Display Error Selection Logic	4-20
4-15	Error Display Logic Functional Block Diagram	4-21
4-15A	Frame Sync Initialize and Reset Logic	4-22
4-16	Word Select and Display Block Diagram	4-24
4-17	Address Decode and Static Stores Functional Block Diagram	4-25
4-18	Serial-to-Parallel Converter and Transposer Functional Block Diagram	4-27
4-19	Alternate Word Length Control Functional Block Diagram	4-28

LIST OF ILLUSTRATIONS (CONT'D.)

FIGURE NO.	TITLE	PAGE
4-20	EOW, EOF, EOSF Timing Generator Block Diagram	4-30
4-21	Word/Frame and Frame/Subframe Counters Functional Block Diagram	4-32
4-22	Display Strobe Generator Functional Block Diagram	4-34
4-23	Word Select Keyboard Control and Display Word, Frame, Interval Enable and Store Functional Block Diagram	4-36
4-24	Upper/Lower Display Drive Select Functional Block Diagram	4-38
4-24A	Parity Control Circuits	4-40
4-25	Data Entry Card Block Diagram	4-42
4-26	Computer Interface Functional Block Diagram	4-43
4-27	Card Reader Interface Functional Block Diagram	4-45
4-28	Subframe Synchronizer Card Block Diagram	4-48
4-29	Address Decoder, Data Buffer and Static Stores Functional Block Diagram	4-49
4-30	Subframe Window Generation Functional Block Diagram	4-51
4-31	Segment Sequence Counter Functional Block Diagram	4-52
4-32	Bits/Segment Control Functional Block Diagram	4-53
4-33	Recycle EOP Generation Functional Block Diagram	4-54
4-34	Recycle Patterns Correlator Functional Block Diagram	4-55
4-35	Recycle SF Correlation Generator Functional Block Diagram	4-57
4-36	Subframe Patterns Counter/Comparator Functional Block Diagram	4-58
4-37	Subframe Mode Logic Functional Block Diagram	4-60
4-38	ID Patterns Correlation Functional Block Diagram	4-62
4-39	ID Mode Logic Functional Block Diagram	4-63
4-40	Frame N Generation Functional Block Diagram	4-64A
4-41	SF1/SF2 Display Selection Control	4-65
4-42	PCM Simulator Overall Block Diagram	4-67
4-43	Program Control and Static Stores	4-69
4-44	VCO/Clock Generator (Card 1) Functional Block Diagram	4-70
4-45	Pseudo-Random Generator (Card 1)	4-72
4-46	ID Word Generator (Card 1) Functional Block Diagram	4-73
4-47	Word and Frame Location (Card 2) Functional Block Diagram	4-75

LIST OF ILLUSTRATIONS (CONT'D.)

FIGURE NO.	TITLE	PAGE
4-48	Word Enable Strobe Generation (Card 2)	4-76
4-49	Bits/Word Control and EOW Generator (Card 2)	4-77
4-50	EOF and EOSF Timing Generator (Card 2)	4-78
4-51	Data Stores and Parallel-to-Serial Converter (Card 2)	4-79
4-52	Polarity Control Logic (Card 2)	4-80
4-53	Data Merging, Code Conversion and Output Amplifier Circuits (Card 1)	4-81
4-54	Variable Word Length Card Block Diagram	4-83
5-1	Program Sample No. 1	5-4
5-2	Program #1 Prepunched Card Format	5-6
5-3	Simulator Word Selection Timing	5-10
5-4	Simulator ID Word Timing	5-11
5-5	Simulator Pseudo-Random Timing	5-12
5-6	Simulator Data Inversion Control Timing	5-13
5-7	Frame Sync Correlation Timing	5-14
5-8	Frame Sync Best Pattern Srch → Vfy.	5-15
5-9	Frame Sync Auto Polarity Control	5-16
5-10	Frame Sync Bit Slip	5-17
5-11	Frame Sync Error Accumulator and Display	5-18
5-12	Subframe Sync Recycle Correlation	5-19
5-13	Subframe Sync ID (LSB First) Correlation	5-20
5-14	Subframe Sync ID (MSB First) Correlation	5-21
5-15	Subframe Sync Recycle Mode Timing	5-22
5-16	Subframe Sync ID Mode Timing	5-23
5-17	Word Select and Display Output Timing (Data Only Output)	5-24
5-18	Word Select and Display Output Timing (Frame Sync Pattern Output)	5-25
5-19	Word Select and Display Output Timing (Status Word Output)	5-26
5-20	Word Selection and Display Timing	5-27
5-21	Variable Word Length and Parity Timing	5-28
5-22	Output Timing Diagram	5-29
NOTE:	Section 6 Illustrations are listed in Paragraphs 6.2, 6.3 and 6.4	

LIST OF TABLES

TABLE NO.	TITLE	PAGE
1-1	Model 710 PCM Decommutator List of Major Subassemblies	1-5
3-1	Model 710 Rear Panel Connector List	3-3
3-2	Model 710 Front Panel Controls and Indicators	3-11
3-3	Frame Synchronizer, Module Address 1 (001), Program Worksheet Description	3-18
3-4	Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet Descriptions for URC and FCC Modes	3-27
3-5	Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet for SFID Mode	3-31
3-6	Simulator Card 1, Module Address 4, Program Worksheet Description	3-34
3-7	Simulator Card 2, Module Address 5, Program Worksheet Descriptions	3-40
3-8	VWL Card, Module Address 0, Program Worksheet Descriptions	3-43

SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This instruction manual contains information describing the EMR Model 710-02 PCM Decommutator. Included in this information are physical and functional descriptions, specifications, installation and operating instructions, theory of operation, maintenance procedures and assembly parts lists.

1.2 FUNCTIONAL DESCRIPTION

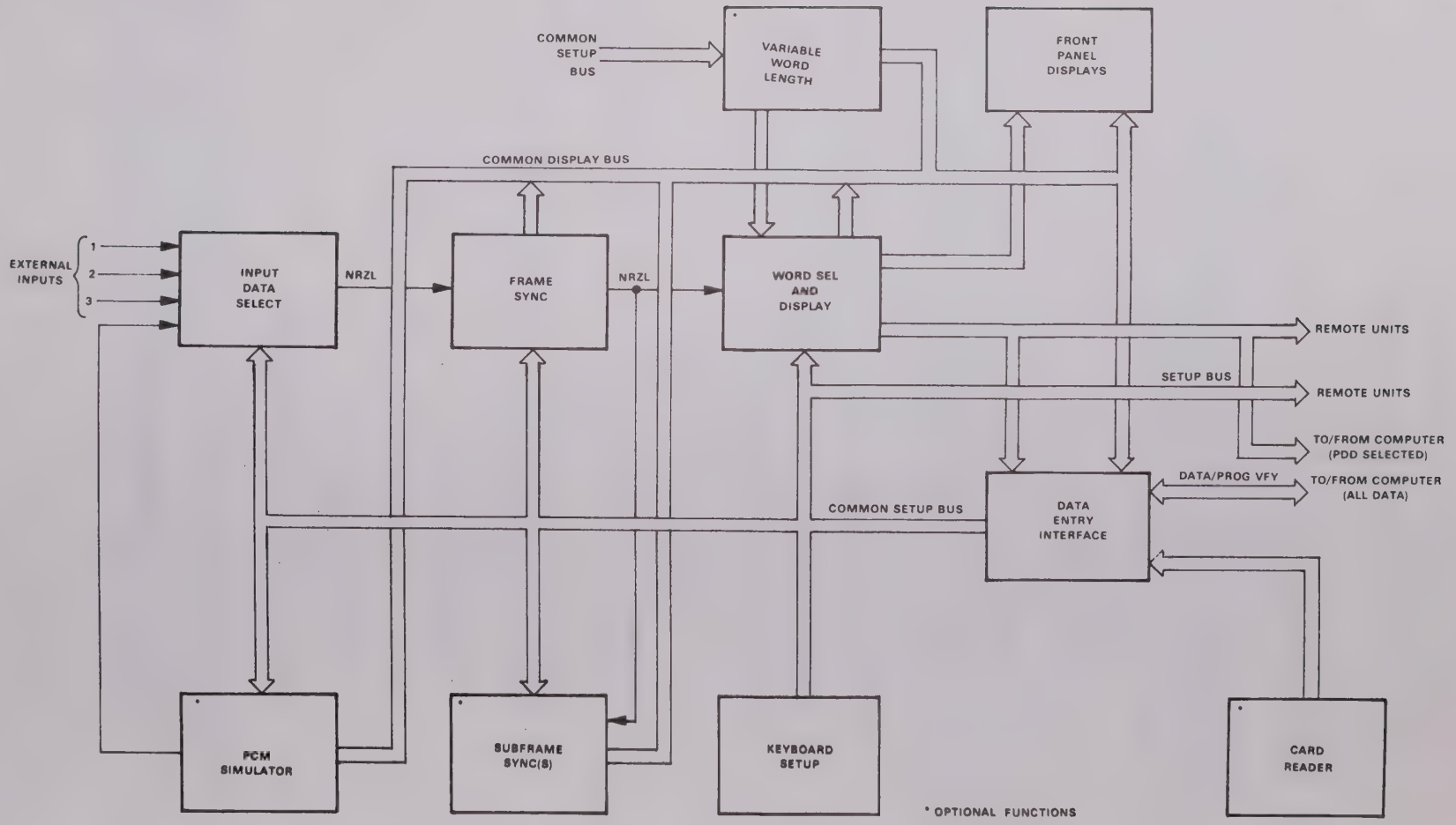
The Model 710-02 PCM Decommutator, when operated in conjunction with a PCM bit synchronizer such as the EMR Model 720, provides a complete PCM telemetry interface operating between an antenna/receiver subsystem and a computer/recorder subsystem. A basic Model 710 provides the following capabilities:

1. Frame synchronization including parity check or generation
2. Manual program setup and control
3. Computer input/output interface
4. Word selection and display in binary or decimal

The basic configuration may be expanded to include any or all of the following capabilities:

1. Subframe synchronization in either frame code complement (FCC), unique recycle code *URC), or subframe ID code
2. PCM data simulation
3. Front panel card reader setup and control
4. Variable word length
5. Programmable Data Distribution

The basic capabilities of the Model 710 are field expandable in a modular fashion. That is, since the interconnections for all options are included in the basic unit even when the minimum configuration is ordered, to expand the operating capabilities it is necessary only to insert the required modules into the basic chassis.


COMMON SETUP BUS
VARIABLE WORD LENGTH
FRONT PANEL DISPLAYS
COMMON DISPLAY BUS
EXTERNAL INPUTS
1
2
3
INPUT DATA SELECT
NRZL
FRAME SYNC
NRZL
WORD SEL AND DISPLAY
REMOTE UNITS
SETUP BUS
REMOTE UNITS
TO/FROM COMPUTER (PDD SELECTED)
DATA/PROG VFY
TO/FROM COMPUTER (ALL DATA)
COMMON SETUP BUS
DATA ENTRY INTERFACE
PCM SIMULATOR
SUBFRAME SYNC(S)
KEYBOARD SETUP
CARD READER
* OPTIONAL FUNCTIONS

Front panel selection controls allow the operating parameters for the 710 to be programmed from one of three sources; an external computer, a card reader or front panel keyboard controls. Refer to Figure 1-1. Inputs from the selected programming source are applied to a common setup bus. This bus distributes the selected input source to allow setup of the frame synchronizer, word select and display, subframe synchronizers and the internal simulator. The bus consists of 16 parallel lines comprising a 3-bit module address, a 5-bit function address, an 8-bit data field and a strobe line. The bus is also routed to the rear panel to provide setup for external units.

Serial NRLZ data and an associated clock input may be applied to the 710 from up to three external sources. When operating under control of the computer or card reader the external input source or the internal PCM simulator (optional) are program selectable. When operating from the front panel keyboard the input signal source is selected by means of front panel controls. The frame synchronizer detects and locks onto the frame sync pattern contained in the selected data stream and generates timing and status related to this pattern. A delayed version of the input data stream is routed to the word select and display and to the subframe synchronizer.

Two independent subframe synchronizers may be provided with the Model 710 PCM Decommutator. Each subframe synchronizer can detect and lock onto individual subframe sync patterns in the input data stream and generate timing and status relating to these patterns. The word select and display card accepts the data and timing from the frame and subframe synchronizers and converts the serial data to a parallel data format. The parallel data is routed to the rear panel for distribution to external monitoring/recording devices. The parallel data is also applied to the computer by way of the data entry interface. The word select and display card also provides the control by which any word in the input format may be selected for display in binary or decimal form on front panel indicators. Subcommutated or supercommutated and alternate word lengths are accommodated.

Circuits for checking or generating parity are located on the word select and display card. The 710 can output data words up to 16 bits plus parity, with parity first or last, odd or even. If the data word is 16 bits, then the parity bit must be stripped from the output. For any other data word length, the parity bit may or may not be stripped (programmable) from the output. In any case, an additional output line will provide a one level for parity error on the word being output, and a zero level for no parity error on the output word. If parity is not being transmitted, a parity bit is generated (programmable odd or even) for each word and the above output line will contain the appropriate level according to the value of the output data word.

The optional variable word length (VLW) feature allows the 710 to accept data formats varying in word lengths from three to 16 bits. With the VWL feature selected frame lengths up to 2048 words can be handled. A programmable data distribution (PDD) capability is provided as part of the VWL function. The PDD capability provides for specific words of the data format to be output, or deleted from the output, at a special rear panel output port.

The common display bus is an 8-bit parallel bus which allows front panel display of any programmable parameter stored in the 710. The stored parameter is placed on the display bus by addressing the desired module and function from the front panel keyboard. The common display bus is also input to the data entry interface to allow the computer to examine the stored parameters.

1.3 PHYSICAL DESCRIPTION

The Model 710 is a self-contained unit, 22 inches (55.9 cm) in overall depth (excluding front panel projections), designed for mounting in a standard 19-inch equipment rack or portable instrument case. The unit is 14-inches (35.6 cm) high and 19-inches (48.3 cm) wide. The major subassemblies of the PCM Decommutator are identified in Table 1-1. Subassembly locations are illustrated on the top level assembly diagram (Dwg. No. 32890) in Section 6.

Figure 1-2 identifies the optional configurations of the PCM Decommutator by model number breakdown.

Table 1-1. Model 710 PCM Decommutator List of Major Subassemblies

REF. DESIG.	NAME	DESCRIPTION
A1	Main Chassis	Contains mating connectors for all printed circuit cards and contains wiring between subassemblies.
A1J1		Not used.
A1J2	Variable Word Length	Contains circuits to enable handling data formats with variable word lengths (VWL) in the range of three to 16 bits in a frame period of up to 2048 words. Also provides circuits for programmable data distribution (PDD) function which either enable specified words to be output at a separate output port or inhibits specific words from being output.
A1J3 and A1J4	(Optional)	Not used.
A1J5 thru A1J6	Frame Synchronizer Card	Contains circuits to provide frame synchronization utilizing an all-digital, five-mode adaptive pattern correlator. Also provides automatic polarity inversion detection and correction.
A1J7 and A1J8	Subframe Synchronizer Card (Optional)	Contains circuits to provide subframe synchronization, programmable to operate in FCC (frame sync code pattern complemented at the subframe rate), URC (unique recycle code), or SFID (subframe ID code).
A1J9 and A1J10	Simulator Card 1 (Optional)	Contains circuits to provide a PCM signal for individual card function or system checkout.
A1J11 and A1J12	Simulator Card 2 (Optional)	The following PCM data codes are simulated under program control: NRZ-L, NRZ-M, NRZ-S, RZ, BiØ-L, BiØ-M, BiØ-S, DM-M, and DM-S.
A1J13 and A1J14	Word Select and Display Card	Contains circuits to provide serial-to-parallel conversion of input data stream and word selecting and display of two data channels. Also provides circuits for parity check or generation.

Table 1-1 (cont'd.). Model 710 PCM Decommutator List of Major Subassemblies

REF. DESIG.	NAME	DESCRIPTION
A1J15		Not used.
A1J16	Data Entry Card	Contains circuits to interface external computer or card reader with the 710.
A1J17		Not used.
A3	Front Panel Assembly	Contains controls, indicators, and test jacks used in operation of the 710. Also contains connector for optional card reader. A description of front panel components is contained in Table 3-2.
A5	Rear Panel Assembly	Contains connectors for termination of input/output wiring between the 710 and peripheral equipment. Also contains primary power input connection, line filter, and fuse. Refer to Table 3-1.
PS1	DC Power Supply (Powertec Model 9E5-50C-17)	Contains components and circuits for generation of +5 VDC used in operation of the 710. Refer to Appendix B.
PS2	DC Power Supply (Optional)	Contains components and circuits for generation of ±15 VDC used by the optional Simulator card.

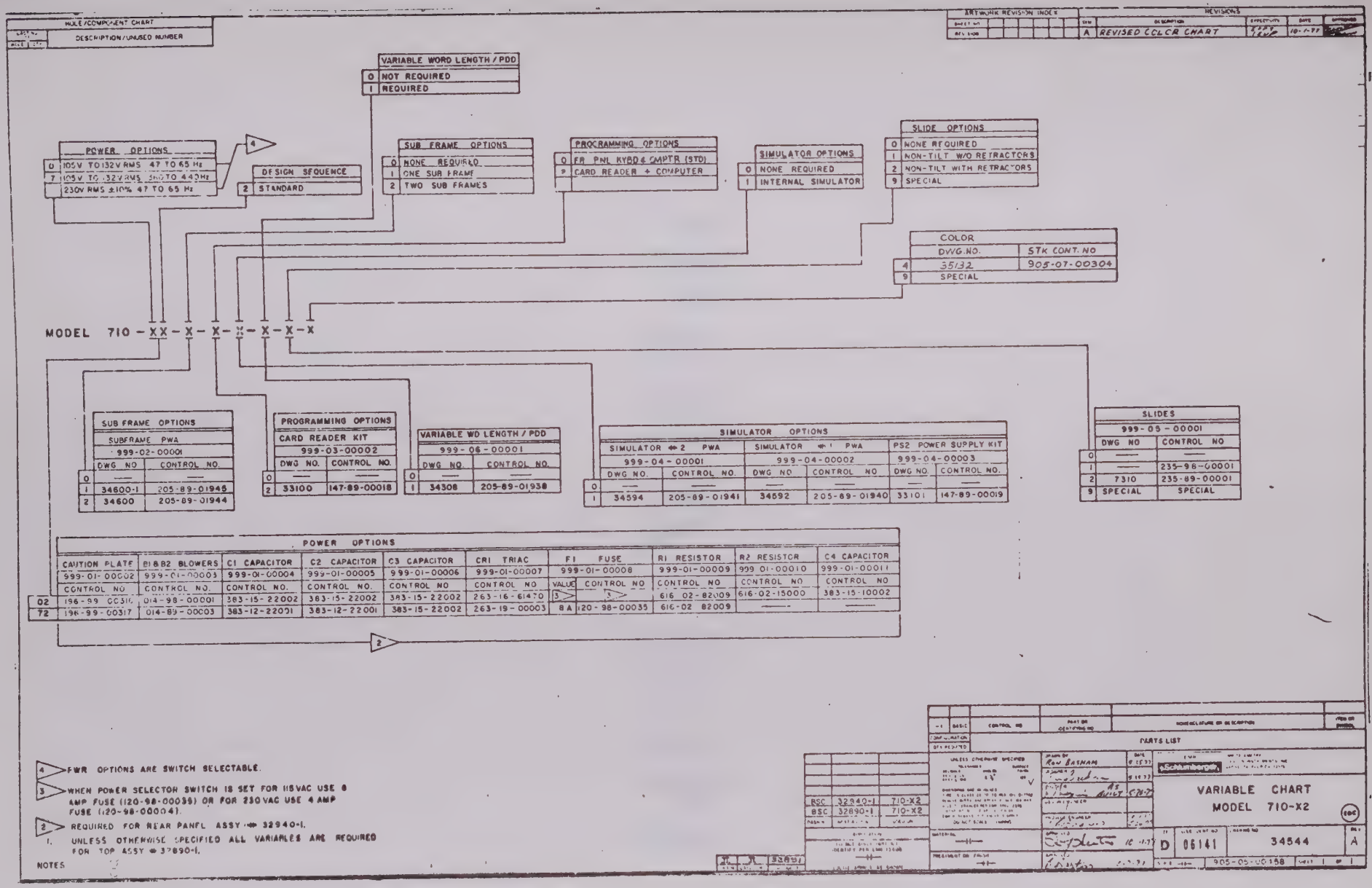


Figure 1-2. Model 710-02 PCM Decommutator Variable Chart

OPERATION

SECTION 2

SPECIFICATIONS

2.1 GENERAL

This section contains the electrical, mechanical and environmental specifications for the Model 710 PCM Decommutator.

2.2 ELECTRICAL SPECIFICATIONS

2.2.1 Frame Synchronizer

a. Inputs: Four, front-panel or program selectable -- three external inputs, and internal simulator. Each input requires an NRZ-L data stream and 0° clock at TTL levels.

b. Bit Rates: Up to 5 Mbps.

c. Bits per Word: Three to 16 plus parity bit (if programmed). Alternate length (once per frame or every Nth word) capability is standard. Optional variable word length capability is provided for three to 16 bits per word and frame lengths up to 2048 words.

d. Words per Frame: Three to 9999.

e. Frames per Subframe: Two to 9999 (two to 512 in ID mode).

f. Pattern: Four to 33 bits, any combination of ones and zeros. The pattern complement can be checked on alternate frames (FAC) or at the subframe rate (FCC).

g. Correlator: Digital.

h. Strategy: Six modes, Non-adaptive (Search, Verify, Lock, and Check) modes: best pattern selected in Search; zero to 15 patterns programmable in Verify and Check; zero to 15 errors allowed in Verify, Lock, and Check. Adaptive mode: allows bypassing Verify if data quality warrants. Auxillary Sync mode: leaves Search mode when first sync pattern meeting Verify mode errors is found.

i. Pattern Aperture: One, three or five-bit wide window.

j. Polarity Ambiguity Resolver: Automatic detection and correction of inverted data.

k. Pattern Bit Error Display: Two-decade display indicating errors over one, 10, or 100 patterns.

l. Output Data: Three 16-bit wide ports.

m. Status Word: 16-bit status word may be output in lieu of frame sync pattern.

n. Throughput Mode: Allows serial-to-parallel conversion without frame synchronization.

2.2.2 Subframe Synchronizer

a. Quantity: Up to two, independent.

b. Modes:
- Frame Code Complement (FCC)
- Unique Recycle Code (URC)
- Identification Code (SFID)

c. Pattern:
- FCC mode: frame code pattern complements at subframe ratio
- URC mode: four to 32 bits, any combination of ones and zeros, contiguous or up to four segments
- SFID mode: one to nine bits, incrementing or decrementing binary count, LSB or MSB first.

d. Correlator: Digital.

e. Strategy: Four modes (Search, Verify, Lock and Check): programmable errors (zero to 15, except in SFID mode) and frames (zero to 15).

2.2.3 Word Select and Display

Any channel (main frame, subframe, or supercommutated) may be displayed on the

2.2.4 Simulator

a. Bits Rates: 1 bps to 5 Mbps.

b. Clock Sources: Internal: frequency synthesizer with deviation input (1% V sensitivity). External: TTL square wave at twice the required bit rate.

c. Codes: NRZ-L, NRZ-M, NRZ-S, BiØ-L, BiØ-M, BiØ-S, RZ, DM-M, DM-S.

d. Bits per Word: Five to 16, common word length; two alternate word lengths programmable for two unique words located anywhere in the frame.

e. Words per Frame: Three to 9999.

f. Frames per Subframe: Two to 9999.

g. Word Types: Unique (six words with programmable data content, up to 16 bits each); Words per Frame (one word which contains the content of the word counter at the time the word is simulated); PN Sequence (one word which contains the output of an 11- or 16-bit pseudo random sequence generator). Note: The common or filler word is programmed to be any one of the above word types.

h. ID Sync Word: Contained within one of the unique words, one to nine bits, LSB or MSB first, count up or down.

i. Data Complementing: Any or all data words may be complemented every N frames.

j. Outputs: NRZ-L data, PCM data (Programmable code, variable amplitude and offset), PCM data (Programmable code, TTL levels), zero degree clock.

2.2.5 Programming

a. Methods: Front-panel keyboard and computer setup are standard. An optional card reader is available.

b. Program Structure: 16-bit party line setup word: three bits, module address (frame sync, simulator, etc.); five bits, function address; eight bits, instruction content.

c. Manual Mode: Keyboard addressing of module and function in decimal; instruction content in binary. Step mode allows sequential loading or reading without readdressing.

d. Card Reader Mode: Interface provided for the Hewlett-Packard P/N 11310A Marked Card Reader, or equivalent. Entire system (less VWL/PDD option) is loaded with five cards. One card loads basic unit.

e. Computer Mode: 16-bit party line interface provided for computer load and verify setup. The entire system (less VWL/PDD option) is loaded with 115 16-bit instructions. Basic unit is loaded with only 32 16-bit instructions.

f. Program Setup Output: Setup bus provided as output for driving additional EMR 700 and 2700 units using the EMR 710 as a host.

2.2.6 Power Requirements

105V to 132V rms, 47 to 65 Hz. 105V to 132V rms. 360 to 440 Hz. 230V rms ±10%. 47 to 65 Hz. 400 to 800 Watts depending upon configuration ordered. (Refer to Figure 1-2.)

2.3 MECHANICAL SPECIFICATIONS

a. Panel Size: 14-in. H x 19-in. W (35.6 cm x 48.3 cm), rack mountable.

b. Overall Depth: 22-in. (55.9 cm), excluding front-panel projections.

c. Weight: Net, 79 pounds (35.8 kg). Shipping, 89 pounds (40.4 kg). (Full configuration.)

d. Panel Finish: Gray semigloss baking enamel with black lettering standard; special paints also are available (per FED-STD-595).

e. Mounting: Slides and hardware for installation in an EIA-type rack can be provided.

2.4 ENVIRONMENTAL SPECIFICATIONS

a. Humidity: Operating, 5% to 95% without condensation.

b. Temperature: Operating, 0° to 50° C. Nonoperating, -55° C to 85° C.

c. Altitude: Operating, sea level to 10,000 feet.

d. Vibration: Nonoperating, per MIL-STD-810A, Method 514, Equipment Class 6, Figure 514-6, Curve A.

e. Shock: Nonoperating, per MIL-STD-810A, Method 516, Procedure III.

SECTION 3

INSTALLATION AND OPERATION

3.1 INSTALLATION

The EMR Model 710 is shipped completely assembled and ready for mounting. The unit should be inspected immediately on its arrival and notice given to EMR-Telemetry of any claim that the product does not conform with the terms of the order.

The 710 is designed for mounting in a standard 19-inch EIA equipment rack or portable instrument case. Physical dimensions of the unit are listed in Section 2. Installation is dependent upon the type of mounting slides provided with the unit. If no slides are purchased, the installation is performed in accordance with the customer requirements. When mounting slides are purchased, hardware is also supplied for a direct installation in the mounting equipment.

The general method for unit installation when slides are provided is as follows:

a. Remove the unit from the shipping carton.

b. Remove the outside brackets of each slide.

c. Mount these brackets to the internal frame of the mounting equipment.

d. Insert the unit into the slides and push the unit into the slides until the unit is locked in position.

Turn-to-lock fasteners are provided on each side of the front panel which are used to secure the unit in the mounting equipment. The unit may be extended from the rack for checkout, adjustment, or troubleshooting by releasing the turn-to-lock fasteners and pulling straight out. Stop latches on the slides hold the unit at the maximum extension.

After installing the unit, the external electrical connections are terminated at rear-panel connectors. A rear-panel view is shown in Figure 3-1. A list of the connectors and the type of connections to be terminated is contained in Table 3-1.

Figure 3-1 Model 710-02 Rear Panel Connectors

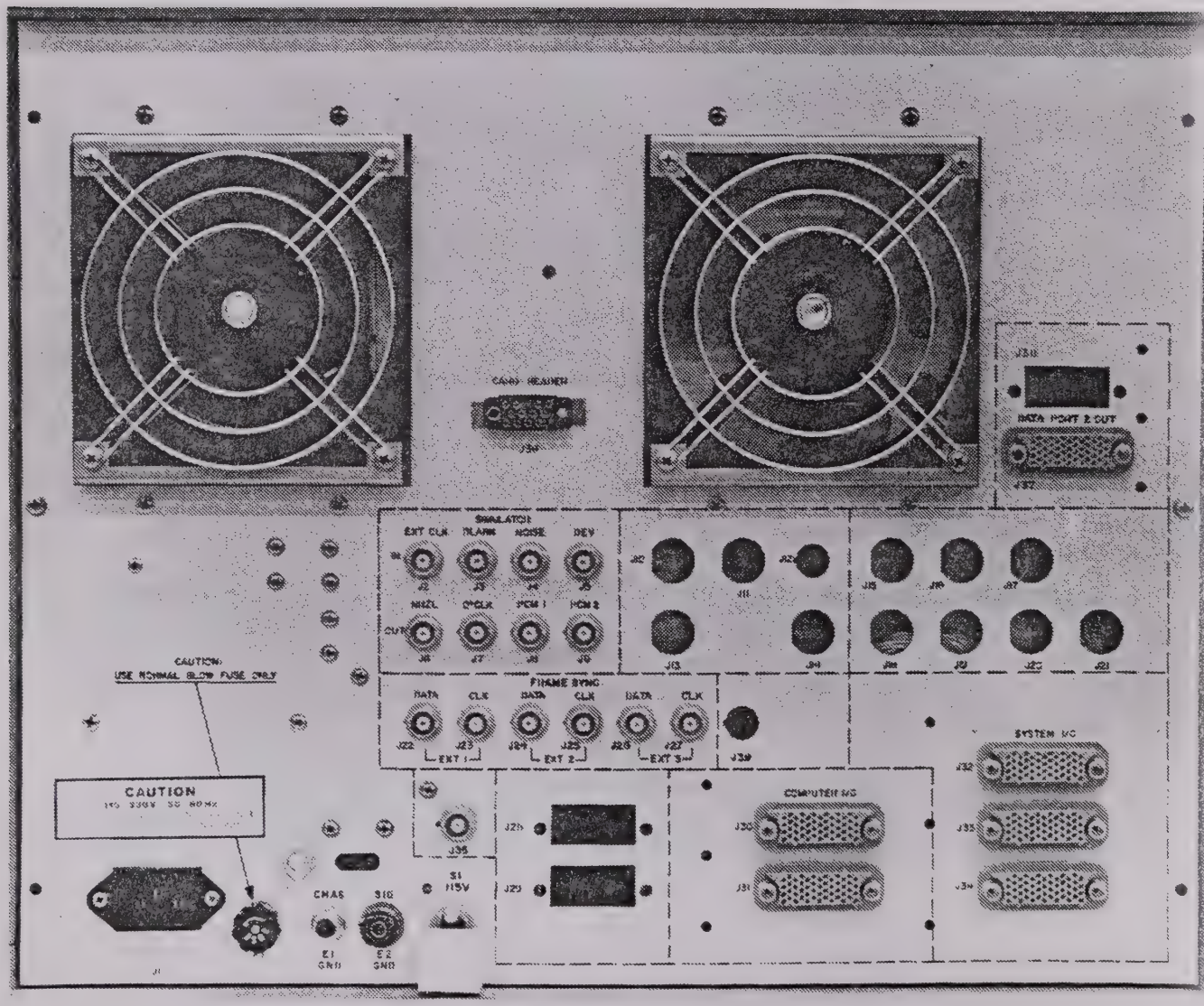


Table 3-1. Model 710 Rear Panel Connector List

Ref. Desig.	Connector Type	Function
A5J1		AC Power Input
	SIMULATOR	
A5J2	BNC	EXT CLK IN -- An external bit rate input to provide simulator timing. Requires square wave at twice the desired bit rate frequency.
A5J3	BNC	BLANK IN -- An input compatible with TTL logic levels used to blank the PCM 1 output at A5J8. A logic "0" blanks the PCM 1 output and a logic "1" enables the PCM 1 output. (A pull up resistor on the card insures that the PCM 1 output is enabled when no connection is made to the Blanking Input.)
A5J4	BNC	NOISE IN -- An external input provided to sum noise or AC baseline offset to the PCM 1 output at A5J8. Noise input impedance is 50Ω and maximum allowable input level is 2.5V RMS.
A5J5	BNC	DEV IN -- An external input which modulates the bit rate VCO with 1% volt sensitivity.
A5J6	BNC	NRZL OUT -- A serial data stream in NRZL code.
A5J7	BNC	0° CLK OUT -- A 50% (±10%) duty cycle bit rate clock output with positive-going transitions at the beginning of the bit period.
A5J8	BNC	PCM 1 OUT -- A bipolar serial data output in any of the programmable PCM codes. Noise and blanking inputs may be introduced through connectors A5J4 and A5J3 as de-described above.
A5J9	BNC	PCM 2 OUT -- TTL level PCM coded output.
A5J10 thru A5J21		Not used.
	FRAME SYNC	
A5J22	BNC	EXT 1 DATA -- Switch or program selectable serial NRZL data input to frame synchronizer.

Table 3-1 (cont'd.). Model 710 Rear Panel Connector List

Ref. Desig.	Connector Type	Function
A5J23	BNC	EXT 1 CLK -- Bit rate timing input associated with external 1 data input.
A5J24	BNC	EXT 2 DATA -- Switch or program selectable serial NRZL data input to frame synchronizer.
A5J25	BNC	EXT 2 CLK -- Bit rate timing input associated with external 2 data input.
A5J26	BNC	EXT 3 DATA -- Switch or program selectable serial NRZL data input to frame synchronizer.
A5J27	BNC	EXT 3 CLK -- Bit rate timing input associated with external 3 data input.
A5J28 and A5J29		Not used.
	COMPUTER I/O	
A3J30	Amphenol-52 pin	Provides interface between the 710 and an external computer for the following programming setup signals: a. 16 Data Output Register (DOR 1 thru DOR 16) signals from an EMR Model 2763 Buffered Data Channel, or equal, which provide computer programming inputs. b. Input Strobe signal which initiates loading of program data into the 710. c. Input Request signal from the 710 which indicates to the computer readiness of the 710 to accept the next program instruction.
A5J31	Amphenol-52 pin	Interfaces the 710 with an external computer for the following 710 output signals: a. 16-bit parallel data output (CMPD 1 thru CMPD 16). b. Data Ready (DATA RDY) signal to computer which indicates 710 data output stable and ready for transfer.

Table 3-1 (cont'd.). Model 710 Rear Panel Connector List

Ref. Desig.	Connector Type	Function
A5J31 (cont'd.)		c. Acknowledge (ACK) signal from the computer verifying receipt of data output. Resets Data Ready condition in the 710. d. External Start (EXT STRT) signal to computer. Used to initiate data transfers at frame rate or subframe rate (program selectable). e. Time Enable (TIMENAB) signal to computer for switching channel ports to merge time data. High during the time from last data word acknowledge through sync pattern occurance when frame sync pattern is not output. f. Parity Data (PAR DATA 1).
	SYSTEM I/O	
A5J32	Amphernol-52 pin	Provides interface between 710 and external units for the following 710 output signals: a. 16-bit common setup bus output (Setup 1 thru Setup 16) used to setup external units from the 710. b. Setup Strobe (STRB) signal. c. Input Request (INRQ IN) signal from external units which the 710 passes on to the computer. d. Six status lines (FLAG 11 thru FLAG 16) for customer use. e. Two card reader status signals, Card Reader Strobe Delayed (CRSTDLY) and Enable Card Reader (ENCRPST), for use in EMR Model 713 Programmable Word Selector when part of the system configuration.
A5J33	Amphenol-52 pin	Provides interface between the 710 and external units for the following frame and subframe synchronizers status and timing outputs.

Table 3-1 (cont'd.). Model 710 Rear Panel Connector List

Ref. Desig.	Connector Type	Function
A5J33 (cont'd.)		a. Rate, Increment, Reset, and Preset Enable signals for subframe synchronizers 1 and 2. b. Mode status signals (Search, Verify, Lock, and Check) for the frame synchronizer and both subframe synchronizers. c. Ready (RDY) status signal to the computer indicating that 710 power is on and 710 is in the computer mode. d. Frame Rate (FRATE) signal. e. Parity Data (PAR DATA 1).
A5J34	Amphenol-52 pin	Provides interface between 710 and external monitor/display units for the following 710 output signals: a. 16-bit parallel data output word programmable for either LSM or MSB alignment. b. Word Increment (WD INC) and Word Reset (WD RST) signals used to drive an external word counter. c. Frame Rate signal. d. Word Rate signal. e. Word Select Strobe signal. A 1/2-bit wide pulse coincident with Word Rate for displayed word.
A5J35		Not used.
CARD READER		
A5J36	AMP 14-pin	Provides signal interface between the 710 and an external card reader for the following signals: a. Eight data lines (CRSET 1 thru CRSET 8) providing card reader programmed inputs to the 710.

Table 3-1. (cont'd.). Model 710 Rear Panel Connector List

Ref. Desig.	Connector Type	Function
A5J36 (cont'd.)		b. Two control inputs, Card Reader Strobe and Card Present, from the card reader. c. +5VDC power input to the card reader.
DATA PORT 2 OUT		
A5J37	Amphenol-52 pin	Provides interface between 710 and an external computer for a programmable output format as follows: a. Port 2 B1 (LSB) through B16 - EMR 710 parallel data output for computer channel input. b. DATA RDY - Data Ready signal to computer channel. Indicates data stable and ready for transfer. Active only for program selected (PDD) channels. c. ACK - Acknowledge signal from computer channel. Resets Data Ready. d. Frame Rate WD INC and WD RS - Word Increment and Reset signals driving the internal word counter. e. EXT STRT and TIMENAB - Same signals as on 131. f. PARITY DATA - Word parity bit. Indicates an error if checking or provides a parity bit if generating. g. ENAB PORT - An input which permits external signal to disable port for multiplexing purposes.
GROUNDS		
A5E1		Chassis ground.
A5E2		Signal ground.

3.2 OPERATION

3.2.1 General

All format control parameters for the Model 710 may be manually programmed from a front panel keyboard or may be loaded into the 710 from a remote computer or from either a local or remote card reader. The internal parameter storage elements are controlled by a common setup bus which can be accessed by any of the above devices. The setup bus is the standard 16-bit programming format as shown below:

MODULE ADDRESS			FUNCTION ADDRESS					DATA FIELD (PARAMETERS)							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Three bits (13, 14 15) are used for the module address (frame synchronizer, subframe synchronizers 1 and 2, and simulator); five bits (8 thru 12) are used as function address (internal storage location); and, an eight-bit data field (0 thru 8) which contain the instructions or parameters to be stored. Any programmable function within the 710 can be overridden or changed manually from the front panel regardless of the initial method of program setup.

The front panel controls and indicators for the Model 710 are illustrated in Figure 3-2. Functional descriptions of these components are provided in Table 3-2. Illustrations and descriptions of the program format for each module of the 710 are provided as follows:

Module	Module Address	Program Worksheet	Program Description
Frame Sync	1	Fig. 3-4	Table 3-3
Subframe Sync 1 or 2 (URC and FCC Modes)	2	Fig. 3-5	Table 3-4
Subframe Sync 1 or 2 (SFID Mode)	3	Fig. 3-6	Table 3-5
Simulator (First part)	4	Fig. 3-7	Table 3-6
Simulator (Second part)	5	Fig. 3-8	Table 3-7
Variable Word Length	0	Fig. 3-9	Table 3-8

When programming the PCM Decommutator it is recommended that the simulator (Module Addresses 4 and 5) be loaded first, then the frame synchronizer (Module Address 1) and finally the subframe synchronizers (Module Addresses 2 and 3).

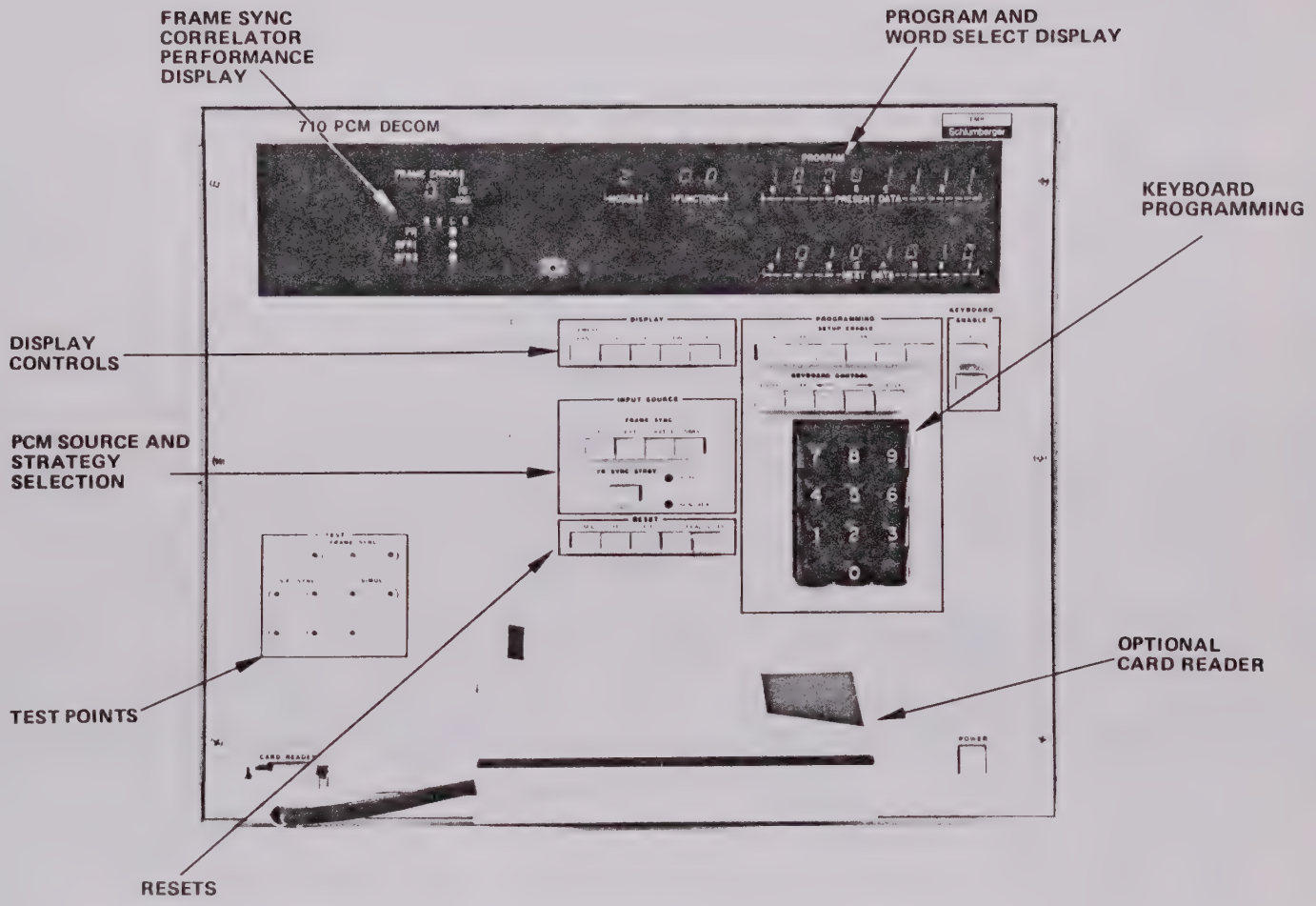


Figure 3-2. Model 710 Front Panel Controls, Indicators and Test Points

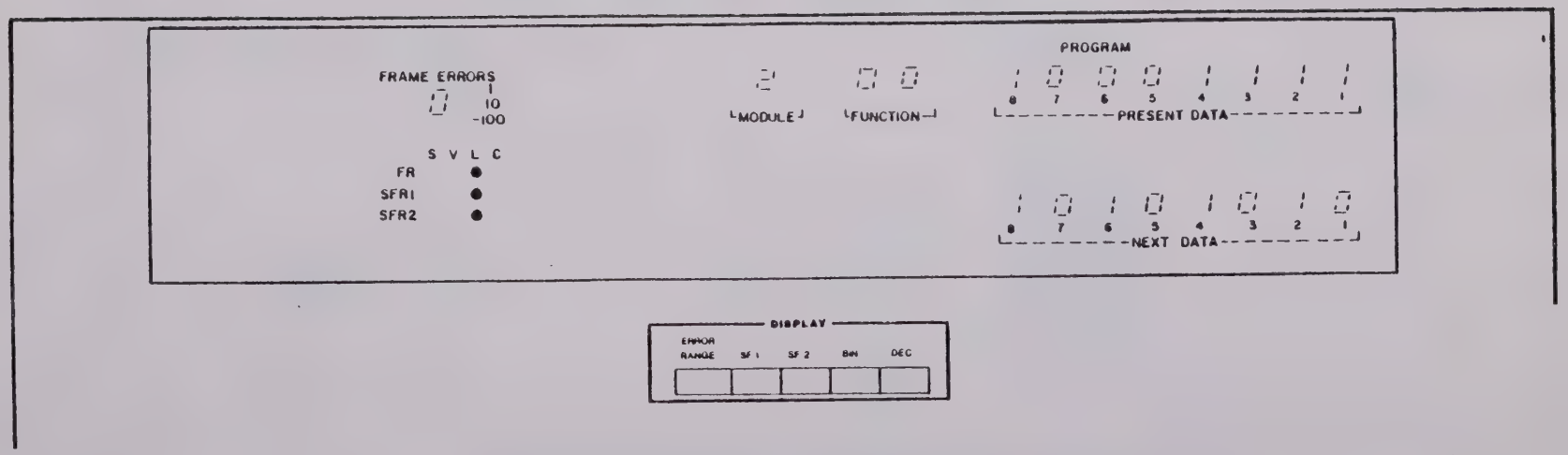


Figure 3-3. Front Panel Program Mode Display.

Table 3-2. Model 710 Front Panel Controls and Indicators (Ref. to Figures 3-2 and 3-3)

Group	Name	Desig.	Function
Frame Sync Correlator Performance Display	FRAME ERRORS display		A two-decade display which indicates the total number of frame sync pattern bit errors accumulated over 1, 10, or 100 frames (as selected by DISPLAY-ERROR RANGE switch) during Lock or Check modes of the frame synchronizer. "Dashes" indicate display overflow.
	FR, SFR1 and SFR2 - S, V, L and C indicators		Lited indicators identify operating mode (Search, Verify, Lock, or Check) of the associated frame or subframe synchronizer.
Program and Word Select Display	NOTE Displays for Word Select mode of operation are as shown on Figure 3-2. For Program mode of operation displays refer to Figure 3-3.		
	PROGRAM		When KEYBOARD ENABLE PROG switch is depressed the following indicators are enabled:
	MODULE indicator		Numeric display indicates module address: 0 = Variable Word Length 1 = Frame Synchronizer 2 = Subframe Synchronizer 1 3 = Subframe Synchronizer 2 4 = Simulator 5 = Simulator
	FUNCTION indicators		Numeric display indicates internal function (device) addressed: 0 through 31
	PRESENT DATA indicators		Binary display (eight bits) indicates the 8 bits of data which are presently stored in the selected address (e.g., Module 2, Function 00).

Table 3-2 (cont'd.). Model 710 Front Panel Controls and Indicators (Ref. Figures 3-2 and 3-3)

Group	Name	Desig.	Function
	NEXT DATA indicators		Binary display (eight bits) indicates the eight bits of data which will be sent to the selected address if the ENTER button is depressed. When this data is sent it will replace the data presently stored in the address.
	WORD SELECT		When KEYBOARD ENABLE WD SEL switch is depressed the following indicators are enabled:
	WORD indicators		Four-digit decimal display of the main frame word number selected for data display.
	FRAME indicators		Four-digit decimal display of the number of the selected frame for the data display. When no frame number is selected (BLANK), main frame data for the specified word number will be displayed. When displaying subcommutated data, the appropriate main frame word number and the correct frame number for the desired subcommutated word must be selected. Additionally, the proper DISPLAY SFR1, subframe synchronizer 1, or SFR2, subframe synchronizer 2 switch must be depressed.
	INTERVAL indicators		Four-digit decimal display of the interval between crossstrapped words. Supercommutated data either on the main frame or subframe will be displayed at the specified rate.
	NOTE When programming WORD, FRAME , or INTERVAL numbers, four digits (including leading ZERO's) are required for each active number. Don't care conditions (FRAME or INTERVAL) are generated by entering BLANKS into the respective displays.		

Table 3-2 (cont'd.). Model 710 Front Panel Controls and Indicators (Ref. Figures 3-2 and 3-3)

Group	Name	Desig.	Function
	DATA indicators		When DISPLAY BIN switch is depressed provides binary display, up to 16 bits, indicating bit values, 1 or 0, of selected word. The data is displayed LSB aligned and unused higher order bits are blanked. When DISPLAY DEC switch is depressed displays five digit decimal value of the selected word (65535 max.).
Keyboard Programming	KEYBOARD ENABLE PROG pushbutton switch	A338	When depressed enables Keyboard Programming displays (Module number, Function number, Present Data, and Next Data).
	KEYBOARD ENABLE WD SEL pushbutton switch		When depressed enables Word Selection displays (Word, Frame, Interval, and Data).
	PROGRAMMING SETUP ENABLE switch	A3S14	
	LOCAL pushbutton		Allows for local setup and examination of all program stores. A cursor is enabled when this switch is depressed. It appears at a point to the left of the data character which can now be changed.
	STEP pushbutton		Operates in conjunction with the KEYBOARD CONTROL ENTER and STEP switches to permit sequential stepping through all addresses.
	CR pushbutton		Enables programming from marked card reader.
	COMP pushbutton		Enables programming from computer.

Table 3-2 (cont'd.). Model 710 Front Panel Controls and Indicators (Ref. Figures 3-2 and 3-3)

Group	Name	Desig.	Function
	KEYBOARD CONTROL switch	A3S10	
	ENTER push-button		When depressed in Local Programming mode causes transfer of data placed in NEXT DATA display into the selected address stores.
	STEP pushbutton		Controls sequential addressing of the program address stores.
	(Cursor left)		Moves cursor to left.
	(Cursor right)		Moves cursor to right.
	Keyboard	A3S16	Keyboard permits manual addressing of module and function in decimal; instruction content in binary. Step mode allows sequential loading (reading) without readdressing. Blank buttons permit entry of blanks for values which are not to be used (for example FRAME and INTERNAL).
Display Controls	DISPLAY/ ERROR RANGE	A3S7	This switch selects one of three ranges for the frame error display. The three ranges are 1, 10, 100 frames.
	SF1		When displaying subcom data, this switch select Subframe Synchronizer 1 as the source of timing for the data display frame counter.
	SF2		When displaying subcom data, this switch selects Subframe Synchronizer 2 as the source of timing for the data display frame counter.
	BIN		To select data for display in binary form.

Table 3-2 (cont'd.). Model 710 Front Panel Controls and Indicators (Ref. Figures 3-2 and 3-3)

Group	Name	Desig.	Function
	DEC		To select data for display in decimal form.
PCM Source and Strategy Selection	FRAME SYNC pushbutton switch EXT 1 EXT 2 EXT 3 SIMUL	A3S11	Signal source input selection for the frame synchronizer. Three external ports are provided plus the internal simulator.
	FR SYNC STRGY switch with LED indicators	A3S13	This switch enables the adaptive strategy feature of the frame synchronizer and allows the unit to proceed directly from search to lock if a completely error-free pattern is detected. With the adaptive strategy not selected, the frame synchronizer verifies the programmed number of acceptable patterns before advancing to lock.
Resets	RESET pushbutton	A3S12	
	SIMUL		Momentary reset switch to reset simulator.
	FR		Momentary reset switch to reset frame synchronizer.
	SF1		Momentary reset switch to reset subframe synchronizer #1.
	SF2		Momentary reset switch to reset subframe synchronizer #2.
	READ STORE		This switch permits readout of recirculating memory. Note: unit may not operate validly with this switch depressed.
Power	POWER pushbutton switch	A3S1	Controls application of primary power to the 710.

Table 3-2 (cont'd.). Model 710 Front Panel Controls and Indicators (Ref. Figures 3-2 and 3-3)

Group	Name	Desig.	Function
Optional Card Reader	CARD READER connector	A3J3	Connection point for local card reader.
Test Points	TEST/ FRAME SYNC/		Test jacks for monitoring the following signals:
	DATA	A3TP1	Frame Sync Selected Data input
	B RATE	A3TP2	Frame Sync Bit Rate Pulses
	WRATE	A3TP3	Frame Sync Word Rate pulse
	FRATE	A3TP4	Frame Sync Frame Rate pulse
	SF SYNC/		
	SF1	A3TP5	Subframe Sync 1 Rate pulse.
	SF2	A3TP6	Subframe Sync 2 Rate pulse.
	SIMUL/		
	EOF	A3TP7	Simulator End of Frame pulse.
	EOSF	A3TP8	Simulator End of Subframe pulse.
	STROBE	A3TP10	Display word strobe pulse.
	GND	A3TP11	Ground.

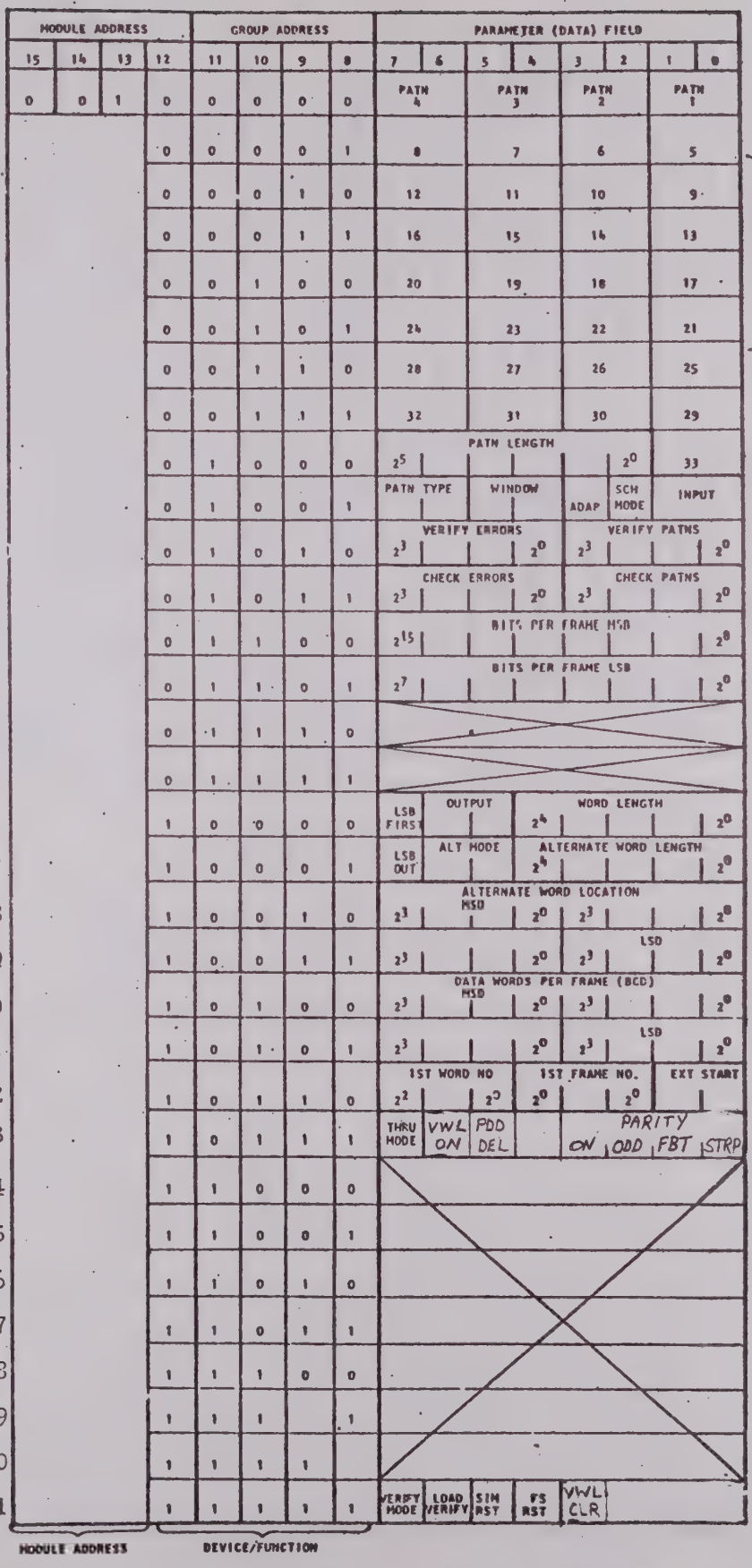


Figure 3-4. Frame Synchronizer Programming Worksheet (Ref. Table 3-3).

Table 3-3. Frame Synchronizer, Module Address 1 (001), Program Worksheet Description

(Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
0 - 7	0 thru 7	Frame Sync Pattern (PATN)	A two-bit code representing any combination of ONES and ZEROS making up the frame sync pattern is programmed in these locations. Two memory bits are used to represent each bit of the pattern in order to give the capability to program "don't care" bits within the pattern. Such a technique is used, for example, when an ID counter is located within the frame sync pattern. Note that the Last Bit Transmitted (LBT) in the pattern is always programmed on function line 0 in bits 0 and 1. If a 33-bit pattern is used the first bit is programmed on function line 8 in bits 0 and 1. The pattern bits are programmed as follows: (10) represents a ZERO pattern; (11) a one pattern; and (00) or (01) represents a "don't care" for the respective pattern bit.
8	0 and 1		
8	2 thru 7	Pattern Length (PATN LENGTH)	A binary number in the range of 4 to 33 which represents the number of bits comprising the frame sync pattern.
9	6 and 7	Pattern Type (PATN TYPE)	The frame synchronization pattern is one of four types specified by a 2-bit code. Normal (00) is a repeating frame code pattern. FAC (01) specifies frame alternating complement. FCC (10) indicates frame code complement at the subframe rate. A "11" specifies automatic polarity control. In this mode, the frame synchronizer will automatically detect and invert the input after identification of two consecutive inverted frame sync patterns.
9	4 and 5	Window (WIN)	A 2-bit code which permits selection of one of three window apertures during the lock and check modes. The three selections are 1 bit (00), 3 bits (01), and 5 bits (10). During the verify mode the window is fixed at one bit.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description
(Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
9	3	Adaptive Strategy (ADAP)	A "1" in this location enables the adaptive strategy feature for the frame synchronizer. This feature allows the unit to proceed directly from Search to Lock if a completely error-free pattern is detected. A "0" programmed in this bit causes the frame synchronizer to verify the specified number of patterns before advancing to Lock.
9	2	Auxiliary Search Mode (ASM)	A logic 0 forces the frame sync to seek a best sync pattern of 9 or less errors before advancing from Search to Verify Mode. A logic 1 allows the frame sync to advance to Verify Mode one a pattern is detected with no more errors than are programmed for the Verify Errors count.
9	0 and 1	Input Source (INPUT)	A two-bit code selecting data input source as follows: 00 = EXT 1, 01 - EXT 2, 10 = EXT 3, 11 = internal simulator.
10	4 thru 7	Verify Mode Errors Count (VFY ERRS)	A binary number (0-15) which specifies the number of bit errors per frame which will be considered acceptable. This definition applies to the pattern detected at the end of the Search mode and during the Verify mode of the frame synchronizer. The unit must identify one acceptable pattern before proceeding from Search to Verify.
10	0 thru 3	Verify Mode Patterns Count	A binary number (0-15) which specifies the number of consecutive acceptable frame sync patterns which must occur before the frame synchronizer will proceed from Verify to Lock. If this criterion is not met the unit will return to Search.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description

(Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
11	4 thru 7	Check Mode Errors Count (CHK ERRS)	A binary number (0-15) which specifies the number of bit errors per frame which will be acceptable during the Lock and Check modes. If the frame synchronizer detects a pattern with more errors than specified it will drop from Lock to Check.
11	0 thru 3	Check Mode Patterns Count (CHK PATNS)	A binary number (0-15) which specifies the number of consecutive unacceptable patterns which will be checked before the unit drops from Check to Search. The receipt of one acceptable pattern returns the unit to Lock.
12 and 13	0 thru 7	Bits per Frame	A binary number in the range 8 to 65, 535 which specifies the total number of bits per frame including the frame sync pattern. The least significant bit of the number is located in bit position 0 of Function Address 13.
16	7	Input Data Format (LSBF)	Defines input data alignment. A "0" represents MSB first; a "1" defines LSB first.
16	5 and 6	Output Format	Specifies the treatment of the frame sync pattern at the frame synchronizer output. A "00" suppresses the frame sync pattern and gives data only output. A "01" gives an output which incudes the frame sync pattern. A "10" substitutes a frame synchronizer status word in place of the output of the frame sync pattern. The status word consists of 16 bits as follows: Bits 0 - 3 -- The number of errors in the frame sync pattern. All ONES indicate 15 or more errors.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description

(Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
16 (cont'd.)	5 and 6	Output Format	Bit 4 --- Frame sync verify mode. Bit 5 --- Frame sync lock mode. Bit 6 --- Frame sync check mode. Bit 7 --- Subframe sync search mode. Bit 8 --- Bit slip. This bit is set if the preceding frame sycn pattern occurred at any windows bit position except the expected position. Bit 9 --- Frame dropout. This bit is set when the frame sync leaves the search mode and remains set for one frame. (This flag indicates that data transfer is resuming after a period of search.) Bits 10 - 15 --- These bits to be input from the rear panel -- user selectable.
16	0 thru 4	Word Length	A four-bit binary number (3-16) specifying the number of bits contained in each word of the input PCM data stream.
17	7	Output Data Format (LSB0)	Defines output alignment. A "0" specifies MSB first; a "1" specifies LSB first.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description (Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
17	5 and 6	Alternate Word Select (ALT MODE)	Controls the frame synchronizer for acceptance of an alternate word length in the input data format as follows: 00 = No alternate length words. 01 = One alternate length word. 10 = Alternate length word is repeated more than once per frame.
17	0 thru 4	Alternate Word Length	A five-bit binary number identifying the number of bits (3-16) contained in the alternate length word.
18	0 thru 7	Alternate Word Location/ Interval	When the alternate length word occurs once per frame (Function Address 17, Bits 5-6 = 01) Function Addresses 18 and 19 identify in BCD the alternate word location (1-9999) within the frame.
19	0 thru 7	Alternate Word Location/First Occurrence	When the alternate length word is repeated more than once within a frame (Function Address 17, Bits 5-6 = 10) Function Address 18 identifies in BCD the word interval (2-99) between occurrences. Function Address 19 identifies in BCD the word location (1-99) for the first occurrence of the alternate length word.
20 and 21	0 thru 7	Data Words	A four digit BCD number (3 to 9999) identifying the number of words, excluding the frame sync pattern contained in each frame of the input format.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description

(Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
22	5 thru 7	First Word Number (1st WD NR)	A binary number (0-7) defining the number of the first word in the frame. Normally the frame synchronizer treats the frame sync pattern as the last word(s) in the frame.
22	2 thru 4	First Frame Number (1st FR NR)	A binary number (0-7) defining the frame number of the frame following the subframe pattern. Normally the frame following the subframe pattern is frame one.
22	0 and 1	External Start (EXT STRT)	A two-bit code specifying the source of the External Start output pulse as follows: 00 = Frame sync frame rate pulse 01 = Subframe sync 1 subframe rate pulse 10 = Subframe sync 2 subframe rate pulse 11 = No External Start Output
23	7	Thruput Mode (THRU)	A one-bit code permitting selection of a special Thruput Mode which allows the unit to serial-to-parallel convert the input data stream and output parallel data without regard to frame synchronization. A "0" in this location permits the unit to operate normally, a "1" selects the special serial-to-parallel conversion. In this mode the parallel data word lengths are determined by the bits per word programming (Function Address 16; Bits 0-4).
	6	VWL on	A logic ONE enables Variable Word Length operation.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description (Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
23 (cont'd.)	5	PDD Delete (PDD DEL)	Used in conjunction with PDD (Module Address 0, Function Address 2, Bit 7) to identify selected or deleted words in the data output (Data Port 2 only) as follows: PDD / PDD Delete / Parallel Data Output 0 / 0 / Word deleted 0 / 1 / Word output 1 / 0 / Word output 1 / 1 / Word deleted
23	0 thru 3	Parity Controls	Controls parity check/generation circuits as follows:
	3	On	1 = enables parity check of incoming data. 0 = enables parity generation for incoming data.
	2	Odd	1 = odd parity. 0 = even parity.
	1	FBT	1 = parity is first bit transmitted. 0 = parity is last bit transmitted.
	0	Strip	1 = incoming parity bit is deleted (stripped) from data output. 0 = parity bit remains in output word.

Table 3-3 (cont'd.). Frame Synchronizer, Module Address 1 (001), Program Worksheet Description

(Ref. Figure 3-4)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
NOTE Bits 4 - 7 of the following instruction are programmed from the computer only.			
31	7	Verify Mode	This instruction is provided for allowing computer read-out of the setup stores via the EMR Model 2763 Buffered Data Channel. The Verify Mode is initiated by a command from the Model 2763 which sets a "1" in this location. When operating in this mode, the Model 710 setup stores will be placed in the output lines normally used to transfer data to the Model 2763. This output is intended for reading setup status into the computer under direct program control. The Verify Mode is terminated when the Model 2763 sends a "0" to this instruction location.
31	6	Load and Verify Mode	This mode is initiated when the Model 2763 sets a "1" in this location. Operation is the same as the Verify Mode (above) but in addition to providing verification, the addressed instruction is first loaded with the setup data received from the Model 2763.
31	5	Simulator Reset	A logic ONE programmed in this position causes a reset of the 710 simulator.
31	4	Frame Sync Reset	A "1" bit programmed in this position causes a reset of the frame synchronizer.
31	3	Variable Word Length Clear	A "1" bit clears the VWL memory (required prior to VWL setup).

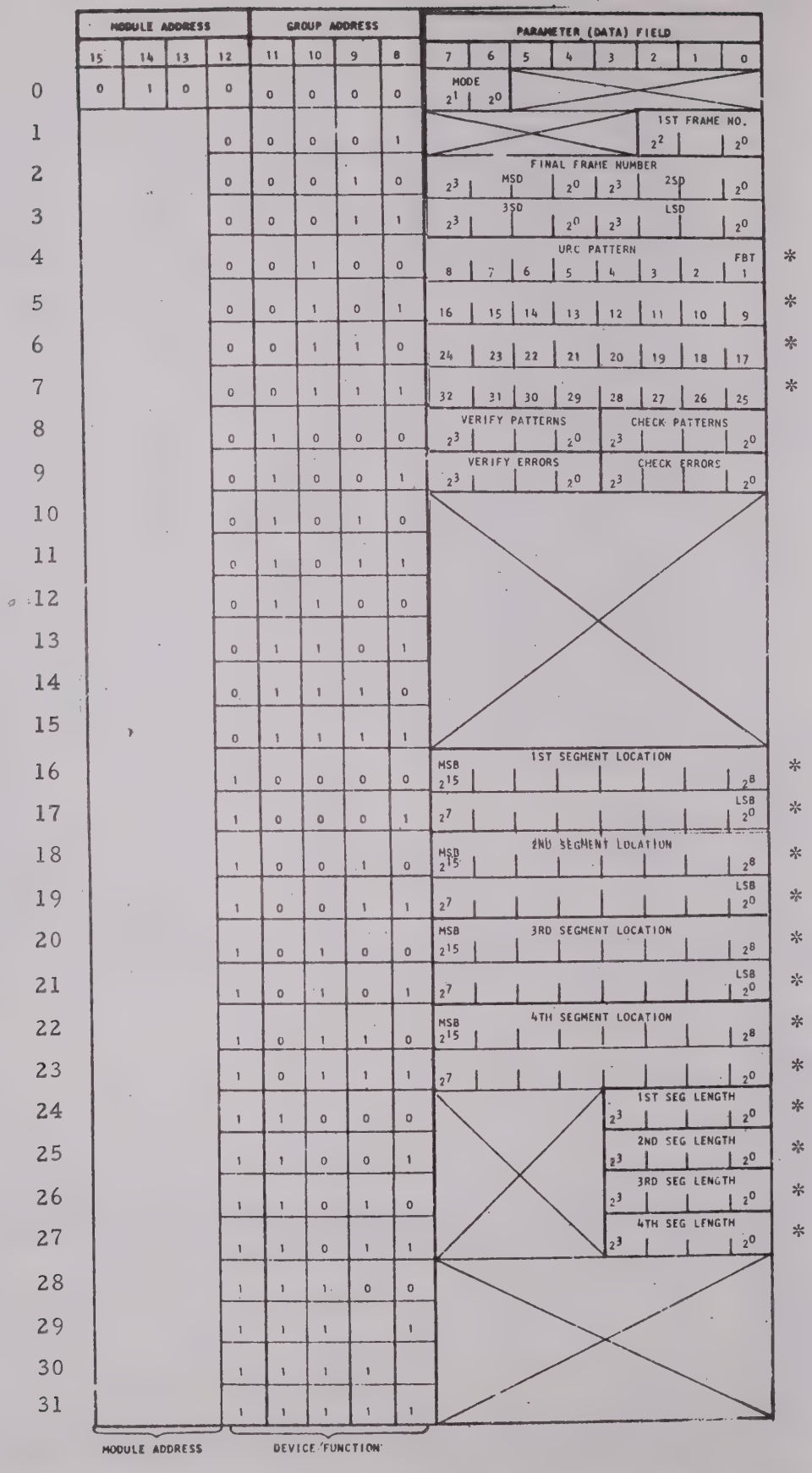


Figure 3-5. Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively Programming Worksheet for URC and FCC Modes (Ref. Table 3-4).

Table 3-4. Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet Descriptions for URC and FCC Modes (Ref. Figure 3-5)

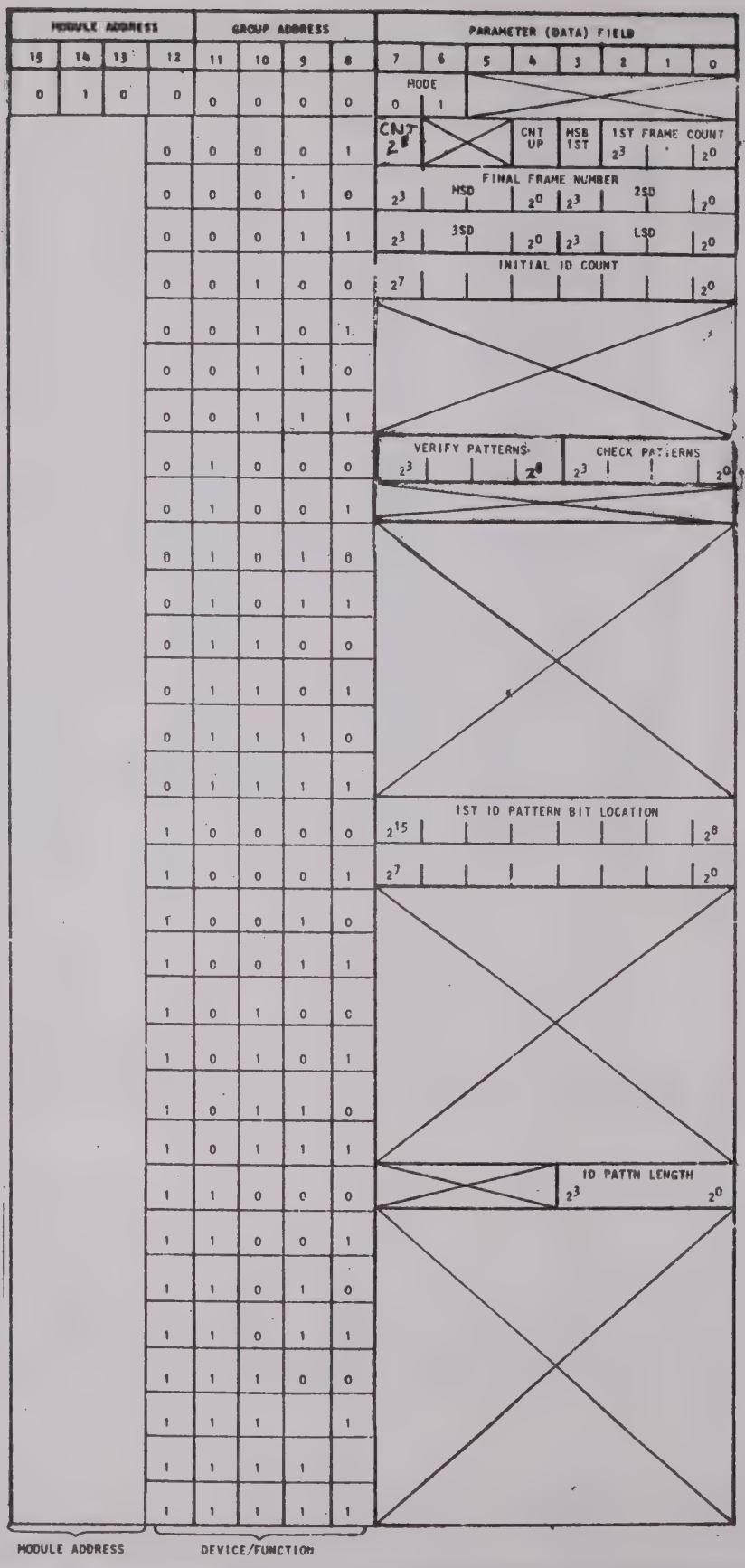
FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
0	6 and 7	Mode Select	A two-bit code specifying the mode of operation for the subframe synchronizer as follows: 00 = Off. 01 = SFID Model (Ref. Figure 3-6 and Table 3-5). 10 = URC Mode. This mode specifies that the subframe pattern is a unique pattern consisting of any combination of 1's and 0's totaling from 4 to 33 contiguous bits or may be split into up to four segments; each segment being from 2 to 15 bits in length. When the pattern is segmented, all segments must occur in one frame period. In either case, the pattern may be located anywhere within the frame. 11 = FCC Mode. This mode specifies that the subframe sync pattern is complement of the frame sync pattern and occurs once per subframe.
1	0 thru 2	First Frame	A binary number [illegible]

Table 3-4 (cont'd.). Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet Descriptions for URC and FCC Modes (Ref. Figure 3-5)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
4 thru 7	0 thru 7	Unique Recycle Code Pattern	A bit-by-bit representation of the Unique Recycle pattern. It may consist of any combination of 1's and 0's from 4 to 32 bits in length. Note that the First Bit Transmitted is located in Function Address 4; Bit 0.
8	4 thru 7	Verify Patterns	A binary representation (0-15) of the number of consecutive acceptable subframe patterns which must be verified before the subframe synchronizer will advance from Verify to Lock. One unacceptable pattern will cause the unit to return to Search. If the frame sync drops to Search it will cause the subframe sync to also drop to Search.
8	0 thru 3	Check Patterns	A binary number (0-15) specifying the number of consecutive unacceptable subframe patterns which will be checked before the unit drops from Check to Search. One acceptable pattern returns the unit to Lock.
9	4 thru 7	Verify Errors	A binary number (0-15) defining the number of bit errors per subframe pattern which will be considered acceptable in the Search and Verify modes. This definition applies only to the URC Mode of subframe synchronization. When operating in the FCC Mode the pattern error tolerance is determined by the error tolerance programmed for the frame sync pattern.
9	0 thru 3	Check Errors	A binary number (0-15) which defines the number of bit errors in the subframe pattern which will be tolerated in the Lock and Check modes. Applies only to the URC Mode of subframe synchronization.

Table 3-4 (cont'd.). Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet Descriptions for URC and FCC Modes (Ref. Figure 3-5)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
			NOTE The following instructions apply only to the URC Mode of operation.
16 and 17	0 thru 7	First Segment Location	A binary number specifying the location (within the main frame) of the first bit in the first segment of the subframe sync pattern. May be located anywhere within the frame. (The first bit following the frame sync pattern is defined as bit 1.)
18 and 19	0 thru 7	Second Segment Location	A binary number specifying the location of the first bit in the second segment of the subframe sync pattern.
20 and 21	0 thru 7	Third Segment Location	A binary number specifying the location of the first bit in the third segment of the subframe sync pattern.
22 and 23	0 thru 7	Fourth Segment Location	A binary number specifying the location of the first bit in the fourth segment of the subframe sync pattern.
24	0 thru 3	First Segment Length	A binary number in the range 2-15 which specifies the length of the first segment of the subframe sync pattern.
25	0 thru 3	Second Segment Length	A binary number in the range 2-15 which specifies the length of the second segment of the subframe sync pattern.
26	0 thru 3	Third Segment Length	A binary number in the range 2-15 which specifies the length of the third segment of the subframe sync pattern.
27	0 thru 3	Fourth Segment Length	A binary number in the range of 2-15 which specifies the length of the fourth segment of the subframe sync pattern.



*Memory Stores

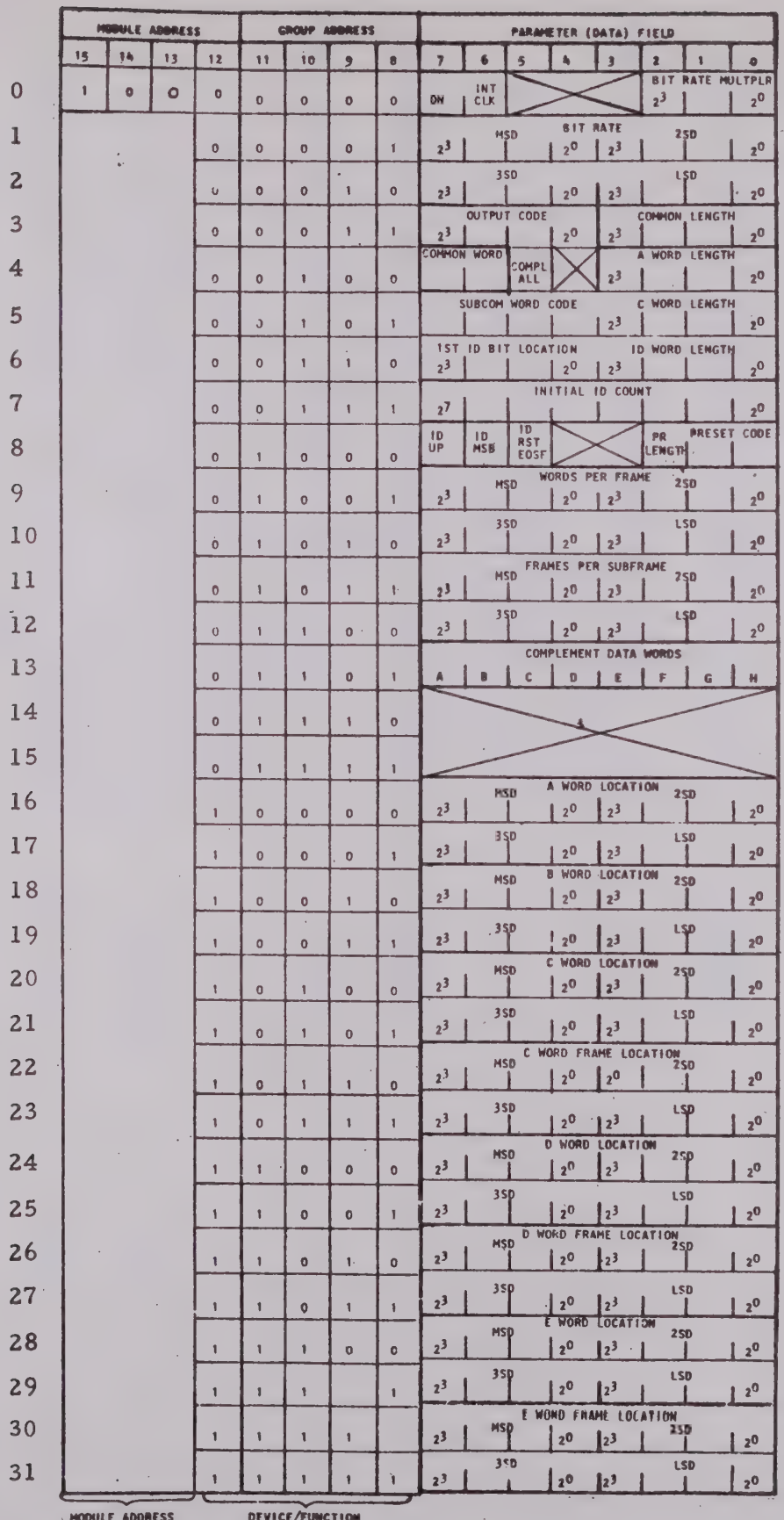
Figure 3-6. Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Program Worksheet for SFID Mode (Ref. Table 3-5).

Table 3-5. Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet for SFID Mode (Ref. Figure 3-6)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
0	6 and 7	Mode Select	A two-bit code specifying the mode of operation for the subframe synchronizer as follows: 00 = Off. 01 = SFID Mode. This mode specifies that the subframe pattern consists of an incrementing or decrementing binary count of from 1 to 9 bits in length. The pattern bits must be contiguous and either MSB or LSB first. The pattern may be located anywhere in the frame. 10 = URC Mode 11 = FCC Mode Ref. Figure 3-5 and Table 3-4
1	7	Initial ID Count	Most significant bit of initial ID count (See Function Address 4).
1	4	Count Direction	Specifies the counting direction of the ID counter. A "0" indicates a decrementing count; a "1" indicates an incrementing count.
1	3	ID Alignment	Identifies the alignment of the incoming ID count. A "0" indicates LSB first; a "1" indicates MSB first.
1	0 thru 2	First Frame Number	A binary number (0-7) defining the frame number of the frame following the last ID count in the sequence.
2 and 3	0 thru 7	Final Frame Number	A BCD number specifying the final frame number. In the SFID mode from 2 to 256.
4	0 thru 7	Initial ID Count	A binary number (2-256) specifying the initial count for the ID counter.

Table 3-5. Subframe Synchronizer 1 or 2, Module Address 2 and 3 Respectively, Programming Worksheet for SFID Mode (Ref. Figure 3-6)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
8	0 thru 3	Check Patterns	A binary number (0-15) specifying the number of consecutive unacceptable subframe patterns which will be checked before the unit drops from Check to Search. One acceptable pattern returns the unit to Lock.
8	4 thru 7	Verify Patterns	A binary representation (0-15) of the number of consecutive acceptable subframe patterns which must be verified before the subframe synchronizer will advance from Verify to Lock. One unacceptable pattern will cause the unit to return to Search. If the frame sync drops to Search it will cause the subframe sync to also drop to Search.
16 and 17	0 thru 7	First ID Bit Location	A binary number specifying the location of the first bit in the ID pattern.
24	0 thru 3	ID Pattern Length	A binary number (1-9) specifying the number of bits in the ID counter.



*Memory Stores

Figure 3-7. Simulator, Module Address 4, Programming Worksheet (Ref. Table 3-6).

Table 3-6. Simulator Card 1, Module Address 4, Program Worksheet Description (Ref. Figure 3-7)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
0	7	Simulator Turn-On (ON)	A "1" enables operation of the simulator. A "0" inhibits operation of the simulator by inhibiting generation of bit rate timing.
	6	Int/Ext. Clock Select	A "1" enables the simulator clock as the source of simulator bit rate timing. A "0" inhibits the internal clock pulses and enables an External Clock, input to the simulator via the rear panel, to provide the source of bit rate timing. The External Clock is input to the simulator at twice the desired bit rate frequency.
0	0 thru 2	Bit Rate Multiplier	A binary representation of the bit rate multiplier exponent. 000 = x 10^0 100 = x 10^4 001 = x 10^1 101 = x 10^5 010 = x 10^2 110 = x 10^6 011 = x 10^3
1 and 2	0 thru 7	Bit Rate	A four-digit BCD number representing the bit rate as follows X.XXX. Valid from 1.000 bps to greater than 5.000 Mbps
3	4 thru 7	Output Code	A four-bit code which enables a specific simulator output code as follows: 0000 = NRZ-L 0100 = Biø-L 0001 = NRZ-M 0101 = Biø-M 0010 = NRZ-S 0110 = Biø-S

Table 3-6 (cont'd.). Simulator Card 1, Module Address 4, Program Worksheet Description (Ref. Figure 3-7)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
3 (cont'd.)			0011 = RZ 0111 = DM-M 1000 = DM-S NOTE When programming the simulator for input to the frame synchronizer the NRZ-L code (0000) must be selected. Other codes may be selected as inputs to remote units.
3	0 thru 3	Common Word Length	A binary number representing the common word length (5-16 bits). All "O's" are decoded as 16 bits.
4	6 and 7	Common Word Select	A two-bit code which identifies the word to be the common word as follows: 00 = F word(programmable) 01 = G word (word count) 10 = H word (pseudo random) 11 = Illegal
4	5	Complement ALL Data	A "1" in this position causes the simulator output data stream to be output in complement form during alternate subframes.
	0 thru 3	A-Word Length	A binary number specifying the length of the "A" word (5-16 bits). The "A" word length may be programmed independent of the length of other words in the format. All "0's" is decoded as a 16-bit length.
5	4 thru 7	Subcom Word Selection	A four-bit code specifying which, if any, of the four possible subcom words are to be used in the subcom mode.

Table 3-6 (cont'd.). Simulator Card 1, Module Address 4, Program Worksheet Description (Ref. Figure 3-7)

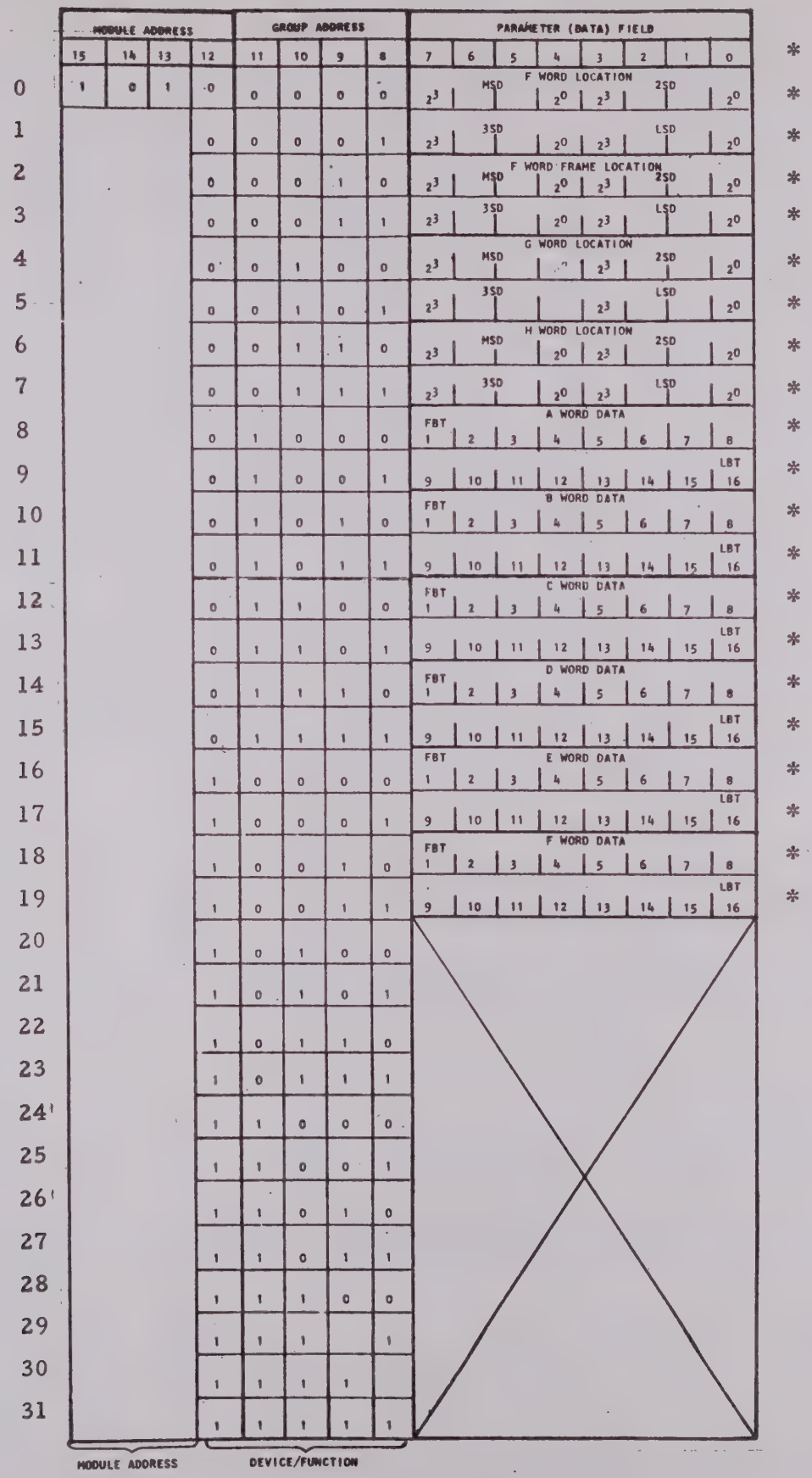
FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
5 (cont'd.)			0000 = no subcom 1xxx = "C" word subcom x1xx = "D" word subcom xx1x = "E" word subcom xxx1 = "F" word subcom For example, if only the "C" and "D" words were to be used for subcom. this instruction would be: 1100.
5	0 thru 3	C-Word Length	A binary number (5-15) specifying the length of the "C" word. The "C" word may be programmed independent of the length of other words in the format. All "0's" are decoded as a 16-bit length.
6	4 thru 7	First Bit Location of ID Count	A binary number specifying the location within the "D" word of the first bit in the ID count. For example, a 4 in this position indicates that three programmed "D Word" bits precede the first bit of the ID pattern.
6	0 thru 3	ID Word Length	A binary number defining the bit length (1 to 9 bits) of the ID Word (count) within the D-Word.
7	0 thru 7	Initial ID Word Count	A binary number, 1 to 511, specifying the initial value to be used as the ID count.
8	7	ID Counting Order	A one bit code defining the counting order of the ID counter. A "0" specifies count down; a "1" specifies count up.
8	6	ID Count Alignment	A one bit code defining the alignment of the ID counter. A "0" specifies LSB is transmitted first; a "1" specifies MSB first.

Table 3-6 (cont'd.). Simulator Card 1, Module Address 4, Program Worksheet Description (Ref. Figure 3-7)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
8	5	ID End of Subframe Reset	A one bit code specifying the reset of the ID counter at the end of subframe. A "0" indicates the counter is not to be reset; a "1" specifies it is to be reset.
8	4	Initial ID Count	Most significant bit of ID count (See Function Address 7).
8	2	PR Length Select	A one bit code for specifying the length of a pseudo-random generator. A "0" selects an 11-bit generator; a "1" selects a 16-bit generator. The selected PR sequence is output on the "H" word which may be used either as a unique word or as a common word.
8	0 and 1	PR Reset Control	A two bit code defining the reset mode of the pseudo-random generator: 00 = No reset. In this mode, the PR generator will output its entire sequence repetitively; asynchronously with the format content. That is, Word 1, Frame 1, will, in general, have a different content each time it occurs. This will simulate a pseudo-random data content. 01 = Reset at end of frame. In this mode, each common word in the frame shall contain bits from the PR sequence, but each word will have the same content from frame-to-frame. 10 = Reset at end of subframe. In this mode, unique common words are generated until the completion of a master frame; after which time they begin to repeat.
9 and 10	0 thru 7	Words Per Frame	A BCD number specifying the total number of words per frame (Up to 9999).
11 and 12	0 thru 7	Frames Per Subframe	A BCD number specifying the number of frames per subframe (Up to 9999).

Table 3-6.(cont'd.). Simulator Card 1, Module Address 4, Program Worksheet Description (Ref. Figure 3-7)

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
13	0 thru 7	Complement Data Words	Each bit position of this Function Address controls complementing of the data value for the associated word (A thru H) at the subframe rate. A "0" indicates the word is not to be complemented; a "1" causes the word to be complemented.
16 and 17	0 thru 7	A-Word Location	A BCD number which specifies the word number location for the "A" word. (Word one normally follows the frame sync.)
18 and 19	0 thru 7	B-Word Location	A BCD number which specifies the word number location for the "B" word.
20 and 21	0 thru 7	C-Word Location	A BCD number which specifies the word number location for the "C" word.
22 and 23	0 thru 7	C-Word Frame Location	A BCD number which specifies the frame number location for the "C" word when used as a subcom word.
24 and 25	0 thru 7	D-Word Location	A BCD number which specifies the word number location for the "D" word.
26 and 27	0 thru 7	D-Word Frame Location	A BCD number which specifies the frame number location for the "D" word when used as a subcom word.
28 and 29	0 thru 7	E-Word Location	A BCD number which specifies the word number location for the "E" word.
30 and 31	0 thru 7	E-Word Frame Location	A BCD number which specifies the frame number location for the "E" word when used as a subcom word.



*Memory Stores

Figure 3-8. Simulator, Module Address 5, Programming Worksheet (Ref. Table 3-7).

Table 3-7. Simulator Card 2, Module Address 5, Program Worksheet Descriptions (Ref. Figure 3-8).

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
0 and 1	0 thru 7	F Word Location	A BCD number, 1 to 9999, identifying the location of the "F" Word within a frame.
2 and 3	0 thru 7	F Word Frame Location	A BCD number, 1 to 9999, identifying the frame within a subframe containing the "F" Word when used as a subcom word.
4 and 5	0 thru 7	G Word Location	A BCD number, 1 to 9999, identifying the location of the "G" Word within a frame.
6 and 7	0 thru 7	H Word Location	A BCD number, 1 to 9999, identifying the location of the "H" Word within a frame.
8 and 9	0 thru 7	A Word Data	Up to 16 bits representing the data to be output for the "A" Word. The first bit transmitted is located in bit position 7 of Function Address 8. Program as many bits as are required by the simulated format.
10 and 11	0 thru 7	B Word Data	Up to 16 bits representing the data to be output for the "B" Word. The first bit transmitted is located in Function Address 10, bit position 7.
12 and 13	0 thru 7	C Word Data	Up to 16 bits representing the data to be output for the "C" Word. The first bit transmitted is located in Function Address 12, bit position 7.
14 and 15	0 thru 7	D Word Data	Up to 16 bits representing the data to be output for the "D" Word. The first bit transmitted is located in Function Address 14, bit position 7.

Table 3-7 (cont'd.). Simulator Card 2, Module Address 5, Program Worksheet Descriptions (Ref. Fig. 3-8).

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
16 and 17	0 thru 7	E Word Data	Up to 16 bits representing the data to be output for the "E" Word. The first bit transmitted is located in Function Address 16, bit position 7.
18 and 19	0 thru 7	F Word Data	Up to 16 bits representing the data to be output for the "F" Word. The first bit transmitted is located in Function Address 18, bit position 7.

	MODULE ADDRESS			FUNCTION ADDRESS					PARAMETER (DATA) FIELD								
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	2^3	2^2	2^1	2^0	2^3			2^0	VWL LOCATION (THOU) (HUND)
1				0	0	0	0	1	2^3	2^2	2^1	2^0	2^3	2^2		2^0	VWL LOCATION (TENS) (UNITS)
2				0	0	0	1	0	PDD	STEP		2^4	2^3	2^2	2^1	2^0	VW LENGTH *

* Memory Store

Notes:

1. Above programming must be repeated for each variable length word in the data format.

2. When using card reader, instructions 0-2 may be repeated up to 10 times on one programming card.

3. VWL Location (Function Addresses 0 and 1) cannot be displayed or computer verified.

4. The STEP instruction (Function Address 2, Bit 6) is not stored and generates a pulse only.

5. When the Variable Word Length option is to be used the 1st WD NR parameter (MA1, Function 22) must be loaded prior to loading the VWL memory.

Figure 3-9. Variable Word Length, Module Address 0, Programming Worksheet (Ref. Table 3-8).

Table 3-8. VWL Card, Module Address 0, Program Worksheet Descriptions (Ref. Fig. 3-9).

FUNCTION ADDRESS	DATA FIELD BITS	PARAMETER	DESCRIPTION
0 and 1	0 thru 7	VWL Location	A BCD number (0 thru 2047) identifying the word number of the VWL position to be loaded.
2	0 thru 4	VW Length	A binary number (3 thru 16) identifying bit length of the variable length word.
2	6	STEP	Causes VWL memory address counter to increment by one count after loading data. This instruction is intended for manual operation only.
2	7	PDD	Used in conjunction with PDD Delete (Module Address 1, Function Address 23, Bit 5) to identify selected or deleted words in the data output (Data Port 2 only) as follows:

PDD	PDD Delete	Parallel Data Output
0	0	Word deleted
0	1	Word output
1	0	Word output
1	1	Word deleted

3.2.2 Local Mode of Operation

The Model 710 front panel controls and indicators, Figure 3-2 and 3-3, provide facilities for manual program setup and verification and for selection and display of any word in the PCM input format. The following paragraphs provide procedures for these operations.

3.2.2.1 Local Program Setup Procedure

To manually program the 710 proceed as follows:

a. Make required input/output connects at the rear panel. (Refer to Table 3-1 for input/output connector identification).

b. Depress front panel POWER switch to apply primary power to the unit.

c. Select the desired input source by depressing the appropriate INPUT SOURCE pushbutton (EXT 1, EXT 2, EXT 3, or SIM).

d. Select the local mode of operation by depressing KEYBOARD ENABLE/PROG pushbutton and by depressing either the PROGRAMMING SETUP ENABLE LOCAL or STEP pushbutton. At this point the front panel PROGRAM displays (MODULE, FUNCTION, PRESENT DATA, and NEXT DATA) are enabled and KEYBOARD CONTROL cursor ← and → pushbuttons can be operated to align the cursor to a desired position.

e. To load an instruction into a specific storage location proceed as follows:

1. Align the cursor with MODULE display.

2. Depress the keyboard switch for the Module Address number (i.e. Subframe Sync 1 = 2; Frame Sync = 1, etc.) The selected Module Address will be displayed and the cursor will step to the most significant digit of the FUNCTION ADDRESS display.

3. Select the Function Address (two-digits) by depressing the keyboard switches corresponding to the Function Address number.

4. At this point the PRESENT DATA display indicates the eight-bit binary content of the storage devices for the Module and Function Addresses selected. New data is sequentially loaded from left to right into the NEXT DATA displays by depressing the appropriate "1" or "0" switch on the keyboard for the cursor enabled data bit locations.

5. Depress the KEYBOARD CONTROL ENTER pushbutton. This causes the new data to be loaded into the selected

Function Address storage device and returns the cursor to a predetermined position. With the SETUP ENABLE switch in the STEP mode the Function Address advances to the next sequential address and the cursor returns to the Data 8 (MSB) position of the NEXT DATA display. The 710 is thus enabled for selecting the parameter for the next address of the program format. This setup procedure is normally used for mass manual loading of the Model 710 program.

When the SETUP ENABLE switch is in the LOCAL mode the cursor returns to the MODULE ADDRESS position when the ENTER pushbutton is depressed. This setup would normally be used for single address programming.

f. In order to load the optional variable word length memory, enter a ONE in the VWL CLR bit (MODULE 1, FUNCTION 31), and then set the address to MODULE 0, FUNCTION 00, and enter the two most significant digits (in BCD) of the word location of the variable length word to be loaded. Next, address FUNCTION 01 and enter the least significant digits of the word location. The third step is to address FUNCTION 02 and enter the actual word length of the variable word location and the PDD bit. Additional variable word locations can be addressed by repeating the above steps (omitting the VWL CLR step) for all variable word locations in the format.

3.2.2.2 Program Verification Procedure

The program parameters stored in the Model 710 may be verified as follows:

NOTE

Programmed parameters stored in static storage devices of the 710 may be monitored at any time without affecting normal operation of the system. However, to monitor the content of certain memory storage devices, the dynamic operation of the 710 must be halted in order that these devices remain stable. This is accomplished by depressing the READ STORES pushbutton. The memory stored parameters are identified on the program worksheets (Figures 3-3 thru 3-7) by an asterisk alongside the applicable Function Addresses.

a. Depress the KEYBOARD ENABLE - PROG pushbutton.

b. Depress the SETUP ENABLE STEP pushbutton.

c. Select the Module and Function Addresses for the program instruction(s) to be verified as described in step E (substeps 1 thru 3) of paragraph 3.2.2.1. The content of the selected address is displayed on the PRESENT DATA displays and can be compared to the required data on the applicable programming worksheet. If a program error is detected it may be corrected as described in paragraph 3.2.2.1 .

d. Depress the KEYBOARD ENABLE STEP pushbutton. This action increments the Function Address thereby displaying the next sequential program instruction on the PRESENT DATA display. The content of static stores associated with each Module and Function Address can thus be monitored and corrected as necessary.

e. Upon completion of verification disengage the RESET READ STORES pushbutton to allow the 710 to resume normal operation.

f. Note that if the variable word length (VWL) option is present, and if the VWL memory is to be verified, each memory address must be loaded into MODULE 0, FUNCTIONS 00 and 01 in order to read the memory content in FUNCTION 02.

3.2.2.3 Word Select and Display Procedure

Any word of the input format may be selected for display on front panel indicators as follows:

a. Depress KEYBOARD ENABLE WD SEL pushbutton. The WORD SELECT display (Figure 3-3) should be lit.

b. Align the cursor with the most significant digit of the WORD number display.

c. Using the front panel keyboard, select the number of the word in the input data format to be displayed. (Do not omit leading ZERO's.) If the word to be displayed is a main frame word, blank the WORD SELECT FRAME and INTERVAL DISPLAYS. To write blanks depress one of the blank pushbuttons on the keyboard for each digit.

d. If a subcommutated word is to be displayed select the appropriate subframe synchronizer by depressing either DISPLAY SF1 or SF2 pushbutton. Select the word number and frame number of the data to be displayed and enter blanks for the interval as described above.

e. If a main frame super commutated word is to be displayed, select the word number and interval, and blank the frame number as described above. Interval is the number of words between recurrences of the selected channel.

f. If the super subcommutated word is to be displayed select the word number, frame number, and interval as described above. Interval is the number of frames between recurrences of the selected channel.

g. The selected data word may be displayed in either binary or decimal form on the DATA displays by depressing either the DISPLAY BIN or DEC pushbutton on the front panel.

h. When displaying data words, depression of the KEYBOARD CONTROL STEP button causes the WORD number to increment.

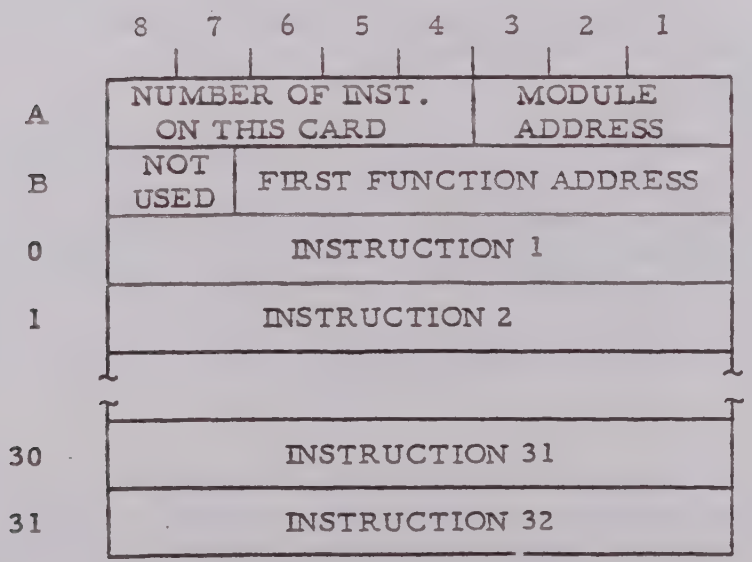
3.2.3 Computer Setup Mode

When the front panel SETUP ENABLE --COMP pushbutton is depressed, interface is enabled for programming the Model 710 from a Digital Equipment Corp. PDP-11 Computer Series via an EMR Model 2763 Buffered Data Channel. A full configuration of the 710 (frame sync, two subframe syncs, simulator and VWL function) is programmed with 115 16-bit instructions, plus three 16-bit instructions for each variable word length position programmed. A basic configuration (programmable frame sync) can be loaded with 32 16-bit instructions. The programmable inputs to the 710 are the same for computer setup mode as they are for local or card reader setup modes except for computer program verification and reset capabilities. (Refer to Table 3-3, Function Address 31).

3.2.4 Card Reader Setup Mode

With the front panel SETUP ENABLE --CR pushbutton depressed, interface is enabled for programming the Model 710 from a Hewlett-Packard Model 11310A Marked Card Reader. Provisions are made for connecting the card reader option to the front panel of the 710 or inputting the card reader program to the rear panel from a remote unit. A Model 710 with all options except VWL can be fully programmed with five cards. Up to 10 VWL locations may be programmed on each additional card. Programming using the marked card option is the same as the manual programming format except for the method of addressing the function Addresses. Each marked card has two additional line entries identified as A and B on the card as shown below.

MARKED CARD FORMAT



The functions for lines A and B are as follows:

- Function Line A; Bits 1-3

  A binary number defining the module address for the data contained on this card. For example, module address 1 = frame synchronizer.

- Function Line A; Bits 4-8

  A binary number specifying the number of data lines used on this card (not including lines A and B). All 0's are decoded as 32 data lines.

- Function Line B; Bits 1-6

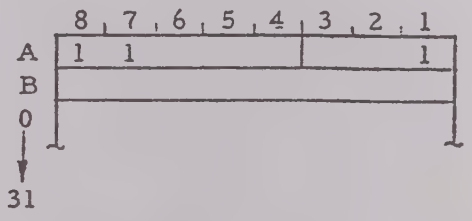
  A BCD number which specifies the starting function number where the data specified in function line 0 through function line n will start loading.

Example 1:

Module address ---------- 1

No. of data lines used on this card ---------- 24

Starting function number ------- 0

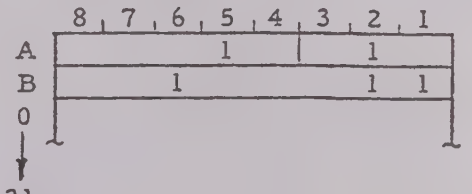


Example 2:

Module address ---------- 2

No. of data lines used on this card ---------- 2

Starting function number ------- 23



It is recommended that after loading, the card reader programmed format be verified as described in paragraph 3.2.2.2 .

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section describes the operation of the three basic cards in the Model 710 PCM Decommutator (Frame Synchronizer Card, Word Select and Display Card, and Data Entry Card) and the three optional functions (Subframe Synchronizers 1 and 2, PCM Simulator and Variable Word Length. Refer to Figure 4-1.) Two levels of card descriptions are provided; a functional description referenced to an overall block diagram and detailed descriptions of the individual circuits identified on the card level block diagram. The detailed descriptions are referenced to associated functional block/logic diagrams. Each of these diagrams is referenced to appropriate schematic diagram (Section 6) by drawing number and sheet number to facilitate locating the specific circuit on the schematics.

4.2 FRAME SYNCHRONIZER (Figure 4-2)

The frame synchronizer requires a serial NRZ-L data stream and its related 0° clock signal at TTL levels as inputs. The frame synchronizer utilizes an all-digital, five-mode, adaptive pattern correlator. Any combination of up to 33 ones and zeros (including "don't cares" within the pattern, if necessary) can be accomodated by the pattern correlator. In the Search mode, the most likely pattern position is determined by checking all possible pattern positions and selecting that one containing the fewest errors. Once this position is determined, the unit enters the Verify mode for verification of the periodic recurrence of the transmitted pattern. If the adaptive mechanism is enabled, a perfect pattern in the Verify mode causes an immediate transition to the Lock mode, thus assuring rapid data acquisition in the event that data quality warrants. With the adaptive mechanism disabled, the pattern (within a programmable error tolerance) must occur for a programmable number of consecutive frames prior to the transition to the Lock mode. Once in Lock, receipt of an unacceptable pattern (acceptability governed by a programmable error tolerance) causes entry into the Check mode. In Check, the pattern position is interrogated for a programmable number of frames with the result that either receipt of one acceptable pattern returns the unit to Lock (thereby tolerating occasional noise bursts) or receipt of the required number of unacceptable patterns reverts the unit to Search for re-entry into the acquisition phase. An Auxiliary Sync mode is provided for those operators who want to leave the Search mode upon detection of the first acceptable pattern. The programmed errors for the Verify mode set the acceptable pattern in the Search mode.

An additional feature of the frame synchronizer is the automatic polarity inversion detection and correction function. This function searches continually for receipt of an inverted pattern (as might occur due to signal inversion in external hardware). When two consecutive inverted patterns are received, the incoming data stream is automatically inverted without loss of synchronization.

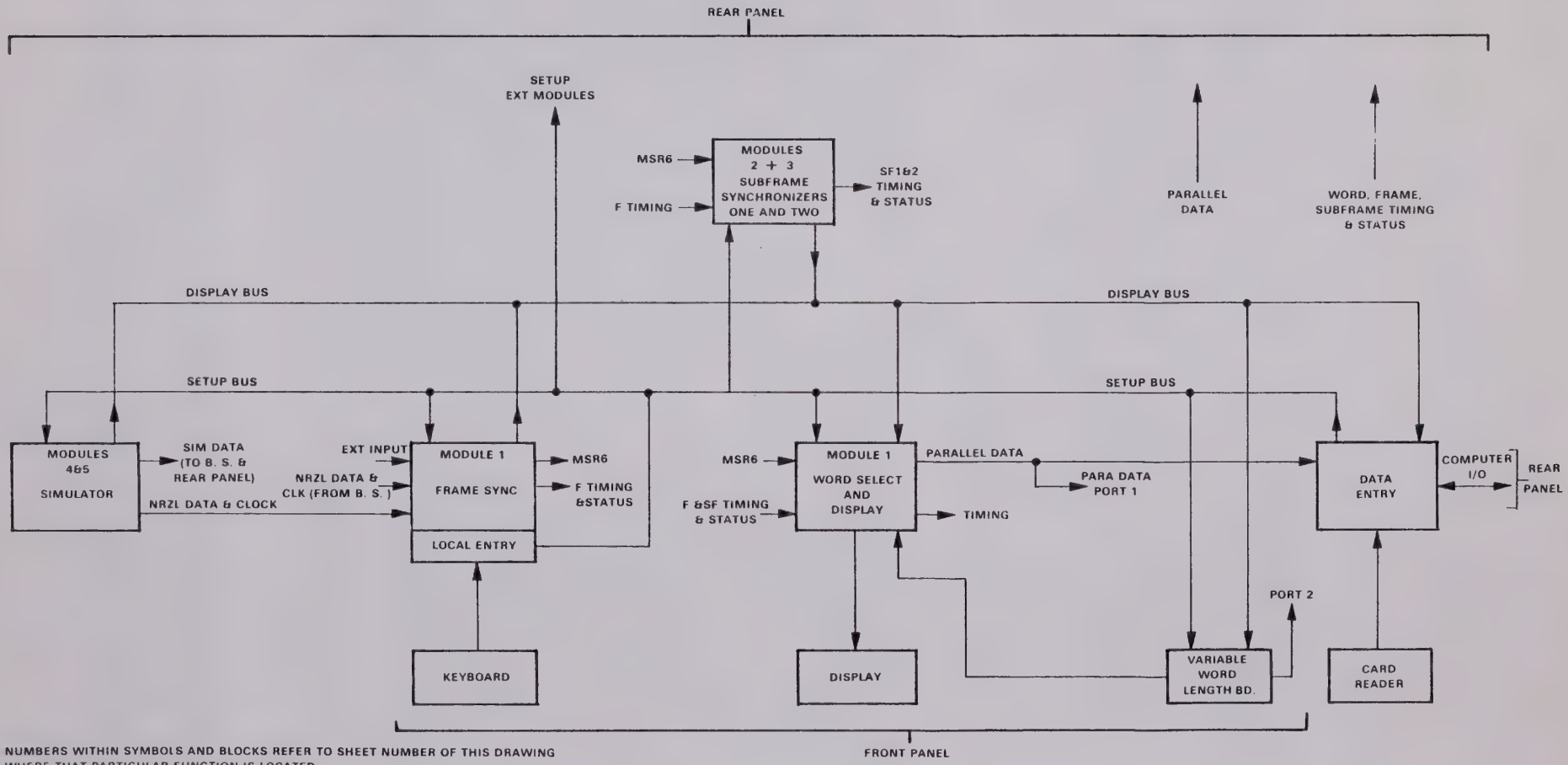


Figure 4-1 Overall Block Diagram

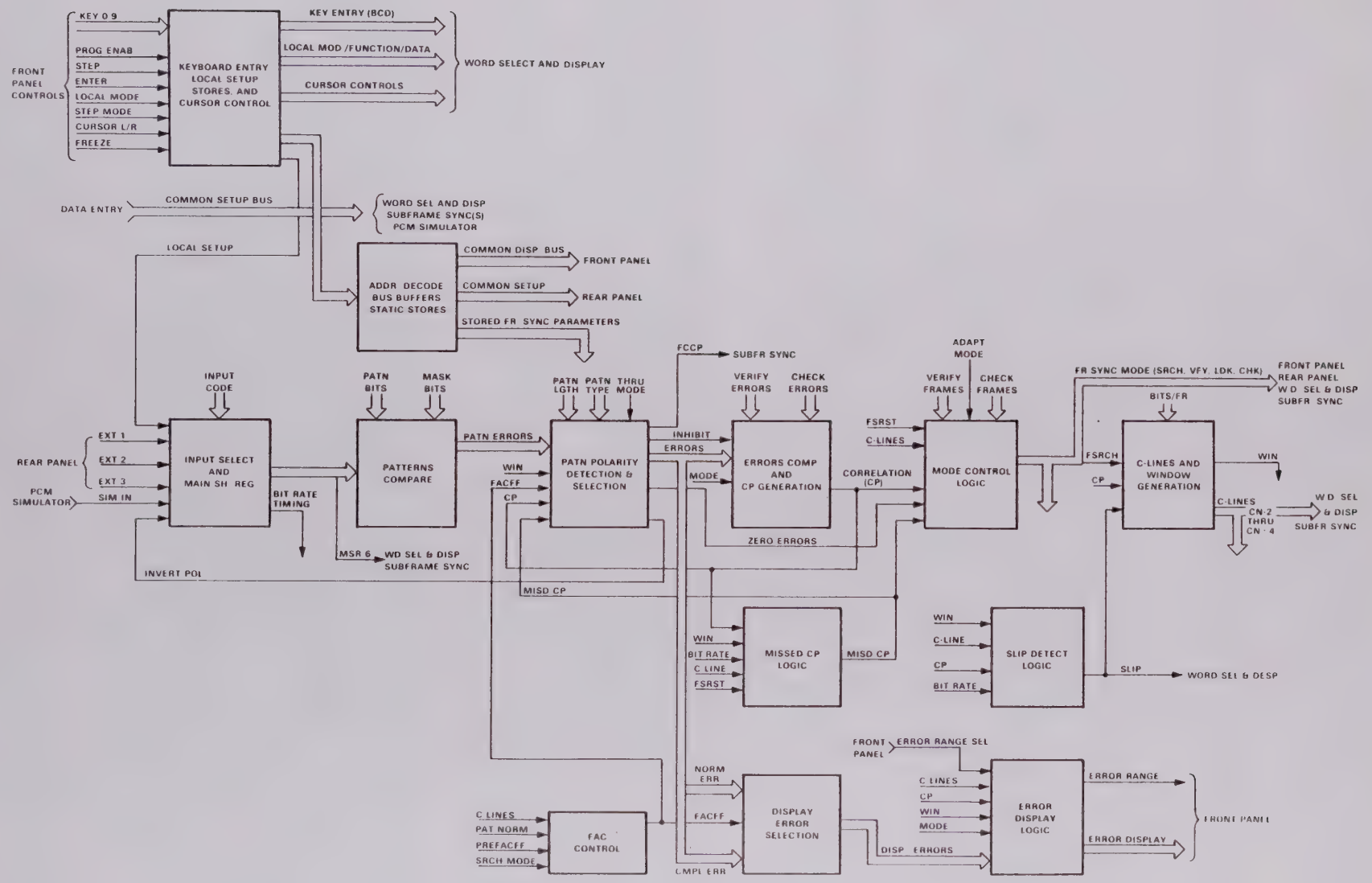


Figure 4-2 Frame Synchronizer Block Diagram

The following paragraphs describe the operation of frame synchronizer functional circuits as shown on Figure 4-2. The numbers within symbols and blocks of the individual circuit diagrams refer to the sheet number of the schematic diagram (Drawing No. 34595) on which the particular function is located.

4.2.1 Keyboard Entry, Local Setup Stores, and Cursor Control (Figure 4-3)

4.2.1.1 Keyboard Entry

The eleven output lines from the keyboard are routed to an 11 line BCD converter. (Blank is decoded as all ONES. Its use is described in the Word Select and Display theory of operation.) When a key is depressed, the BCD output is simultaneously applied to the module, function and data store inputs. A flag pulse, which occurs when any key is depressed, generates KEYSTROBE following a 20 millisecond delay which allows the BCD data to settle on the store inputs. KEYSTROBE will load the module, the function, or one of the eight data bit stores depending upon which gate is presently enabled.

In addition to its programming function, the keyboard is used to select a word, frame, and interval when in the word select mode. KEYSTROBE and BCD data are routed to the Word Select and Display card for this purpose.

4.2.1.2 Local Setup Stores

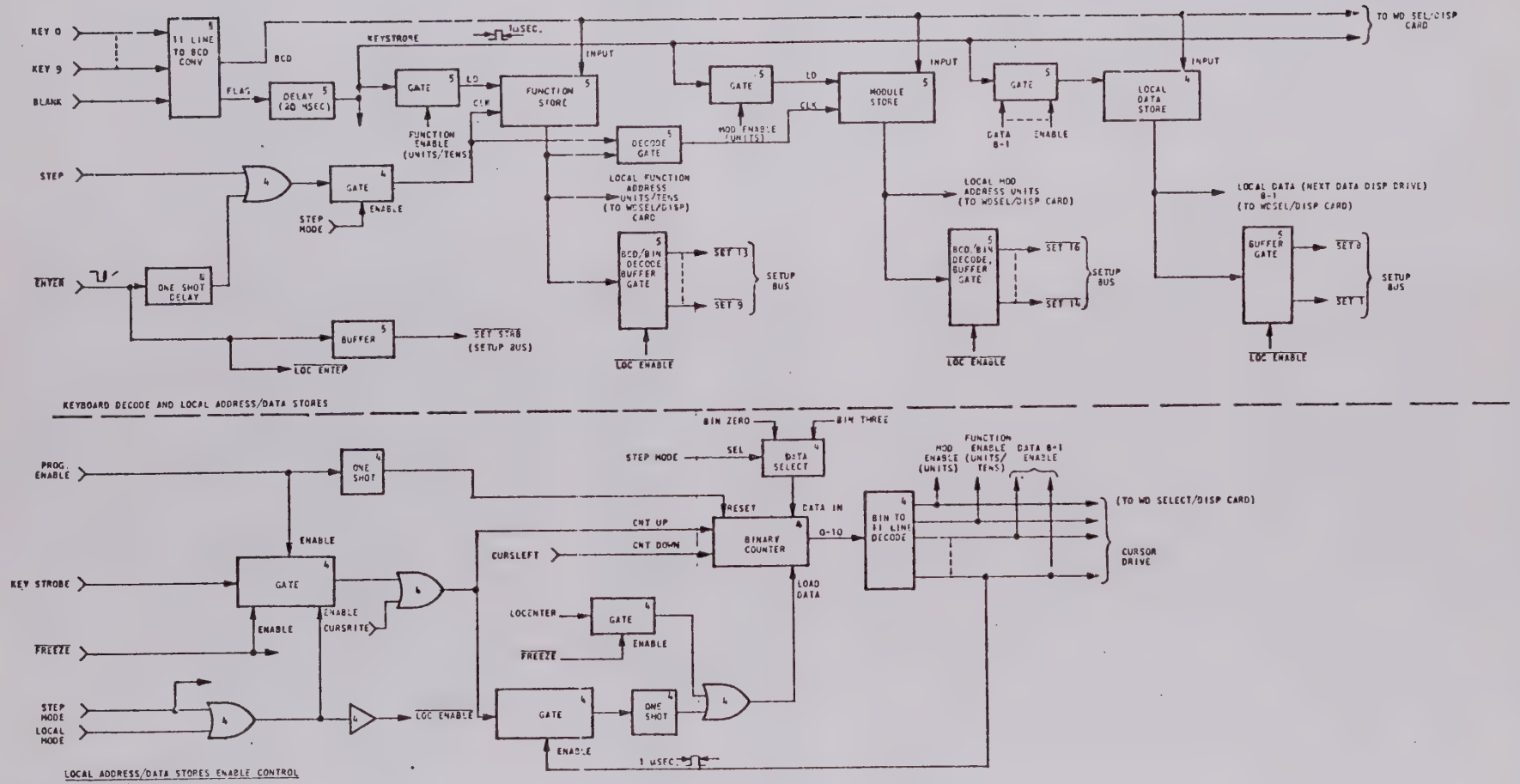
When the 710 is in the LOCAL or STEP mode the module, function and data store outputs are gated onto the setup bus by $\overline{\text{LOC ENAB}}$. If the 710 is in the card reader, or computer mode, these gates are inhibited. The module, function and data store outputs also go to the Word Select and Display card where they ultimately drive the front-panel display.

The BCD outputs from the module and function stores are converted to binary and buffered prior to driving the setup bus, and the data stores are simply buffered prior to driving the setup bus.

In the STEP MODE, the module and function stores can be incremented by one, from two sources, the STEP and ENTER buttons on the front panel. STEP MODE enables a gate which allows STEP or $\overline{\text{ENTER}}$ to clock the stores. STEP simply increments the function stores and is useful when examining the stores. The leading edge of $\overline{\text{ENTER}}$ generates $\overline{\text{SET STRB}}$ which loads LOCAL DATA ($\overline{\text{SET 1}}$-$\overline{\text{SET 8}}$) into the selected module and store. The trailing edge of $\overline{\text{ENTER}}$ increments the function store. There are 32 function addresses (0-31). When the function store reaches 31, a decode gate is enabled. The next clock pulse will increment the function store to zero and also increment the module store by one. The decode gate is then inhibited until the function store again reaches 31.

4.2.1.3 Cursor Control

This logic has two major functions. First, it controls the specific function, module or local data store into which the keyboard data is loaded and second, it drives the corresponding cursor on the front-panel display to indicate to the operator which store will be loaded by the subsequent keyboard operation.



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

Figure 4-3. Keyboard Entry, Local Setup Stores, and Cursor Control

The main components are a binary counter which ranges from 0 through 10 and a decoder which enables one of eleven output lines. Control of the counter (count up, count down, reset, load) is determined by front-panel operation.

When the keyboard is placed in PROG mode, PROG ENAB goes to a one level. This provides an enable to the KEYSTROBE gate and also triggers a one shot which resets the binary counter to zero. The zero count is decoded as MOD ENAB which enables the load gate to the module store. If the unit is under LOCAL or STEP control and the keyboard is not in FREEZE, the KEYSTROBE GATE is fully enabled and the next KEYSTROBE will first enter the BCD data into the module store and then increment the counter by one. The decoder output now enables the function tens store. Subsequent KEYSTROBES load the function units store and local data stores 8 through 1 and after each load operation increment the counter by one. When the decoder output reaches DATA 1 ENAB, a load gate to the counter is enabled. The next CNT UP pulse will load the counter. The one shot following this gate ensures that the load pulse overrides the CNT UP input to the counter. The counter is also loaded when the front-panel ENTER button is depressed and the keyboard is not in FREEZE. If the unit is not in step mode, binary zero is loaded into the counter providing an enable to the module store and bringing the display cursor back to the module display. If the unit is in the step mode, it is not necessary to load the module or function from the keyboard because these stores automatically increment by one, when the ENTER or STEP buttons are depressed. Therefore, a binary three is loaded into the counter providing an enable to DATA 8 and moving the display cursor back to the MSB of the NEXT DATA display.

The Cursor Right and Cursor Left buttons increment the counter up or down by one count each time they are depressed. They provide a means of moving the enable/cursor to a specific store without disturbing the other stores.

Placing the keyboard in FREEZE locks the counter at its present state by inhibiting KEYSTROBE clocks to the counter and blocking load pulses to the counter. This locks the enable/cursor in position and allows repeated changes to be made to a store. In this mode, the enable/cursor can still be moved by the cursor controls.

4.2.2 Address Decode, Bus Buffering and Static Stores (Figure 4-4)

$\overline{\text{SET 16}}$ through $\overline{\text{SET 13}}$ of the setup bus enable the frame sync address decoder. $\overline{\text{SET 12}}$ through $\overline{\text{SET 9}}$ are decoded to provide one of 14 address enables ($\overline{\text{FSADR 0}}$ through $\overline{\text{FSADR 13}}$). Note that the Frame Sync and the Word Select and Display stores are both under Module One address. It is the level of $\overline{\text{SET 13}}$ which determines which address decoder will be enabled.

$\overline{\text{SET 8}}$ through $\overline{\text{SET 1}}$ are buffered and applied to the static store inputs. When $\overline{\text{FSSTRB}}$ occurs, data is entered into the addressed store. The store address also enables the display bus drive circuit and the store content is displayed on the front panel.

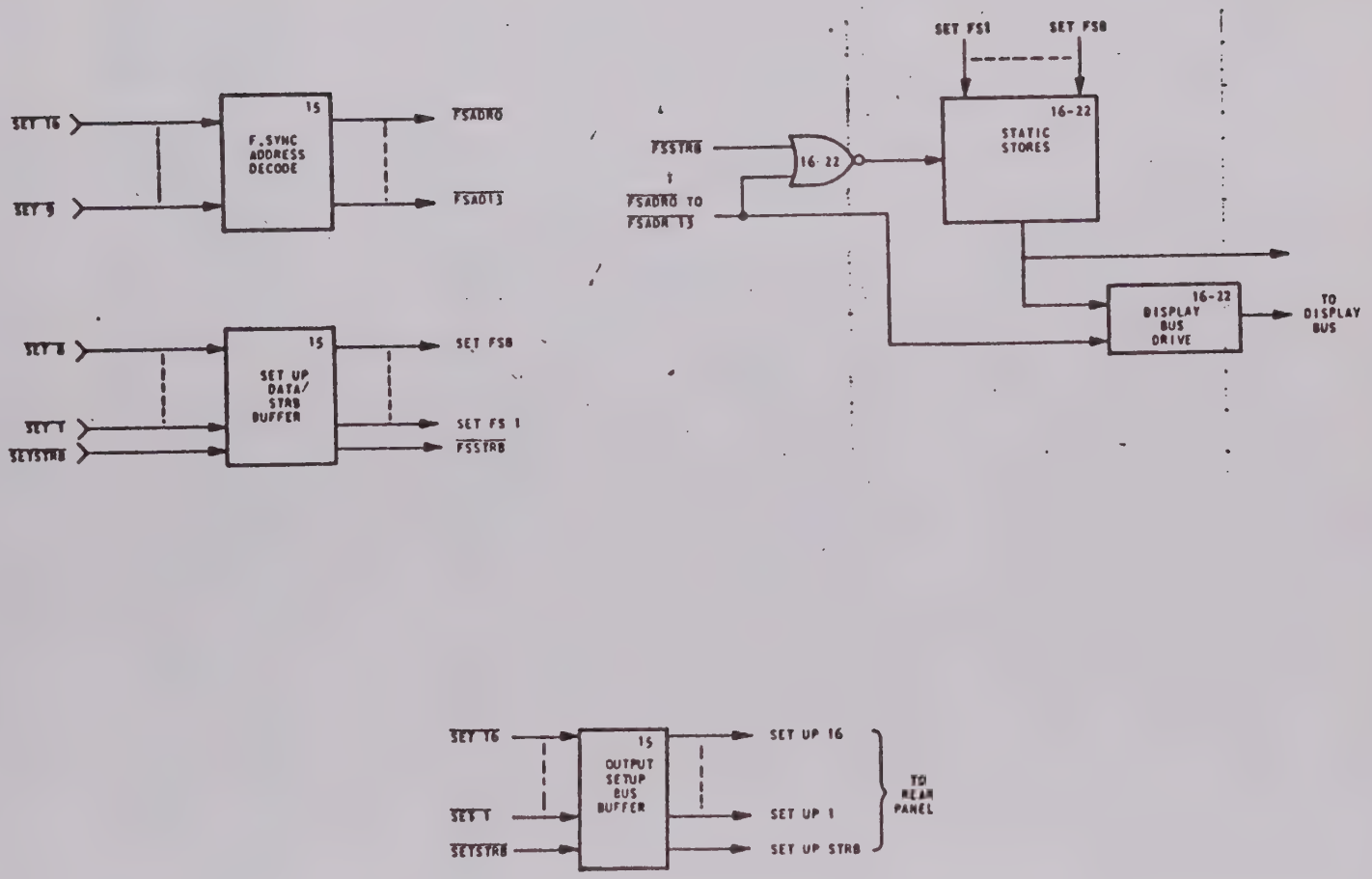


Figure 4-4. Address Decoders, Static Stores, and Bus Buffers

The internal setup bus is buffered and routed to the rear panel. This output allows setup of other units from the 710.

4.2.3 Input Select Polarity Control, Main Shift Register and Patterns Comparator Circuits (Figure 4-5).

4.2.3.1 Input Select

The frame synchronizer requires both NRZ-L data and 0° clock. One of four inputs can be selected by front-panel switch. EXT 1, EXT 2, and EXT 3 inputs are BNC connector inputs on the rear panel. Outputs of the internal simulator can also be selected as inputs to the frame synchronizer. The clock drives the B BIT and M BIT generators. The outputs of these generators are 40 nanosecond pulses. B BIT coincides with the rising edge of the clock and M BIT coincides with the falling edge of the clock. These are the basic timing pulses in the synchronizer. The serial data is routed to the main shift register via a polarity gate. The polarity of this gate output is controlled by $\overline{\text{INPOL}}$.

4.2.3.2 Auto Polarity Control

The frame synchronizer will resolve input data polarity ambiguity when in the auto polarity control mode. This is accomplished by looking for the frame sync pattern and its complement. The polarity control logic monitors $\overline{\text{PATN}}$ (pattern normal) and adjusts the state of $\overline{\text{INPOL}}$ to cause $\overline{\text{PATN}}$ to be a zero level. This logic consists of a two stage counter and the $\overline{\text{INPOL}}$ flip-flop which is armed by the counter and clocked by the CN+3 pulse. The counter is clocked by coincidence of WIN, CP and M BIT. CP (correlation pulse) is generated when the frame sync pattern or its complement is detected. As long as frame sync pattern is detected, $\overline{\text{PATN}}$ will be a ZERO and this inhibits the counter. If the complement of frame sync pattern is detected, $\overline{\text{PATN}}$ will be a ONE level and allow the counter to increment. Detection of two consecutive inverted patterns causes the counter to increment to the count of two and arm the $\overline{\text{INPOL}}$ flip-flop. At CN+3 time, $\overline{\text{INPOL}}$ is switched and the data stream into the main shift register is inverted. Anytime a MISDCP (missed correlation pulse) is generated the counter will be reset to zero.

4.2.3.3 Main Shift Register and Patterns Comparator

The polarity gate output is applied to a 33-bit shift register which performs serial-to-parallel conversion of the data stream. Data is shifted through the register at bit rate. The main output from this register is a 33-bit parallel "slice" of the data stream which is routed to the pattern comparator. A second output from the register is MSR6 which is a delayed version of the input data stream. It is obtained from stage 6 of the register and routed to the subframe synchronizer.

In the pattern comparator, the parallel output from the shift register is compared to the 33 bits programmed in the pattern stores. The 33 output lines from this comparator each represent a specific pattern bit position. When the received bit and pattern bit agree, the output line for that bit position goes to a ZERO

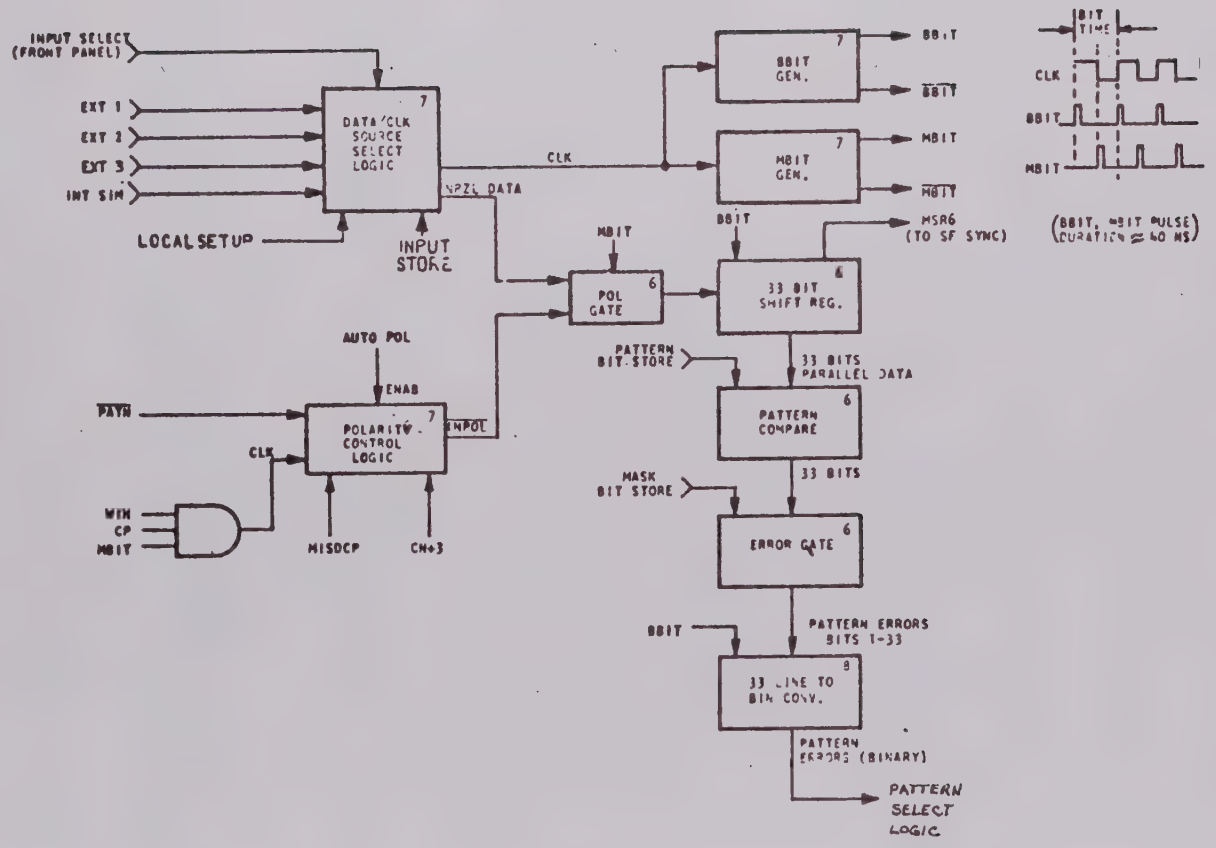


Figure 4-5. Input Select, Polarity Control, Main Shift Register and Pattern Comparator Circuits

level. When they disagree, the output line goes to a ONE level indicating an error. The pattern comparator output is routed through an error gate to a 33 line to binary converter. A second input to the error gate, the mask bits, either gate the 33 pattern comparator outputs through, or set zero levels on the corresponding inputs to the converter. This allows sync patterns of less than 33 bits or specific bits within a pattern to be masked out.

The binary converter sums the ONES appearing on the 33 input lines and provides a binary output representing the total errors in the pattern. Because the propagation delay from input to output of the converter becomes a factor at higher bit rates, a partial sum store is included in the converter.

4.2.4 Pattern Polarity Detection and Selection (Figure 4-6)

When the synchronizer is in the FAC, FCC or AUTO POL modes, it is necessary to examine both the normal pattern errors and the complement pattern errors. The normal pattern error output from the binary converter is stored in the NORM PATN ERR STORE. It is also routed to a comparator and to a logic network which subtracts it from the total number of bits in the pattern. The result of this subtraction is the number of errors in the complement pattern. The complement pattern error output is routed to the comparator and to the COMPL PATN ERR STORE.

The pattern polarity detection logic monitors the comparator output, sets the level of PREPATN to select the normal or the complement pattern errors, whichever is smallest, for application to the error compare and CP generation logic. The selected error count also goes to the zero error decode flip-flop. This circuit generates an output when a perfect pattern (no errors) is detected. At CN-2 times, the ZERO ERRORS output is set to zero. The CN pulse (coincides with CP) will set the output to a ONE level if there are no pattern errors. One bit time after setting PREPATN, the pattern polarity detection logic generates PATN (pattern normal) and its complement. PATN will be a ONE when the normal pattern errors are less than or equal to the complement pattern errors.

In the FCC mode, the sync pattern of the final frame is inverted and $\overline{\text{PATN}}$ will be set to a one level. This signal is gated with WIN, CP and M BIT to produce $\overline{\text{FCCP}}$ (frame code complement pulse) which is routed to the subframe synchronizer.

When the frame synchronizer is in the normal pattern mode, the pattern polarity detection logic is inhibited by $\overline{\text{NORM PATN}}$. This forces selection of the NORM PATN ERR STORE for application to the error compare and CP generation logic. It also forces PATN to a ONE level regardless of the comparator output.

The purpose of the pattern type decode logic is to decode the pattern type stores (NORM PATN, FAC, FCC, AUTO POL) and generate appropriate enable signals. The AUTO POL and $\overline{\text{NORM PATN}}$ outpus are static levels. AUTO POL enables the polarity control logic when this mode is selected and $\overline{\text{NORM PATN}}$ controls the pattern polarity detection logic. The ENAB MISDCP RST which enables the missed correlation pulse reset logic, is a static ONE level when the NORM PATN, FCC, and AUTO POL modes are selected. In the FAC mode, this output will be a ONE level only is PATN and $\overline{\text{FACFF}}$ are at opposite levels.

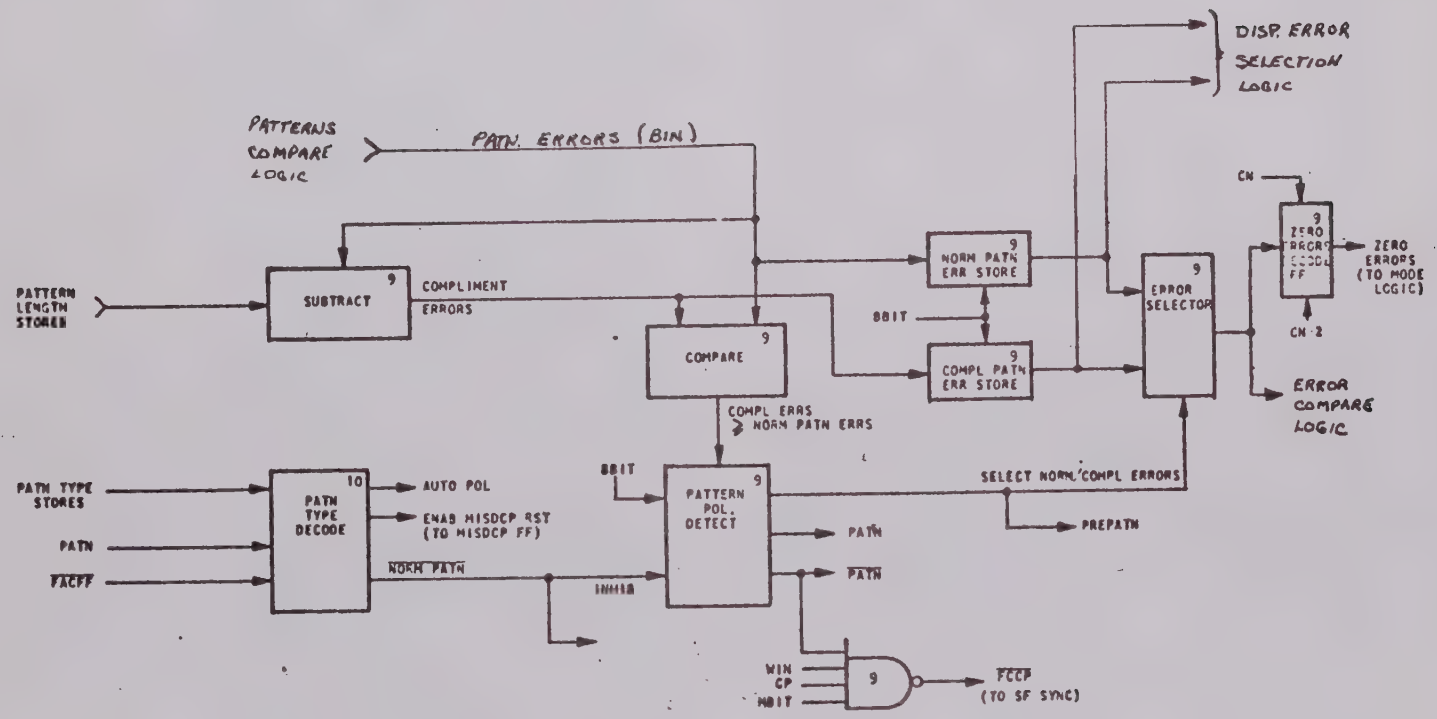


Figure 4-6. Pattern Polarity Detection and Selection Circuits Functional Block Diagram

4.2.5 Error Compare and CP Generation (Figure 4-7)

The purpose of this logic is to compare the incoming error count with various allowable error stores and generate or not generate CP (correlation pulse) based upon this comparison. It also seeks out the best pattern (least errors) over a complete frame before advancing out of the search mode.

The error bus control logic monitors several status and C lines and generates an enable to one of four error store buffers which drive one input to a comparator. The other input to the comparator is the actual pattern error count. The normal sequence as the synchronizer advances from search to lock is as follows: The nine error buffer is enabled placing a nine count on the comparator input. When an actual pattern error count of less than nine occurs, the first CP is generated.

The nine error buffer is disabled and the error store buffer is enabled for at least the next complete frame. During this time, the synchronizer is searching for the best pattern (least errors). If a subsequent pattern contains less errors than the previous best pattern, the latter is discarded and replaced by the better pattern. The synchronizer will again cycle through a complete frame looking for a better pattern. If no better patterns are found, one bit time before the end of the frame (CN-1), the error store buffer is disabled and the verify error buffer is enabled. If the selected pattern meets the allowable verify errors, CP is generated and the synchronizer advances to verify mode. The verify buffer remains enabled while the synchronizer is in verify mode. If it reverts to search, the verify buffer is disabled and the error store buffer is again enabled. If the synchronizer advances to lock, the verify buffer is disabled and the check/lock buffer is enabled.

The error comparator has two outputs; one when the input pattern errors are less than the allowable errors, and the second when the input pattern errors are equal to the allowable errors. During the interval when the synchronizer is looking for the best pattern, the A = B output is inhibited by FSRCH because the synchronizer is looking for a better pattern, not simply an equally good pattern. However, after looking over a complete frame and not finding a better pattern, the $\overline{CN-1}$ pulse enables the A = B input because the incoming pattern at this time is, in fact, the last best pattern received but occurring one frame later. Once the synchronizer leaves the search mode, the A = B inhibit is removed and the A = B or the A $<$ B will generate CORREL (correlation). During the bit period following CORREL, CP is generated and CPDLY is generated following CP. Both of these pulses are one bit time in duration. Generation of CORREL also causes the pattern errors to be loaded into the error store. When searching for the best pattern, the output of this store is the reference against which subsequent patterns are compared.

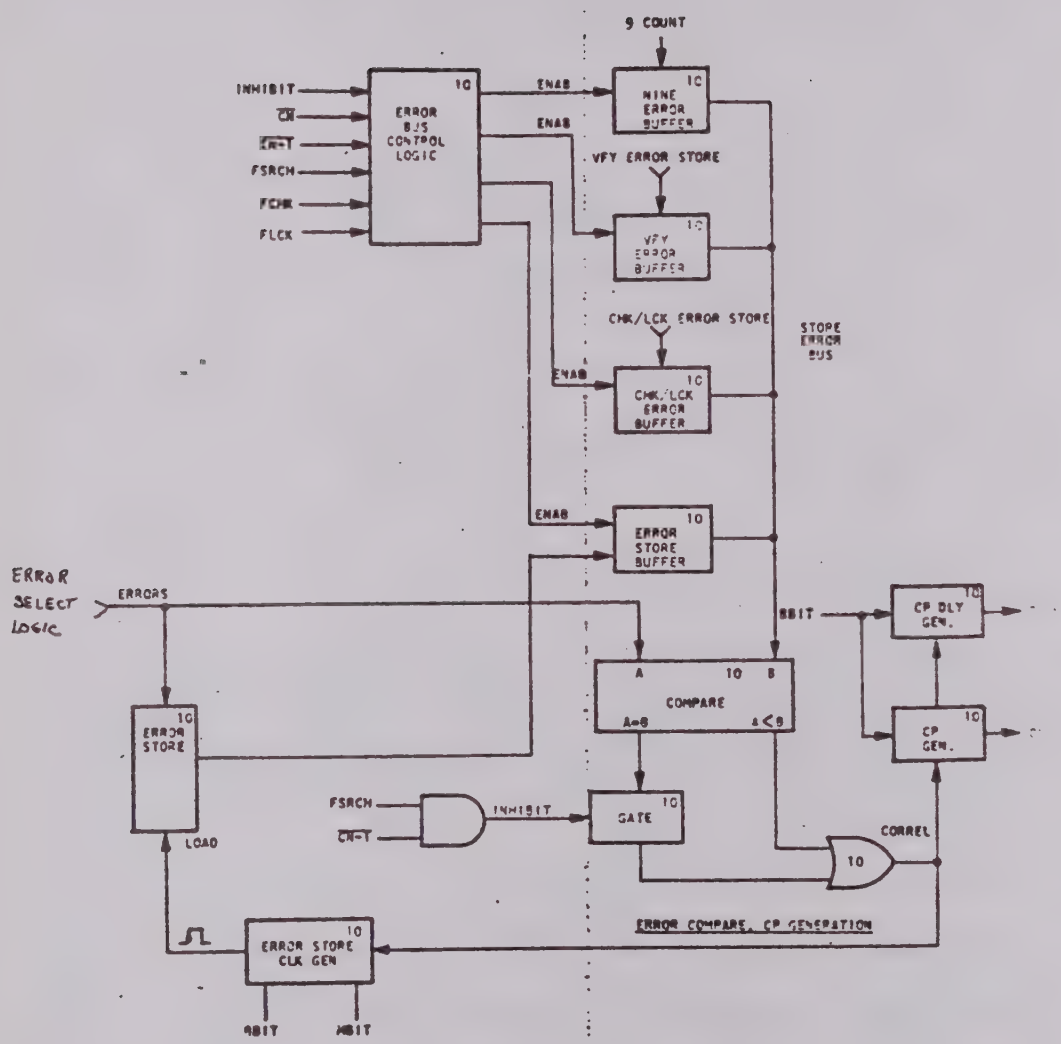


Figure 4-7. Errors Compare and Correlation Pulse Generator

4.2.6 Missed CP Logic (Figure 4-8)

This logic detects the absence of a correlation pulse within the programmed window and provides this information to the polarity control and mode control logic. Each frame just prior to the expected CP time, the MISDCP flip-flop is set to a ONE level (CN-2 time) indicating a missed CP. If CP and WIN (window) are coincident, the flip-flop will be reset. If not it remains set. The ENAB MISDCP RST signal remains at a ONE level in the NORM PATN, FCC and AUTO POL modes. In the FAC mode, this signal is a ONE level only if the frame sync pattern is the complement of the previous frame sync pattern.

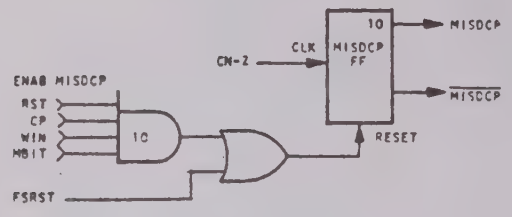


Figure 4-8. Missed CP Logic Circuit

4.2.7 Mode Control Logic (Figure 4-9)

The frame synchronizer can be in one of four modes; search, verify, lock or check. The manner in which it sequences through these modes depends upon several parameters; MISDCP, FR COMP, ADAPT, ZERO ERRS, SORV and LORC. The MISDCP (missed CP) and FR COMP (indicates patterns frame counter has reached the programmed verify or check frame number) are combined to indicate four possible conditions:

- o MF indicates missed CP and have frame count compare.
- o $M\overline{F}$ indicates missed CP and no frame count compare.
- o $\overline{M}F$ indicates received CP and have frame count compare.
- o $\overline{MF}$ indicates received CP and no frame count compare.

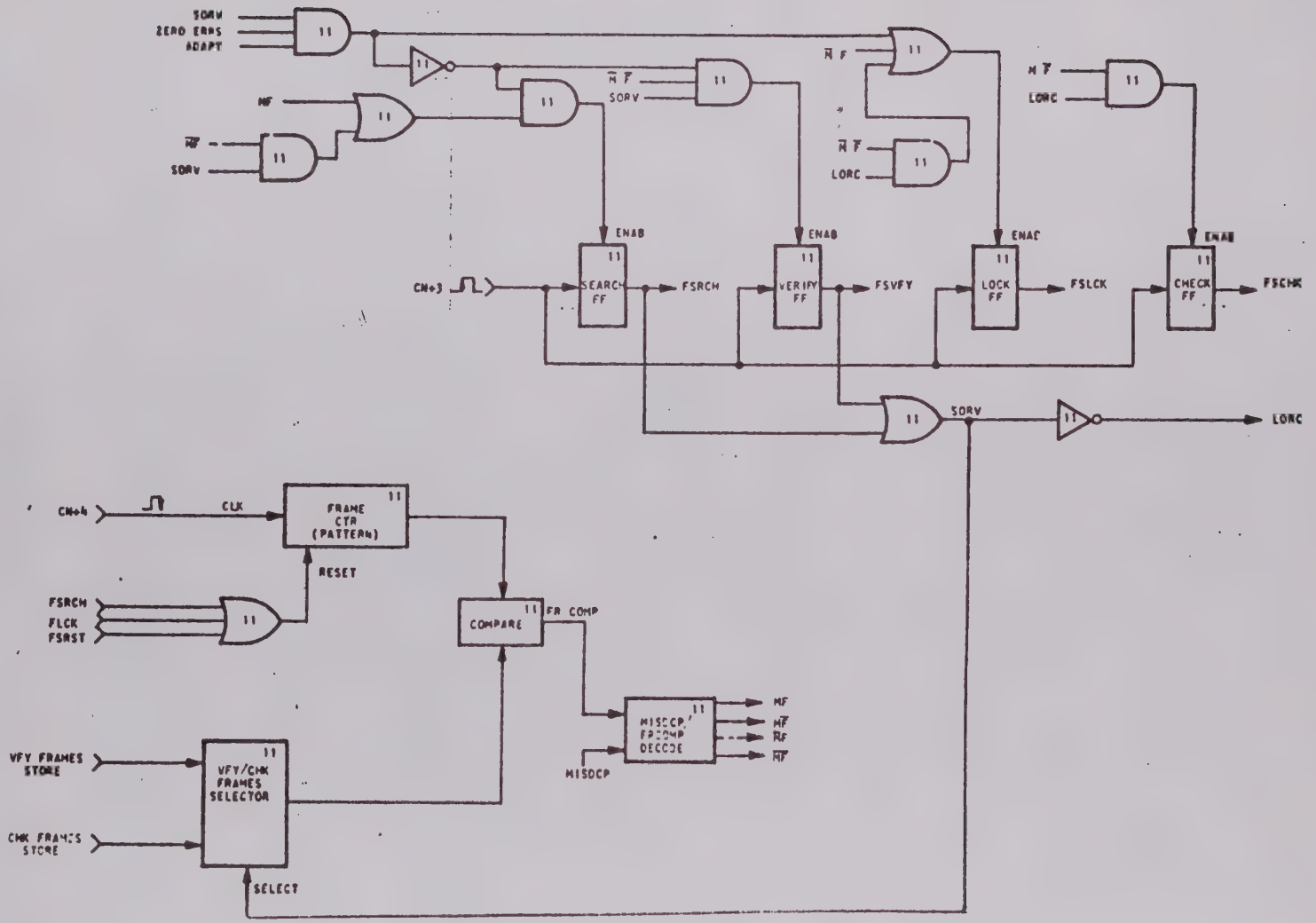


Figure 4-9. Mode Control Logic Circuit

Assuming the sync strategy is non adaptive (ADAPT = 0), the synchronizer would normally advance from search to verify where it remains for a programmable number of frames (0 to 15). If one CP is missed during this time, it reverts to search mode. If there are no missing CP's, the synchronizer advances to lock mode. It remains in lock unless a missing CP occurs, at which time it advances to the check mode for a programmable number of frames (0 to 15). During this time, one good pattern (CP generated) will return the synchronizer to the lock mode. After remaining in the check mode for the programmed number of frames and not detecting one good pattern, the synchronizer will return to the search mode.

The described sequence is modified as follows when the sync strategy is programmed to adaptive (ADAPT = 1): If the synchronizer is in search mode and a perfect pattern occurs (zero errors), the mode logic will bypass verify and advance to the lock mode. If the synchronizer is in verify mode and a perfect pattern occurs, it will ignore the programmable verify frames and advance to the lock mode.

The pattern frame counter is incremented only in the verify or check modes. In search or lock a reset is held on the counter causing the frame count to remain at zero. Note that when the synchronizer is in search and the verify frames store is programmed to zero, a FR COMP is present. When a CP is received $\overline{MF}$ will go to a ONE level and the synchronizer will advance immediately to lock bypassing the verify mode. Also note when the synchronizer is in lock and the check frames store is programmed to zero, a FR COMP is present. If a missing CP occurs; MF goes to a ONE level and the synchronizer will bypass check mode and revert immediately to search.

4.2.8 C Line Generation (Figure 4-10)

The C line pulses are a series of adjacent bit-wide pulses beginning two bits prior to CP (CN-2 time) and terminating four bits after CP (CN+4 time). With the exception of one pulse (CN+2 DLY), they begin and terminate at B BIT time. CN+2 DLY begins at mid bit of CN+2 and terminates at mid bit of CN+3.

The bits/frame store content is loaded into a decrementing counter at CP DLY time if in the search mode and at CN+1 time if not in the search mode. When the count equals four (this corresponds to CN-3 time because counter was loaded one bit after CP time), the C line generator is enabled.

Anytime bit slip occurs (CP andCN not coincident), it becomes necessary to rephase the C line generator to the new CP position. The $\overline{SLIP}$ input to the generator forces the subsequent output from the generator to be a CN+1 pulse regardless of the previous output.

The purpose of the inhibit generator is to prevent C line generation and enable the 9 error buffer. Initially, $\overline{FSRST}$ will set the inhibit line. Following the first CP, which indicates a pattern with less than 9 errors was found, CP DLY will reset the inhibit line removing the C line inhibit and disabling the 9 error

buffer. One frame later, a CN pulse is generated. If a CP coincides with CN, the inhibit line remains reset. If CP is missing or occurs at some other time, CN will set the inhibit line again. Once the synchronizer leaves search, the inhibit line remains reset.

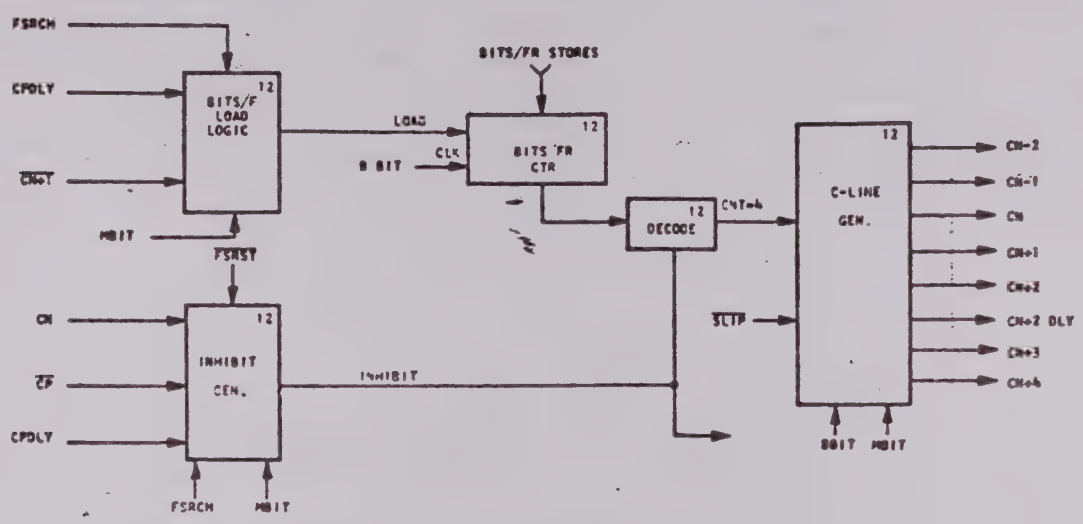


Figure 4-10. C-Lines Generator

4.2.9 Window Generation (Figure 4-11)

During initial synchronization phases, it is important that the selected sync pattern be correct, therefore, the time slot (window) during which a CP will be accepted is held to a minimum. Once the correct pattern has been found however, occasional data bit dropouts or time skews of the input data stream may not be sufficient reason to return to the search mode. Therefore, the window can be widenedto allow slippage. During search or verify modes , the window generator is inhibited (LORC =0) and WIN output is one bit side (CN). During lock or check, the WIN output is programmable. It is set by $\overline{CN}$, $\overline{CN-1}$ or $\overline{CN-2}$ and reset respectively by $\overline{CN+1}$, $\overline{CN+2}$ or $\overline{CN+3}$. The window stores determines whether the 1-bit, 3-bit or 5-bit window is generated.

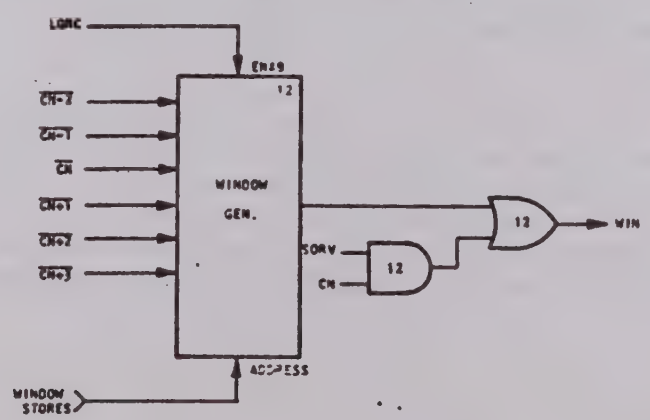


Figure 4-11.. Window Generator

4.2.10 Slip Detect Logic (Figure 4-12)

In normal operation, CP and CN are time coincident. Both represent the last bit of the frame sync pattern. CP indicates receipt of a frame sync pattern and CN represents a count-down from the previous CP. If there has been a data dropout or time skew of the serial data into the frame synchronizer during the frame, CP and CN will not be coincident and it becomes necessary to rephase the synchronizer on the new CP. The slip detect flip-flop output is set to a ONE by a CP which occurs within WIN but not coincident with CN. CP DLY resets the flip-flop one bit time later. SLIP is routed to the C line generator to rephase the C line outputs.

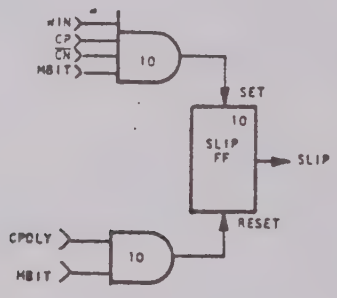


Figure 4-12. Slip Detect Logic Circuit

4.2.11 FAC Control FF (Figure 4-13)

This logic performs two functions. First, in the FAC mode the frame sync pattern polarity is alternately normal then inverted and CP can be generated by either pattern polarity. However, the FACFF output combined with PATN in the pattern type decode logic insures that only a pattern which is the complement of the previous frame sync pattern received will enable the MISDCP reset logic. The second function is to select the normal or complement error store in FAC mode for transfer to the error display logic.

During the time the synchronizer is searching for the best pattern, $\overline{\text{PREFACFF}}$ will be generated whenever a CP is generated. After finding the best pattern, $\overline{\text{PREFACFF}}$ is inhibited. $\overline{\text{PREFACFF}}$ combined with PATN and $\overline{\text{PATN}}$ will set or reset FACFF depending upon the polarity of the received pattern. The purpose is to properly phase the FACFF to the frame sync pattern. After selecting the best pattern, the synchronizer will not generate another CP until one frame

later. At this time, the trailing edge of CN-1 will toggle the FACFF anticipating a complemented sync pattern. After advancing out of the search mode, CN+3 toggles the FACFF each frame.

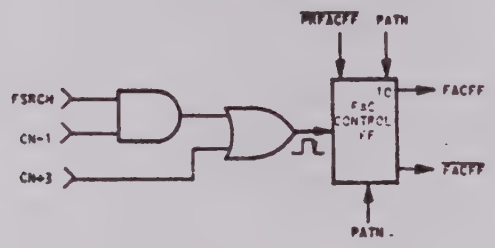


Figure 4-13. FAC Control Logic Circuit

4.2.12 Display Error Selection (Figure 4-14)

The purpose of this logic is to select the normal or the complement pattern errors for input to the error display logic. Inputs to the error display control logic are the pattern type stores, PREPATN and FACFF. In the NORM PATN and AUTO POL modes, the normal pattern errors are selected for input to the error display logic.

In the FCC mode, the polarity of the PREPATN input determines whether the normal or complement pattern errors are selected. During all frames except the final one, PREPATN will be a ONE level and the normal pattern errors are selected for display. In the final frame, the sync pattern will be inverted forcing PREPATN to a ZERO level. The error display control output changes state and selects the complement pattern errors for display.

In the FAC mode, the sync pattern alternates between normal and inverted polarity each frame. This causes FACFF and consequently the error display control output to alternate selecting the normal pattern errors one frame and the complement pattern errors the following frame.

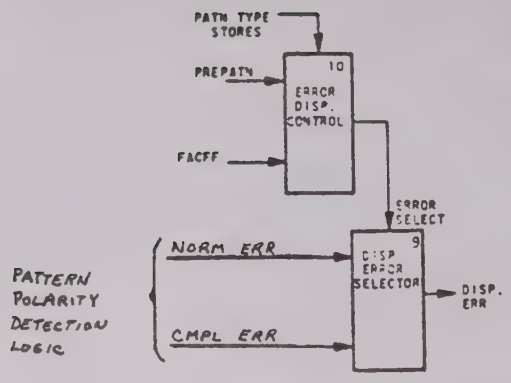


Figure 4-14. Display Error Selection Logic

4.2.13 Error Display Logic (Figure 4-15)

The purpose of this logic is to accumulate the total number of frame sync pattern errors over one, ten or one hundred frame sync patterns and indicate the result on the front-panel error display. A maximum of 99 errors can be displayed.

The input to the display error store (DISP ERR) is being updated each bit time. However, the only error count of interest is when the sync pattern is present. Therefore, the store clock is derived from CP and/or CN. There are three possible conditions. Under nominal conditions, CP and CN are coincident and the correct error count will be entered. A second condition is, when bit slippage occurs, the error count associated with CP time is the desired one. When CP occurs early due to slippage, the associated error count will be entered into the store. The error count associated with CN time will not be entered because the CN pulse is inhibited in the C line generator logic by SLIP. When CP occurs late, the CN pulse will have already occurred and an incorrect error count will be present in the store. However, the store output is not utilized until CN+3 time. The maximum delay CP can have and still remain within WIN is CN+2 time. Therefore, the store will be corrected prior to entry into the error accumulator at CN+3 time. The final condition is when missed CP occurs. The synchronizer will advance to the check mode and remain there for a number of frames before reverting to search, or, if CP is again detected, the synchronizer will return to lock. Under these conditions, it is still desirable to use the error count and CN which continues to occur during this time, clocks the display error store.

The output of the display error store is added to the present error accumulator output and at mid bit of CN+3, this sum becomes the new accumulator store output. The accumulator store is reset to zero by one of two conditions. If the synchronizer is in search or verify, a hard reset is held on the store. If the synchronizer is in lock or check, the store is reset by the frame count decode logic.

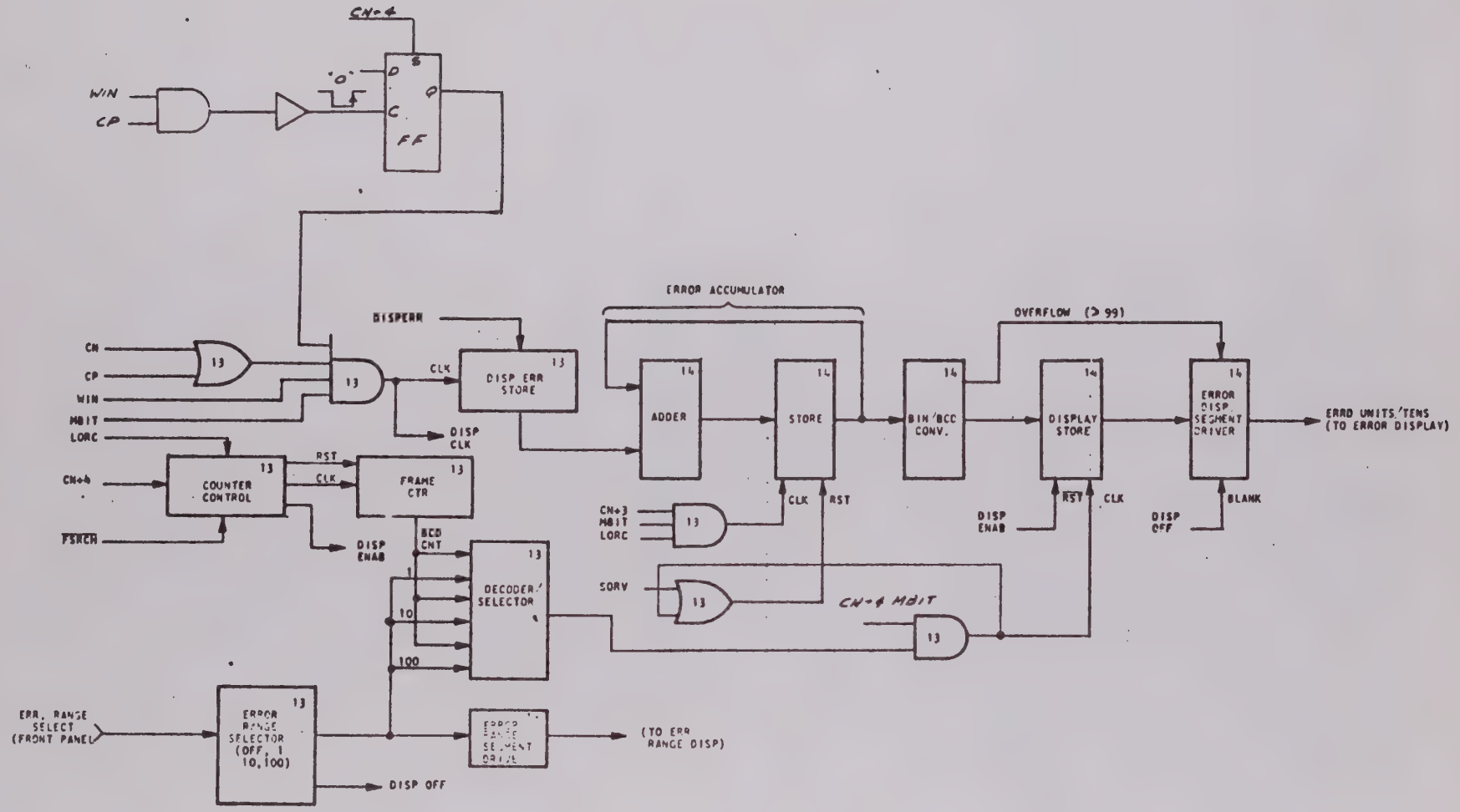


Figure 4-15. Error Display Logic Functional Block Diagram

The frame sync pattern error display can be turned off or set to display accumulated errors over 1, 10, or 100 frames. The error range selector enables one of three circuits which decode a frame counter output. The decoder output resets the error accumulator store and also enables the display store clock. The error accumulator output is converted to BCD and applied to the display store input. The BIN/BCD converter also provides an overflow indication (more than 99 errors) on the display.

4.2.14 Frame Sync Initialize and Reset (Figure 4-15A)

The power on initialize circuit contains a FET switch connected to ground and an RC network which turns the switch off after a time delay. This results in a forced $\overline{\text{FSRST}}$ which initializes counters and places the synchronizer in the search mode. This condition can also be implemented from the front panel by the Frame Sync Reset button.

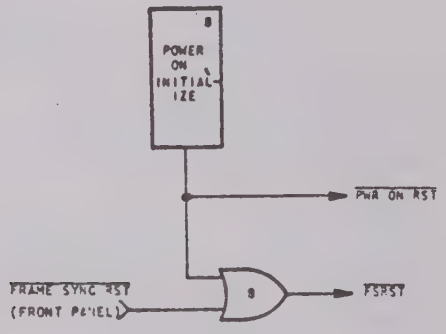


Figure 4-15A. Frame Sync Initialize and Reset Logic

4.3 WORD SELECT AND DISPLAY CARD (Figure 4-16)

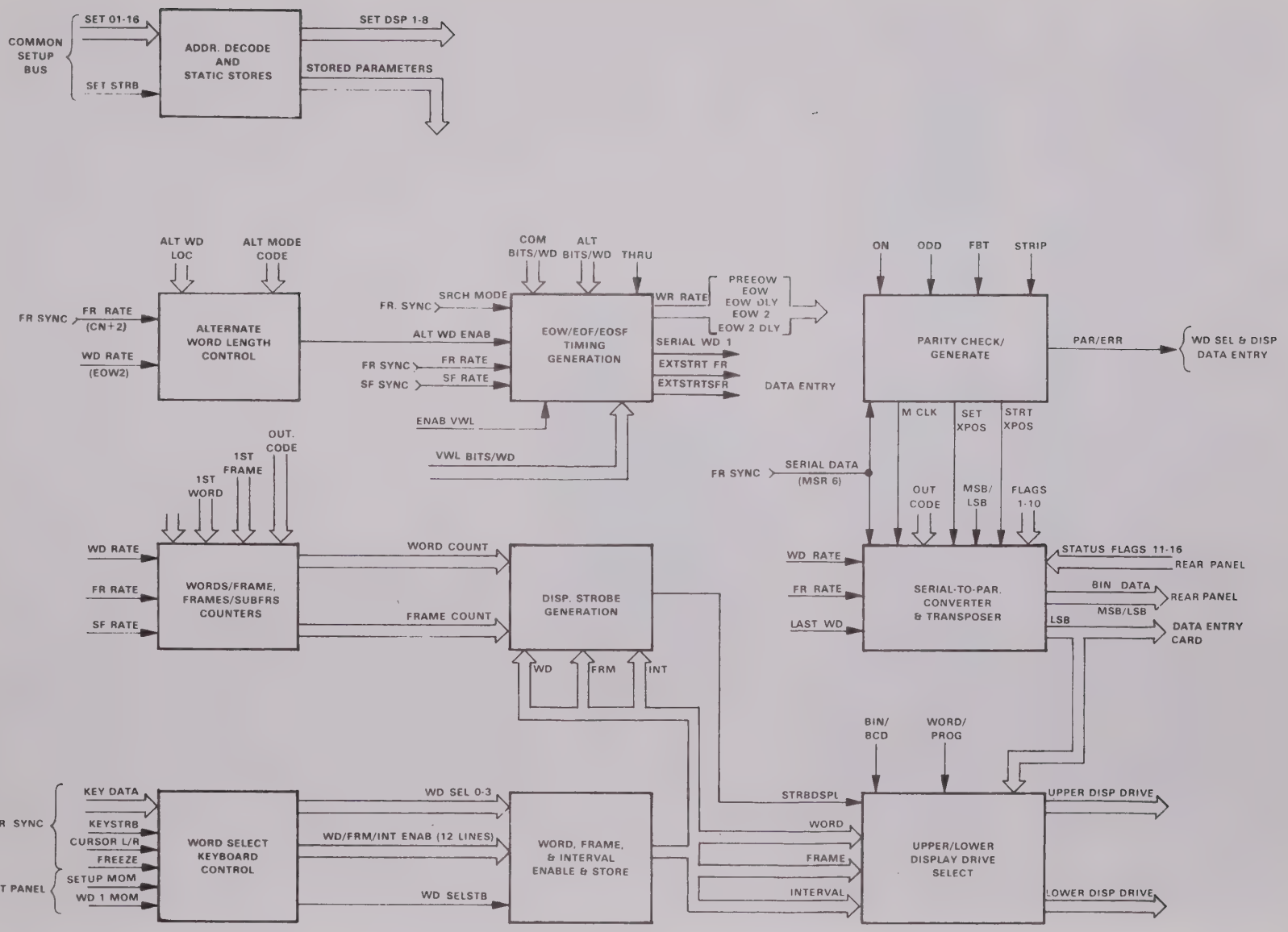
The Word Select and Display Card accepts data and timing inputs from the Frame Synchronizer and Subframe Synchronizer Cards and setup instructions from the common setup bus. Serial data is converted to parallel and routed to the rear panel for distribution to external equipment. The parallel data output is also applied to the Data Entry Card for distribution to the computer. The Word Select and Display Card generates word, frame and subframe timing pulses used for internal timing and are also outputted with the parallel data for external timing control.

This card also controls the front panel Program and Word Select displays. In the Word Select mode any word in the data format can be selected for display in binary or decimal form. Subcommutated or supercommutated words and alternate word lengths are accommodated. The Word Select and Display Card also contains the circuits for parity check or generation.

The following paragraphs describe the individual functional circuits of the Word Select and Display Card.

Note

The numbers within the symbols and blocks of the individual circuit diagrams refer to the sheet number of the Word Select and Display Card schematic diagram (Section 6 - Drawing No. 34595) where the particular function is located.


COMMON SETUP BUS
SET 01-16
SET STRB
ADDR. DECODE AND STATIC STORES
SET DSP 1-8
STORED PARAMETERS
ALT WD LOC
ALT MODE CODE
FR SYNC
FR RATE (CN+2)
WD RATE (EOW2)
ALTERNATE WORD LENGTH CONTROL
COM BITS/WD
ALT BITS/WD
THRU
SRCH MODE
FR. SYNC
ALT WD ENAB
FR SYNC
FR RATE
SF SYNC
SF RATE
EOW/EOF/EOSF TIMING GENERATION
WR RATE
PREEOW
EOW
EOW DLY
EOW 2
EOW 2 DLY
SERIAL WD 1
EXTSTRT FR
EXTSTRTSFR
DATA ENTRY
ENAB VWL
VWL BITS/WD
ON
ODD
FBT
STRIP
PARITY CHECK/ GENERATE
PAR/ERR
WD SEL & DISP DATA ENTRY
M CLK
SET XPOS
STRT XPOS
FR SYNC
SERIAL DATA (MSR 6)
OUT CODE
MSB/ LSB
FLAGS 1-10
OUT. CODE
1ST FRAME
1ST WORD
WD RATE
FR RATE
SF RATE
WORDS/FRAME, FRAMES/SUBFRS COUNTERS
WORD COUNT
FRAME COUNT
DISP. STROBE GENERATION
WD
FRM
INT
WD RATE
FR RATE
LAST WD
SERIAL-TO-PAR. CONVERTER & TRANSPOSER
STATUS FLAGS 11-16
REAR PANEL
BIN DATA
REAR PANEL
MSB/LSB
LSB
DATA ENTRY CARD
BIN/ BCD
WORD/ PROG
FR SYNC
KEY DATA
KEYSTRB
CURSOR L/R
FREEZE
FNT PANEL
SETUP MOM
WD 1 MOM
WORD SELECT KEYBOARD CONTROL
WD SEL 0-3
WD/FRM/INT ENAB (12 LINES)
WD SELSTB
WORD, FRAME, & INTERVAL ENABLE & STORE
STRBDSPL
WORD
FRAME
INTERVAL
UPPER/LOWER DISPLAY DRIVE SELECT
UPPER DISP DRIVE
LOWER DISP DRIVE

4.3.1 Address Decode and Static Stores (Figure 4-17)

The $\overline{\text{SET 1}}$ through $\overline{\text{SET 16}}$ setup data and $\overline{\text{SETSTRB}}$ are applied to the card from the common setup bus. $\overline{\text{SET 16}}$ through $\overline{\text{SET 13}}$ are decoded to enable the Word Select and Display address decoder. $\overline{\text{SET 12}}$ through $\overline{\text{SET 9}}$ are decoded to provide addresses $\overline{\text{WSADR 16}}$ through $\overline{\text{WSADR 23}}$. When $\overline{\text{WSSTRB}}$ occurs, the addressed static store is loaded from the data buffer. The address also enables the appropriate display bus driver which allows the present store content to be read on the front panel display. The stored data establishes the operating parameters for the Word Select and Display Card for a given program format.

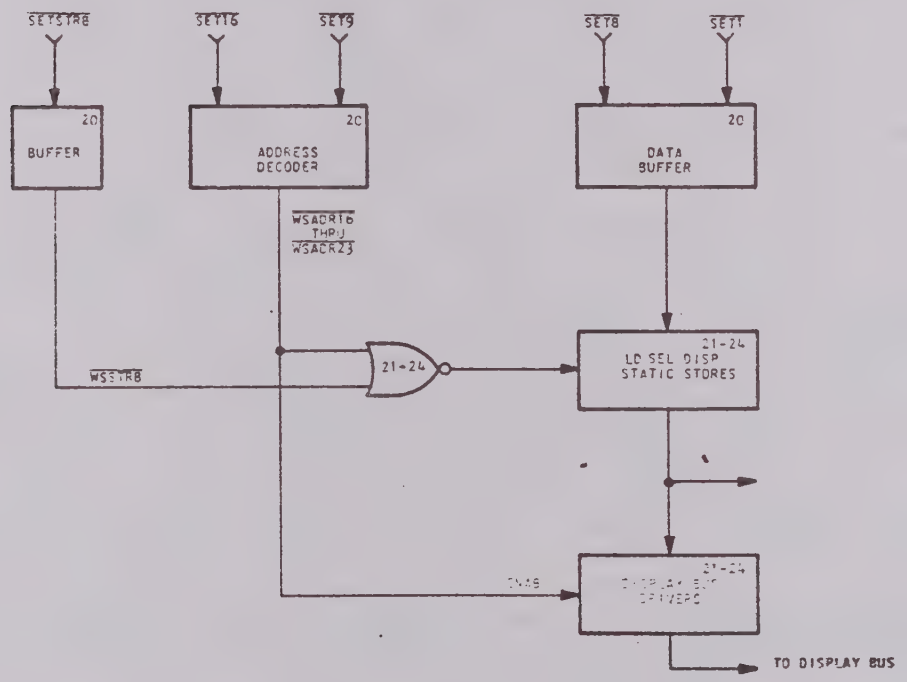


Figure 4-17. Address Decode and Static Stores Functional Block Diagram

4.3.2 Serial-to-Parallel Converter and Transposer (Figure 4-18)

The serial input to the 710 Decom can be LSB first or MSB first data. The purpose of this logic is to convert the data stream into parallel words of programmable length and to provide both LSB aligned and MSB aligned data words. The 710 Decommutator provides one of three output formats: Data Only, Data and Frame Sync Pattern, or Data and Status.

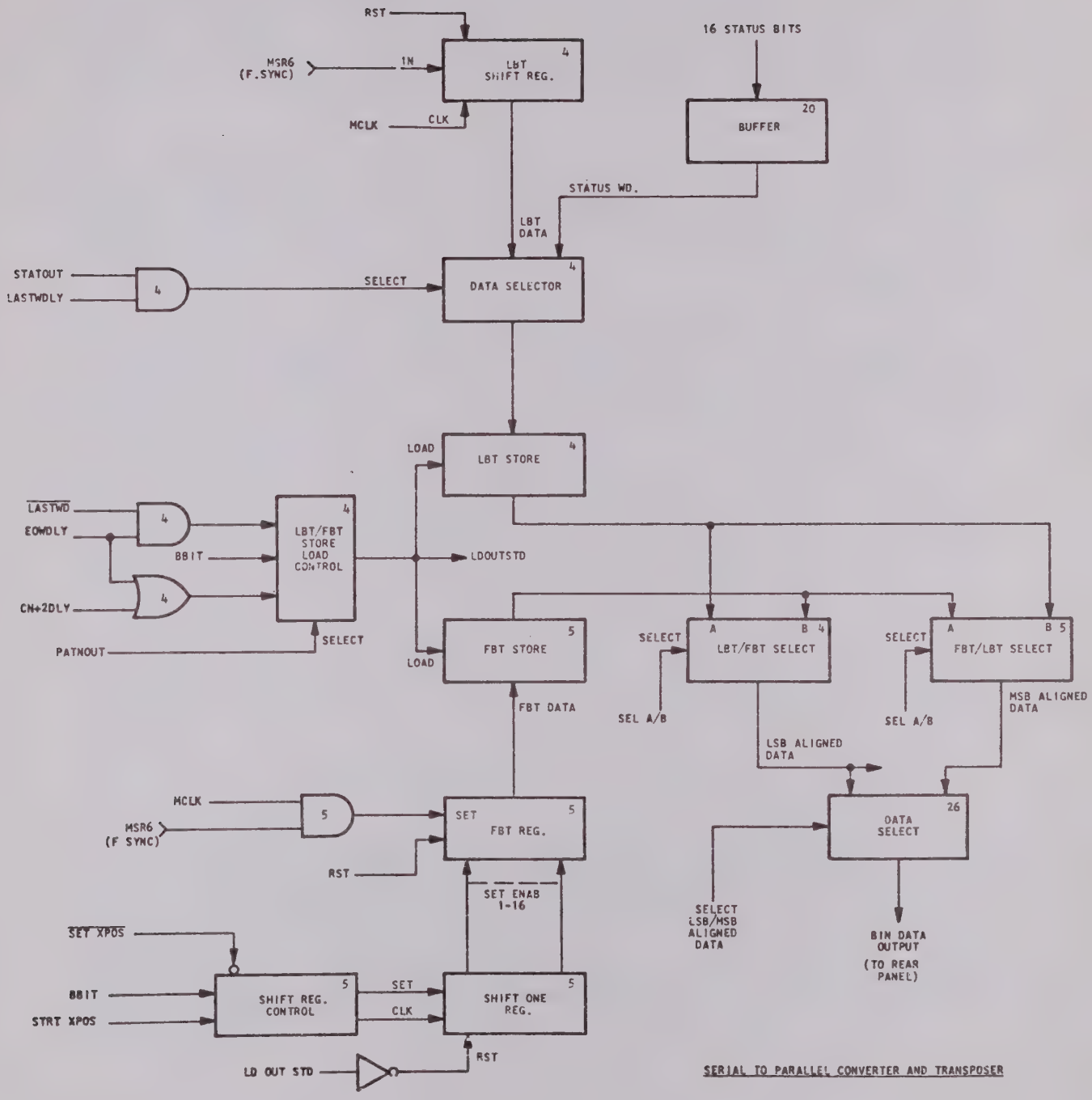
The serial data stream from MSR6 of the frame sync is shifted into the LBT (last bit transmitted) shift register from left to right by the MCLK pulses generated in the Parity Control Logic. The shift register output is applied to a data selector. The other input to this data selector is the status word. When in the Data and Status output mode, the LBT data is applied to the LBT store until LAST WDLY occurs. At this time (while data word one is being assembled in the LBT shift register), the status word is presented to the LBT store.

The load strobe for the LBT store (and the FBT store) is determined by PATNOUT which is a ONE level when in the data and frame sync pattern output mode and a ZERO level in the other modes. In the data only or data and status modes, EOWDLY (end of word delay) generates the store strobe. Subsequent to loading the final data word of a frame, $\overline{\text{LAST WD}}$ inhibits further updates. This signal remains for the duration of the frame sync pattern. In the data and frame sync pattern mode, EOWDLY generates the store strobe. EOWDLY continues to strobe the store during the frame sync pattern chopping it into word lengths equal to data word lengths. The repetition rate of EOWDLY is determined by the data word length stores. Therefore, if the sync pattern length is not a multiple of the data word length, or if it is smaller, the residual bits in the pattern would not be loaded into the store. The [CN+2] DLY pulse which occurs at the end of the pattern generates the load pulse for these bits. Note that the output from the LBT store is always aligned last bit transmitted on the left.

Operation of the FBT (first bit transmitted) logic is different than the LBT logic. At the beginning of each word time, the shift one register is reset to ZERO and a ONE is placed on the set input. This ONE is shifted through the register at bit rate, successively enabling the FBT register set inputs. The FBT register was reset to ZERO simultaneous with the previous FBT store load. If the input data (MSR6) is a ONE level, the shifting ONE is strobed into the enabled FBT register stage. If the input data is a ZERO level, the enabled FBT register stage remains at ZERO. Following assembly of a word in the FBT register, it is strobed into the FBT store. Note that the FBT store is always aligned first bit transmitted on the left. The same data word occurs simultaneously at the LBT and FBT store outputs. The difference is in the bit alignments.

The MCLK pulses and the set transposet (SET XPOS) and start transposer (STRT XPOS) signals control stripping the parity bit from the data words. (Refer to paragraph 4.3.9

The LBT and FBT store outputs are presented to the LBT/FBT selectors. The SEL A/B level, which depends upon whether the decommutator is programmed to receive LSB first or MSB first input data, selects the appropriate output to provide LSB or MSB aligned data. Notice that the status word is merged into the LBT store only. Therefore, at the time the status word is being presented to the output, SEL A/B selects LBT regardless of LSB / MSB first programming. A programmable bit allows selection of LSB or MSB aligned data to the rear panel data output lines.



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

Figure 4-18. Serial-to-Parallel Converter and Transposer Functional Block Diagram.

4.3.3 Alternate Word Length Control (Figure 4-19)

The 710 can decommutate and display two specific data formats containing an alternate word length. In the first, one word of alternate length can occur in a frame. In the second, words of alternate length can occur at regular intervals throughout the frame (every N word where N is programmable from 2 to 99). In the latter format, the location of the first alternate word length is also programmable from 1 to 99.

When the alternate word mode store is programmed for one alternate word length/frame, the two counters are combined into one 4 decade counter by the alternate word mode logic. The alternate word location is loaded into the counter which is then decremented by EOW2. When the count reaches zero ALT WD ENABLE is generated.

In the repeating alternate word length mode, the two counters operate separately. At the end of a frame (CN+2 · M BIT), the first counter is loaded. The loaded data defines the location within a frame of the first alternate length word (programmable from 1 to 99). This counter decrements to zero, generates the first ALT WD ENABLE, and loads the second counter. The number loaded into the second counter represents the interval within a frame at which alternate length words occur. This counter now decrements to zero, generates ALT WD ENABLE, loads itself and continues in this cycle throughout the remainder of the frame. The interval over which this cycle operates is programmable from 2-99 words. At the end of the frame, the first counter is loaded and again takes control of ALT WD ENABLE.

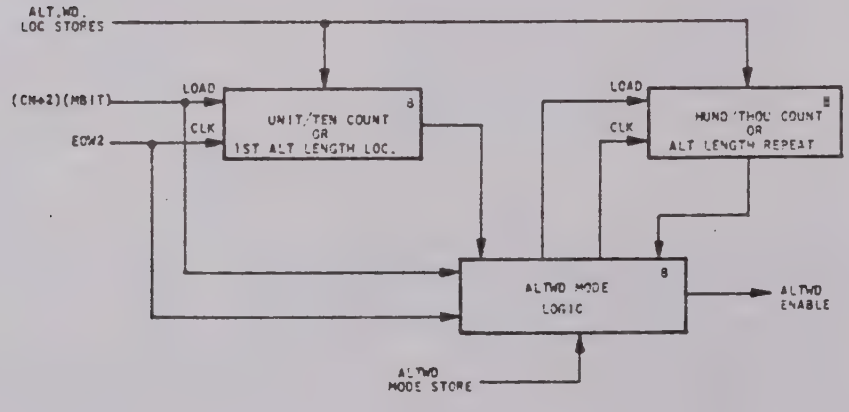


Figure 4-19. Alternate Word Length Control Functional Block Diagram

4.3.4 EOW, EOF, EOSF Timing Generation (Figure 4-20)

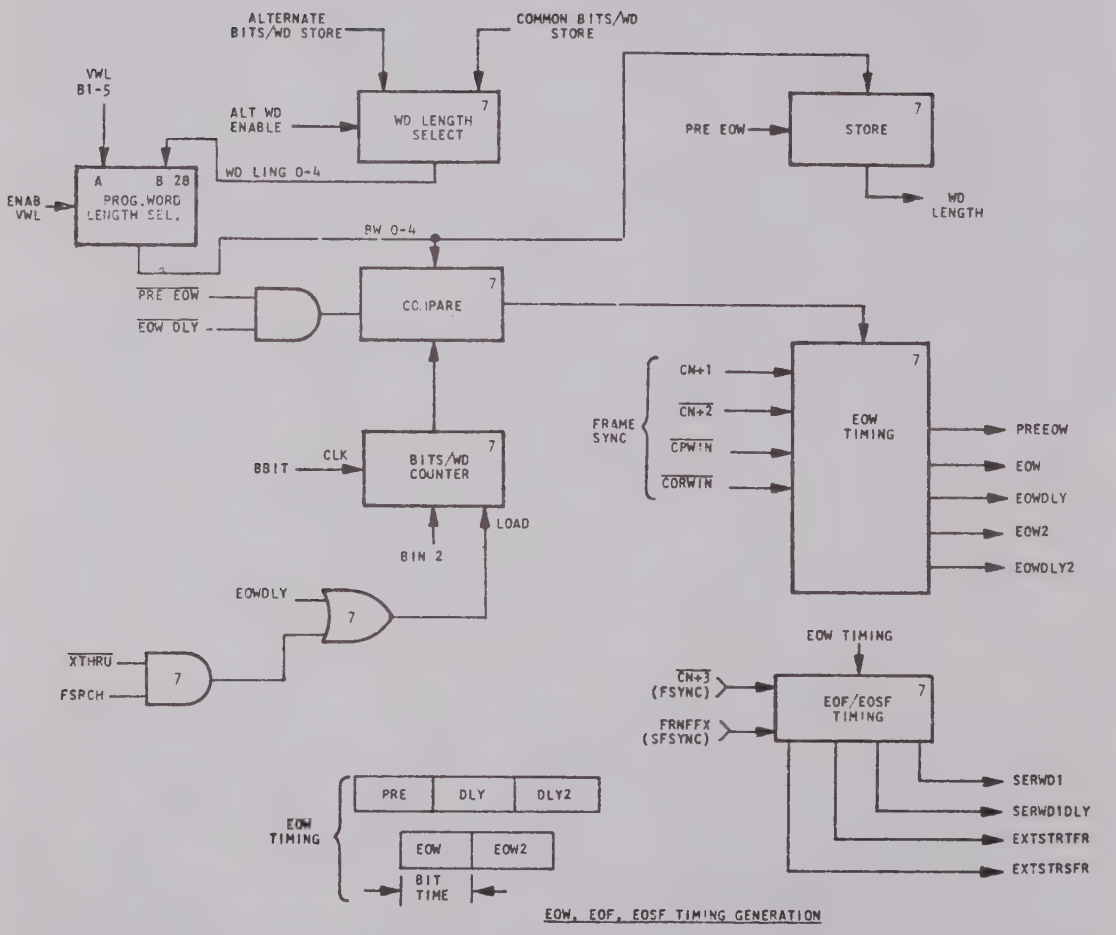
During each word time, a series of bit wide pulses are generated for timing purposes. A bit/word counter output is compared to the selected word length store (common word, alternate word or variable word).

The bits/word counter is continually counting up, loading a two count, counting up, etc. The EOW timing continues through the frame sync pattern time and EOWDLY generates the load pulse. Loading the counter with the count of two instead of one, provides a compare prior to end of word and allows generation of PRE EOW (pre end of word). Normally, when the frame synchronizer is in search mode, a constant load is held on the counter (FSRCH) and EOW timing is not generated. The exception is when the decommutator is programmed to the thru-put (XTHRU) mode. In this mode, the serial input is simply converted into parallel words and output without regard to frame synchronization. Frame synchronizer modes (search, verify, check, lock) are ignored and C lines are not generated. The EOW timing continues to function and the common bits/word store determines the output word length.

The selected word length is also entered into a word length store by EOW. The output of this store controls the leading bit suppression logic when binary data is selected for display on the front panel.

During frame sync pattern time, the bits/word compare continues to generate EOW timing. However, if the frame sync pattern length is not a multiple of the data word length, this compare will not occur during the final segment of the pattern and therefore EOW timing will not be generated at this time. In this case, CN+1 initiates the EOW timing. The $\overline{CN+2}$, $\overline{CP \cdot WIN}$ and $\overline{COR \cdot WIN}$ signals prevent generation of erroneous EOW timing pulses when bit slip occurs.

The EOW timing, $\overline{CN+3}$ and $\overline{FRNFFX}$ generate several timing pulses. SERWD1 is set when the first bit of the first word is in MSR6 and reset when first word assembly is complete. This pulse selects the LBT store output in the serial-to-parallel converter and transposer logic at the correct time to place the status word on the data output. A delayed version of SERWD1 (SERWDIDLY) in conjunction with EOW timing clocks the frame interval counter, the frame counter, and generates EXTSTRTFR (FRATE). EXTSTRTFR is a bit wide pulse coincident with bit one of word one on the data output lines. FRNFFX, from the subframe synchronizer, is combined with EXTSTRTFR to generate EXTSTRTSFR (SFRATE).



EOW, EOF, EOSF TIMING GENERATION

Figure 4-20. EOW, EOF, EOSF Timing Generator Block Diagram.

4.3.5 Word/Frame and Frame/Subframe Counters (Figure 4-21)

The word counter clocks up to the word/frame number and generates a WDN CMP. This compare initiates a series of last word pulses one of which places a load condition on the word counter. When the next clock pulse occurs, the counter is loaded with the first word count (programmable from 0-7) and again counts up to the word/frame number. When the decommutator is in the data only output (DATAOUT) mode, the counter increments up through the final word number. The LAST WD input to the word counter clock logic prevents further clocks to the counter until word one data has been assembled. When this data is presented to the output, the word counter is loaded with the first word count.

When the decommutator is in the data and status word putput mode, the counter increments up to the final word count and remains on this count during frame sync pattern time. When the status word is placed on the output lines (prior to word one data), the word counter is incremented by one.

When the decommutator is in the data and sync pattern output mode, PATNOUT blocks the LAST WD input to the word counter clock logic and the counter continues to increment during the frame sync pattern.

When the decommutator is in search mode, EXT SRCH, which is a delayed version of FSRCH, holds the word counter in a load condition. This ensures a startup on the first word of the frame when the decommutator advances to the verify mode.

In addition to generating WDN CMP, the word count is routed to the display strobe generation logic where it is used to generate the display strobe.

The WDN CMP pulse initiates a series of last word pulses which, depending upon the selected output mode, perform several functions.

LASTWD is used to inhibit the load output store pulse, the word counter clock, WD RATE pulse and DATA RDY reset during the sync pattern interval in data only or data/status modes and to inhibit the ALT WD ENABLE pulse during sync pattern interval in all modes.

LASTWDLY is used to block the extended WDN CMP input to the last word logic in the data only mode, to select the LBT store output for status word output in the data/status mode, to reset DATA RDY prior to presentation of the status word in the data/status mode and to load the word counter in the data/status or data/pattern mode.

LASTWDLY2 is used to load the word counter in the data only mode.

The purpose of the frame counter is to provide a frame count to the display strobe generation logic to be used when displaying subcommutated data. When the subframe synchronizer is in search mode, the DECOM ENABLE signal is at ZERO level. This inhibits subcommutated display strobes and

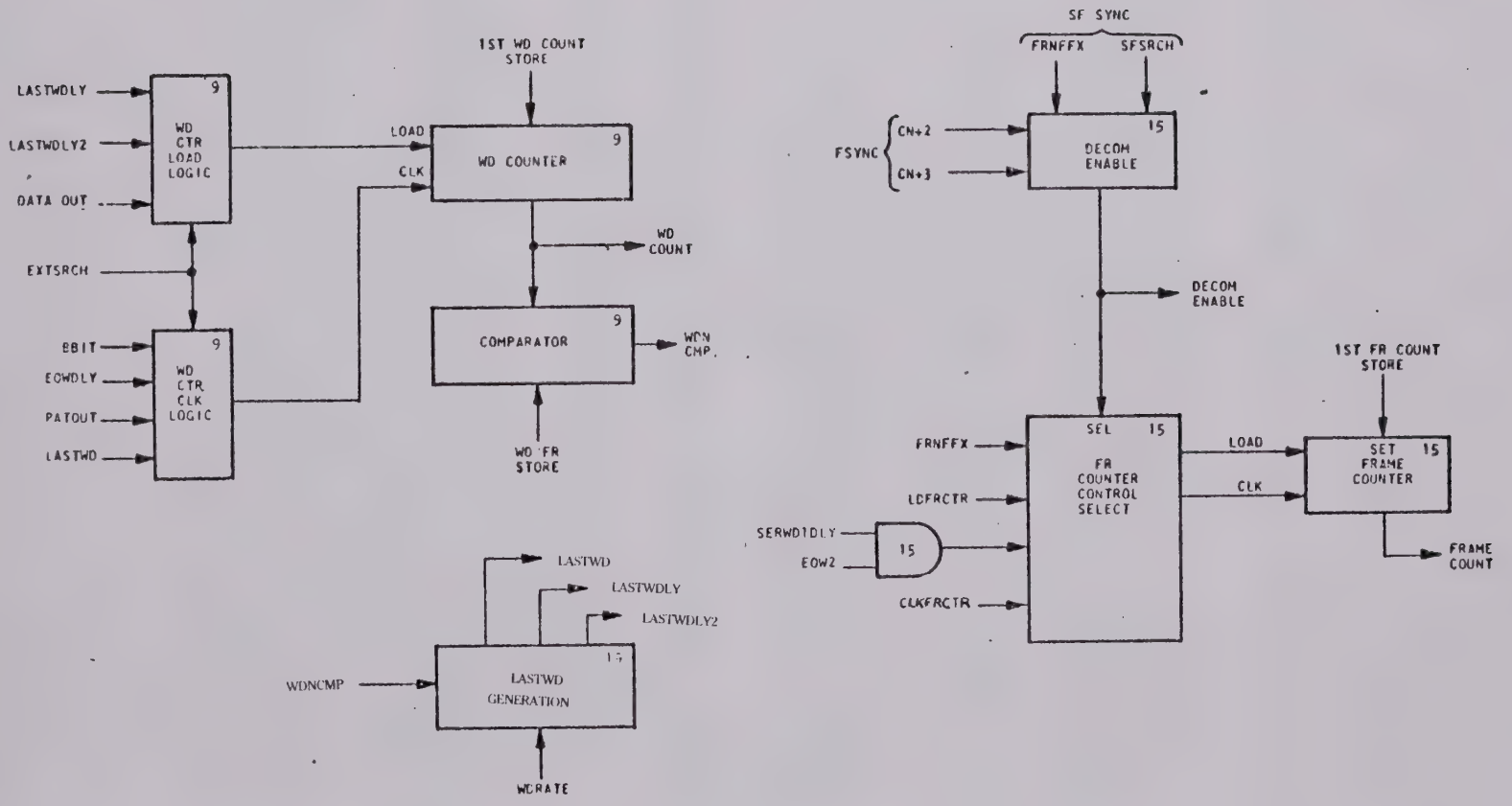


Figure 4-21 Word /Frame and Frame / Subframe Counters Functional Block Diagram

selects LDFRCTR and CLKFRCTR to load and clock the frame counter. These signals synchronize the frame counter with the frame counter on the subframe synchronizer. When the subframe synchronizer advances to verify mode, DECOM ENABLE goes to a ONE level. The load and clock pulses for the counter are now switched to FRNFFX and SERWD1DLY·EOW2. The reason for this switch is because the subframe synchronizer frame counter is required to increment in phase with the incoming data contained in the frame synchronizer main shift register and the parallel data output actually occurs one word time later. FRNFFX and SERWD1DLY·EOW2 will align the frame counter increment and load with presentation of word one of the frame on the output data lines.

4.3.6 Display Strobe Generation (Figure 4-22)

The 710 can display any word in the format including supercommutated and subcommutated words. When a word is to be displayed without regard to subcommutation or supercommutation, the word number is entered into the front panel display from the keyboard. This causes the word number to be entered into the word location stores. The frame and interval displays must remain blanked. When the word counter reaches the stored value WD LOC COMP (word location compare) is generated. Two bit periods after data is on the output lines WD STROBE is generated by the trailing edge of word rate. It is reset by the subsequent M BIT. The strobe updates the displayed data on the front panel.

Display of subcommutated data is accomplished by entering a frame number and a word number. The frame location stores are compared with the frame count to generate FR LOC COMP (frame location compare). The coincidence of this signal and WD LOC COMP is necessary to generate a display strobe.

Interval is used when displaying supercommutated data. In the case of strapping on the main frame, the word number of the first strapped word and the interval between strapped words are entered on the display and the frame number is loaded with blanks. The WD LOC COMP is generated as before and produces the first display strobe. At this time, the word interval counter is loaded and decrements to zero with a word rate clock. The zero count is detected by the strobe control logic and a display strobe is generated. This strobe again loads the interval counter which then decrements to zero. This cycle continues to the end of the frame, at which time the word interval counter is inhibited by EXTSTRTFR (frame rate) until occurrence of WD LOC COMP. In this manner, the display receives multiple updates during a frame period.

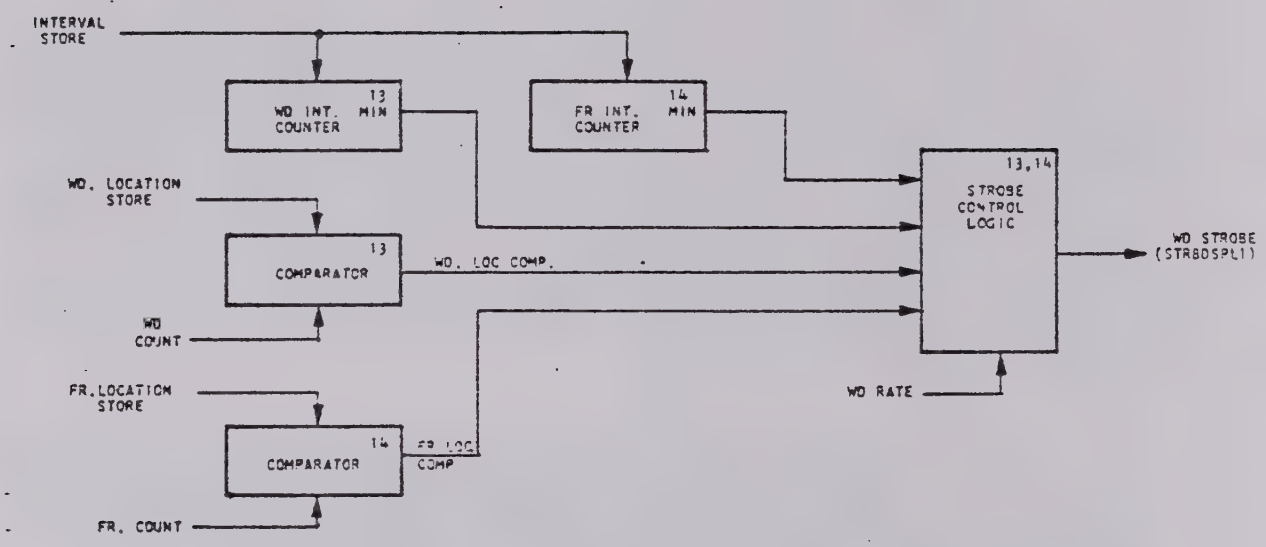


Figure 4-22. Display Strobe Generator Functional Block Diagram

In the case of strapping on the subframe, the word, frame and interval are programmed. The interval now applies to frame, not word. WD LOC COMP and FR LOC COMP are generated as before and produce the first display strobe. The frame interval counter is loaded by this first strobe and decrements to zero with a frame rate clock (the word interval counter is also loaded and decremented but its output is ignored). The frame interval zero count is detected, a display strobe is generated and the counter is loaded again. This cycle continues to the end of the subframe, at which time the frame interval counter is inhibited by FRNFFX unt FR LOC COMP is again generated.

4.3.7 Word Select Keyboard Control and Display Word, Frame, Interval Enable and Store (Figure 4-23)

In the word select mode, the word, frame and interval location are programmed into the display from the front panel keyboard. The counter control logic, binary counter and binary-to-12 line decoder determine the specific display digit affected by the keyboard entry. There are 12 display digits; four each for word, frame and interval. Each time a key is depressed, the number is entered into the enabled store and the subsequent keystrobe pulse increments the binary counter (unless FREEZE = 1). The binary count is decoded to enable one of 12 output lines. Each of these lines controls a store position and drives the corresponding cursor on the display. The display cursor indicates to the operator which digit he will change when a key is depressed. As the binary counter increments the cursor moves from left to right enabling the word ten thousand, thousand, hundred, and unit positions, then the corresponding positions of frame and interval. When the cursor is on the final interval position (units), the counter control logic generates a reset to the counter with the next keystrobe and the cursor moves to the extreme left position (word - ten thousand).

The CURSRITE (→) and CURSLEFT (←) controls on the front panel provide a means of moving the cursor without affecting the stores. CURSRITE clocks the counter up and CURSLEFT clocks it down.

KEYSTROBE and KEYDATA come from the local program logic on the frame sync card. When the display is in word select mode and a key is depressed, KEYDATA (a BCD representation of the number) is presented to the word, frame and interval stores. Following a delay during which the data lines settle, KEYSTROBE generates the WD SEL STROBE (word select). The data is entered into the enabled store position only. The store outputs drive the upper display.

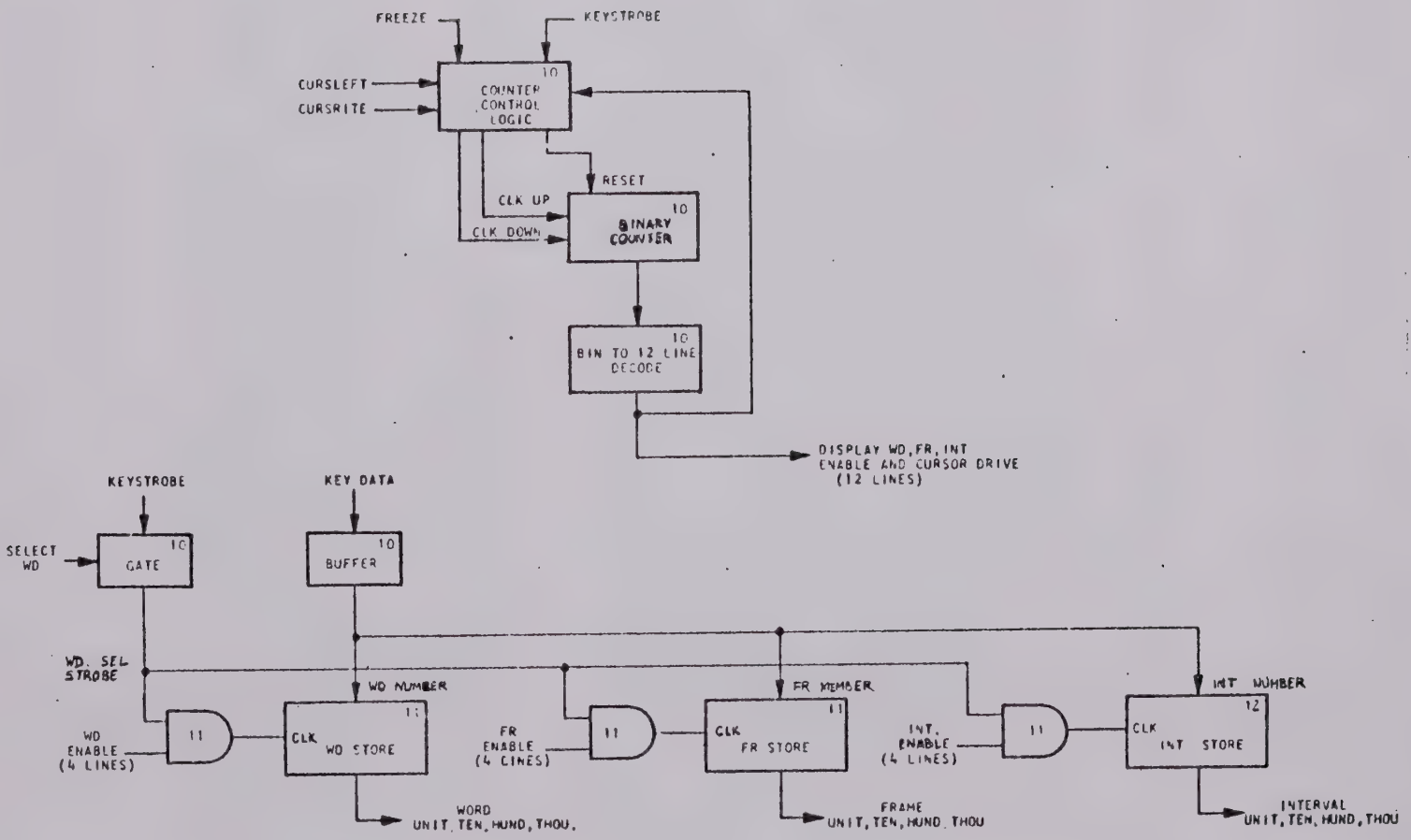


Figure 4-23. Word Select Keyboard Control and Display Word, Frame, Interval Enable and Store Functional Block Diagram

4.3.8 Upper/Lower Display Drive Select (Figure 4-24)

The front panel display serves two purposes. In program mode, it is used to monitor or change the programmable system parameters. In the word select mode, it is used to examine the data content of a specific word in the format. The display drive select logic controls the application of the various stores to the display.

The upper display is relatively simple. In the program mode, the module and function entered from the keyboard are displayed. Also, the present content of the selected module and function store is displayed. In the word select mode, the word, frame and interval store outputs are displayed. The upper display contains 15 seven-segment LED displays (number 12 position not required). Note that only those positions that are shared by the two display modes need be routed through the word/program selector. The remainder can drive the display directly. For example, display 11 represents the tens position of function address and is not used in word select mode. When the display is in the word select mode, display 11 is blanked off by the word/program select line.

The lower display indicates the selected data word content in 5-digit BCD or up to 16-digit binary when in the word select mode. In the program mode, the first eight positions are used to set up the parameters to be entered into the selected module and function.

LSB aligned data (binary) from the transposer logic is routed directly to a data selector. It is also converted to BCD and applied to the second input to the data selector. The front panel switch binary/BCD selects the data for input to the word data store. The data at this point is parallel multiplexed data identical to the output data. WD STROBE enters selected word data into the word data store. The store output goes through a second data selector which routes it to the correct display digit depending whether binary or BCD data was selected. For example, if binary data were selected, bits 1 through 4 from the word data store would drive display digits 1 through 4. However, if BCD data were selected, these same data lines represent 1, 2, 4, 8 of the least significant digit and would be routed to display digit one.

The binary/BCD data for the first five display digits goes to a data/program selector which drives the display with data or local program bits 1 through 5 from the frame sync card. Binary data bits 6 through 8 go to a data/program selector which drives display digits 6 through 8 with binary data, or local program bits 6 through 8 from the frame sync card. Binary data bits 9 through 16 drive display digits 9 through 16 directly.

When displaying binary data words of less than 16 bits, it is desirable to suppress unused bits. This is accomplished by strobing the programmed word length (alternate, common, or variable) into a store and decoding it to blank leading data bits at the same time the data is strobed into the word data store.

When programmed for data and status output, a count of 16 is forced into the word length store during the status word output time. This inhibits suppression of leading zeros during display of the status word.

When displaying BCD data, it is desirable to suppress leading zeros. The 7 segment decoders provide the necessary signals. For example, if the data input to display digit 5 were a zero, the digit would be blanked out and a signal RB05 (ripple blank output 5) is routed through the blank select circuit to display digit 4. If the data input to display digit 4 is also a zero, digit 4 will be blanked and RB04 which is routed to display digit 3 will be set. This blanking signal ripples down to the first digit which is not a zero, at which time, it stops. Display digit one is never blanked.

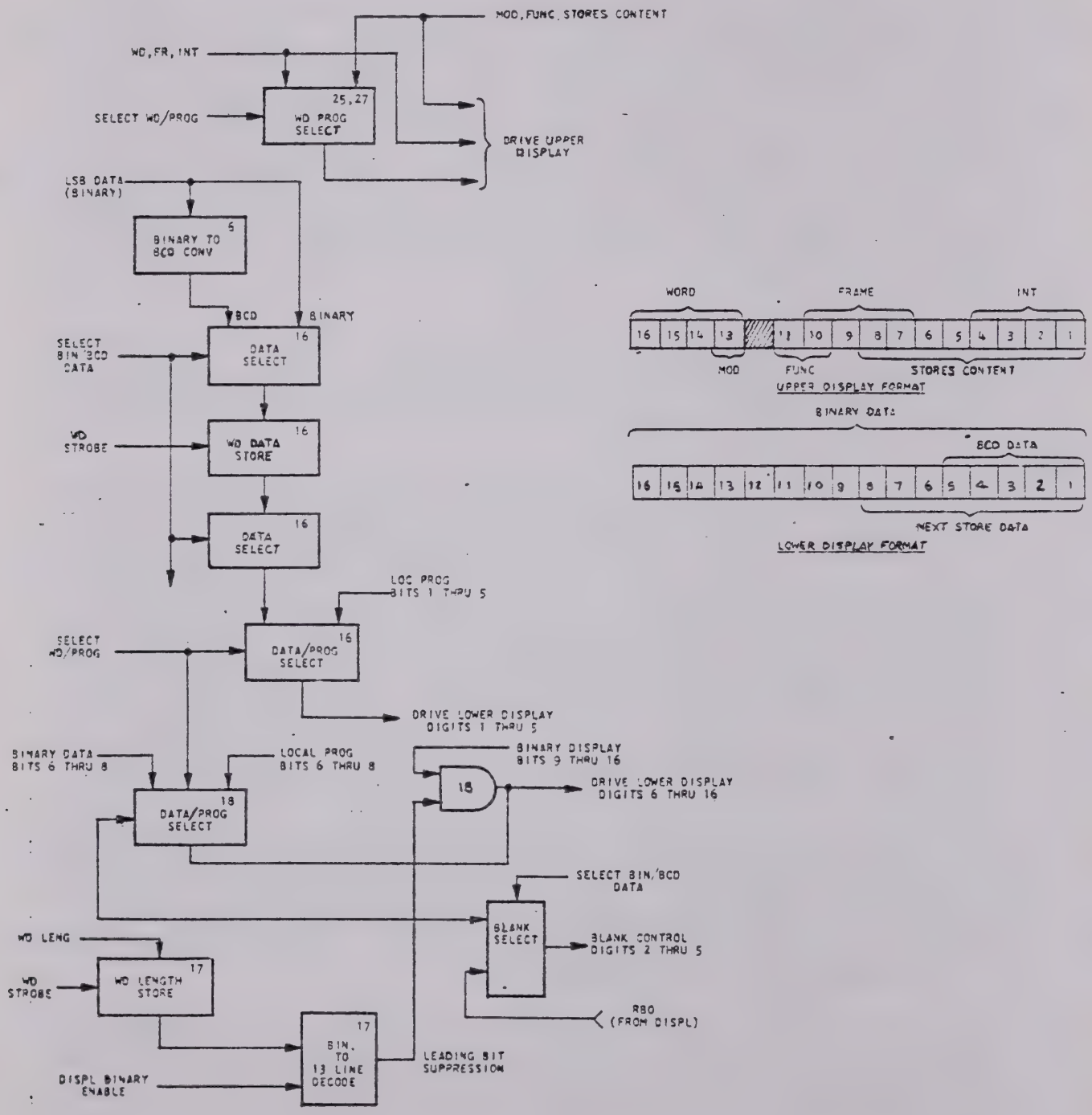


Figure 4-24. Upper/Lower Display Drive Select Functional Block Diagram

4.3.9 Parity Control Circuits (Figure 4-24A)

The purpose of the logic is to monitor the input data format for parity errors. The 710 can output data words up to 16 bits. If the data word is 16 bits, parity must be stripped from the output word format. For any other data word length the parity bit may or may not be stripped (programmable) from the output and parity may be first or last, odd or even. In either case a separate output line will provide a one level if a parity error is detected for the word being output or a zero level if no parity error is detected. If parity is not being received with the input format, a parity bit is generated (programmable odd or even) for each data word and the above output line will contain the appropriate level according to the value of the output data word.

The parity check/generate logic consists primarily of two flip-flop stages. The first stage is triggered on and off sequentially by "1" bits in the (serial) MSR6 input. The load output store pulse (LDOUTSTD) generated at the end of each data word transfers the state (1 or 0) of the first stage to the second and resets the first stage to zero. The condition of the second stage is compared with the programmed odd/even input to generate the appropriate parity output (Parity Generate Mode) or error indication (Parity Check Mode). Since the frame sync word does not contain parity, the parity logic is inhibited during this time. The WDNCMP level (last data word compare) produces the FSWDTIME (frame sync word time) inhibit levels. The inhibit levels are removed by CN+2 (end of frame sync word) thereby reactivating the parity logic for the first data word of the next frame.

When parity is the first bit transmitted and is to be stripped from the format the MCLK pulse to the serial-to-parallel converter and the transposer is inhibited during bit one time of each word by FBT·E0W2. This inhibits the parity bit from being read into the serial shift register. The parity bit is stripped from the transposer by delaying the STRTXPOS input, which loads a "1" into the shift one register, until bit two time by FBT·E0WDLY2. If parity is the last bit transmitted and is to be stripped, the transposer is enabled at the start of the data word by STRTXPOS generated from $\overline{\text{FBT}}$·E0WDLY. The MCLK pulse is inhibited during the last bit of the word by $\overline{\text{FBT}}$·E0W. During frame sync word time SETXPOS overrides STRTXPOS so that the transposer is enabled at the beginning of each word period and the frame sync word time level (FSWDTIME) enables the generation of MCLK pulses for the full word period.

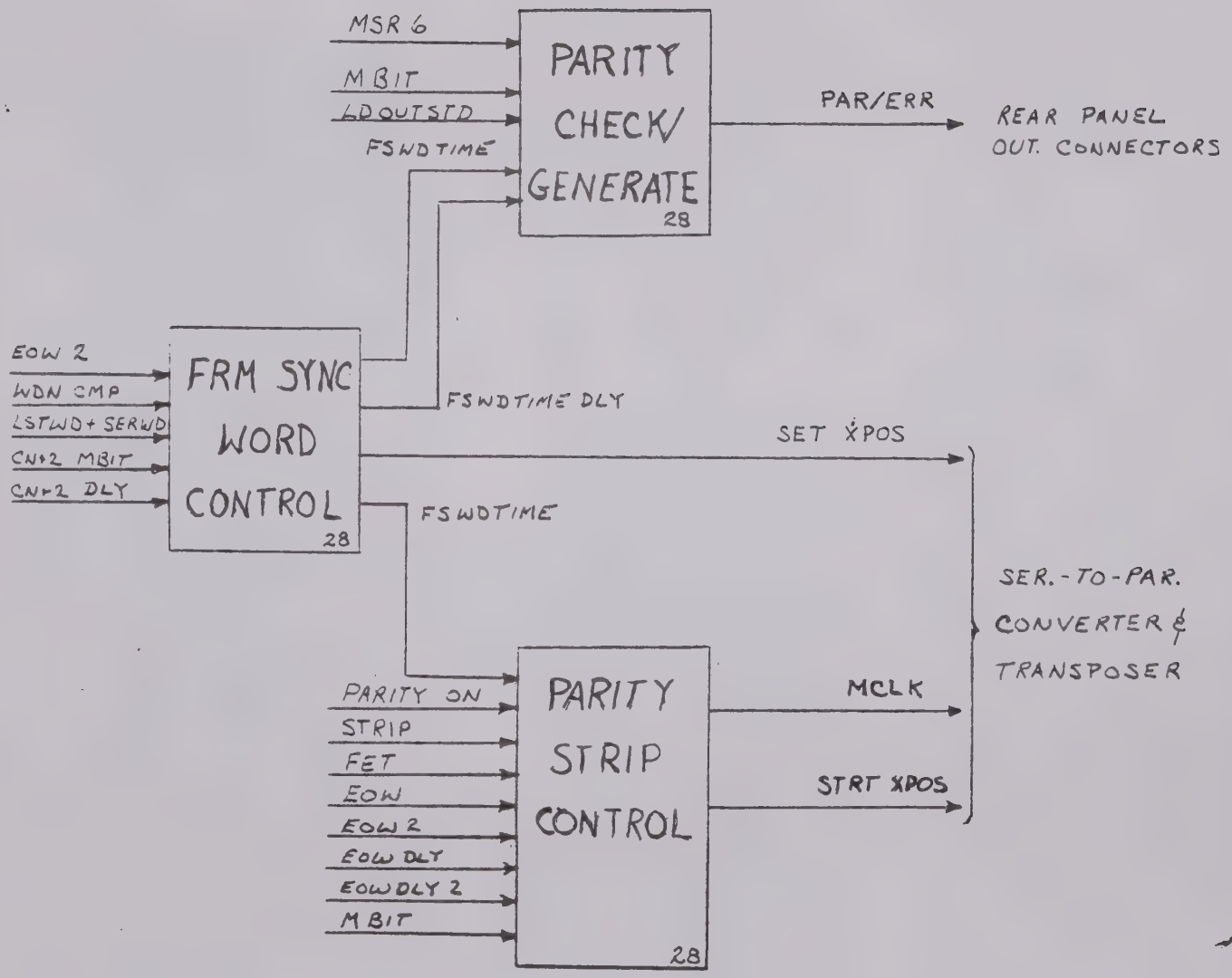


Figure 4-24 A. Parity Control Circuits.

4.4 DATA ENTRY CARD (FIGURE 4-25)

The Data Entry Card provides interfaces for a computer and a card reader with the common setup bus. The computer interface function contains the circuits by which computer programmed setup parameters may be automatically verified. Parallel data outputs are routed to the computer via the computer interface function. The following paragraphs describe the individual functional circuits of the Data Entry Card.

Note

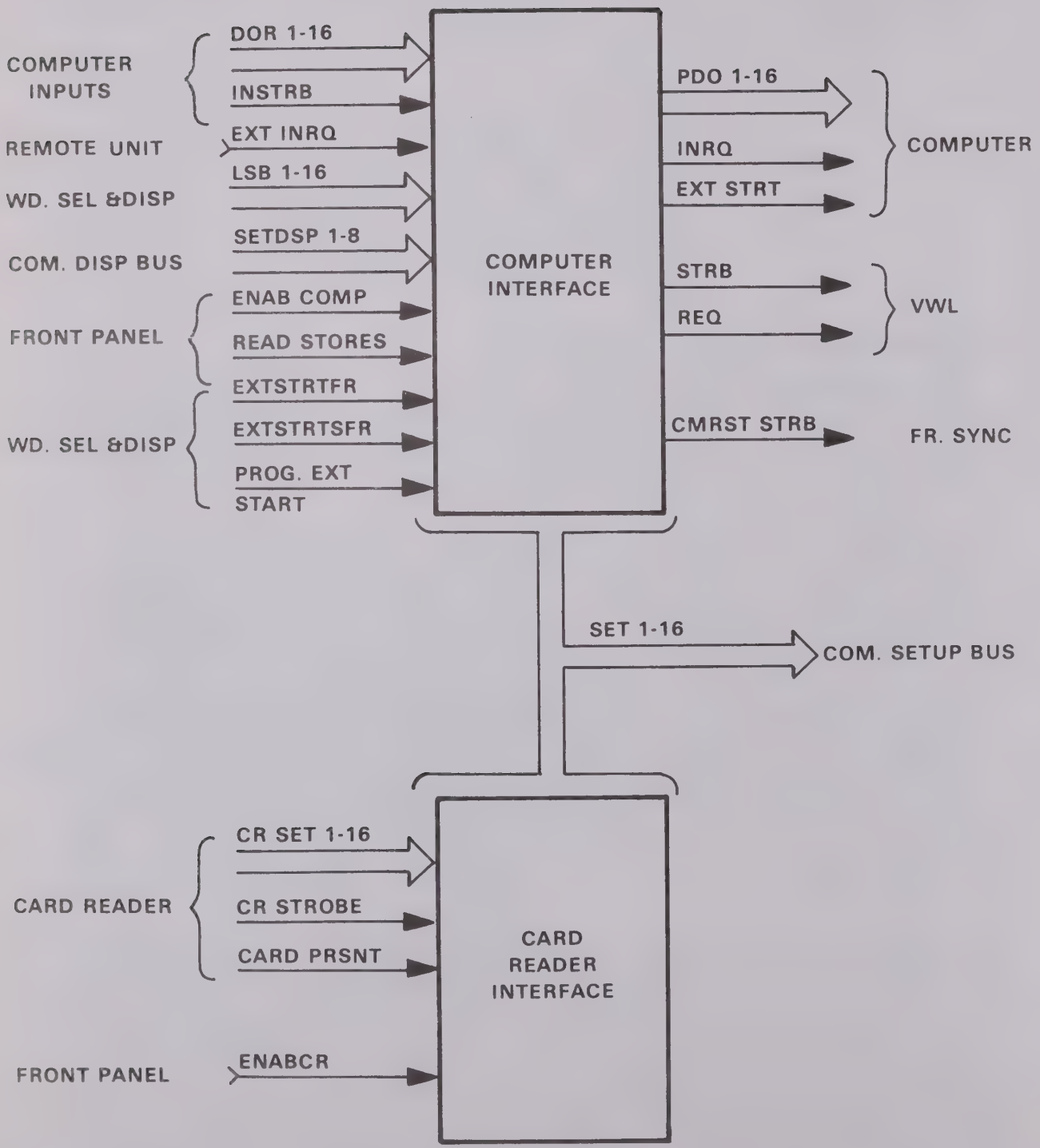
The numbers within symbols and blocks of the individual circuit diagrams refer to the sheet number of the Data Entry Card schematic diagram (Section 6 - Drawing No. 34309) where that particular function is located.

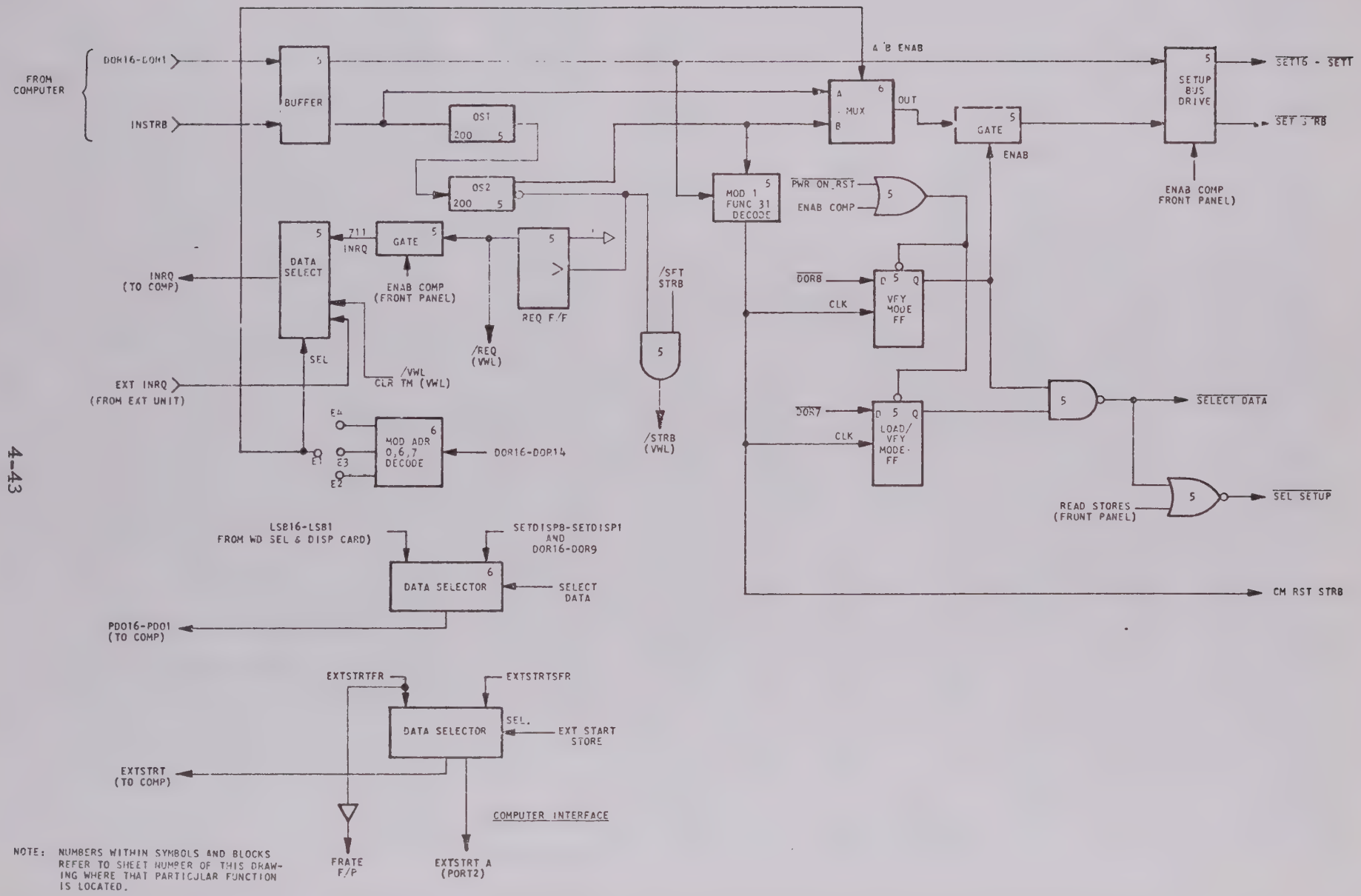
4.4.1 Computer Interface (Figure 4-26)

This logic provides an interface with the computer via the EMR 2763 Buffered Data Channel. The interface can be operated in several modes. The computer can simply load the 710 stores or it can examine the stores (verify mode) or it can load and examine the stores (load/verify mode).

When loading the 710 stores (or external unit connected to the setup bus), Parallel data DOR 16-DOR1 followed by INSTRB is presented to the interface when INRQ (input request) is high. The data is buffered and placed on the 710 setup bus when the computer mode is selected on the front panel controls. The INSTRB pulse is applied to the Request flip-flop, a one-shot multivibrator circuit, and a gating circuit. The INSTRB triggers the flip-flop causing the INRQ level to go low. The delay strobe output of the one-shot circuit resets the Request flip-flop allowing the INRQ input to the computer to go high thereby enabling the next data transfer. The one-shot delay allows the 710 memory devices to stabilize between transfers of data. INRQ comes from the 710, if 710 stores are being addressed (modules 0 through 5). If Modules 6 or 7 are addressed, INRQ is controlled by the external input request from the respective unit. Also, when modules 0 through 8 are addressed the delayed strobe is gated to the setup bus. When module addresses 6 or 7 are decoded the INSTRB from the computer is gated to the bus.

The computer places the interface in the verify mode by addressing Module 1 function 31 and placing a ONE on DOR8. INSTRB will clock the VFY MODE FF output to ZERO level. This disables the SETSTRB line on the setup bus, selects the display bus for reading back to the computer and causes SELSETUP to go low. The addressable memory stores located on the simulator and subframe cards are normally sequencing through four locations and cannot be read. SELSETUP replaces the clocking address for these stores with the setup bus address (SET 13 through SET 9). Without regard to INRQ or INSTRB, the computer can now place a module and function address on the DOR 16 through DOR 9


COMPUTER INPUTS
DOR 1-16
INSTRB
REMOTE UNIT
EXT INRQ
WD. SEL &DISP
LSB 1-16
COM. DISP BUS
SETDSP 1-8
FRONT PANEL
ENAB COMP
READ STORES
WD. SEL &DISP
EXTSTRTFR
EXTSTRTSFR
PROG. EXT START
COMPUTER INTERFACE
PDO 1-16
INRQ
EXT STRT
COMPUTER
STRB
REQ
VWL
CMRST STRB
FR. SYNC
SET 1-16
COM. SETUP BUS
CARD READER
CR SET 1-16
CR STROBE
CARD PRSNT
CARD READER INTERFACE
FRONT PANEL
ENABCR



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

Figure 4-26. Computer Interface Functional Block Diagram.

input lines and the selected module/function store outputs are placed on the PD08-PD01 data lines to the computer. In addition, the module and function address are read back to the computer on the PDO16-PDO9 data lines to the computer. The computer can terminate the verify mode by again addressing module 1 function 31, placing a ZERO on DOR8, and generating INSTRB.

The computer can place the interface in the load/verify mode by addressing Module 1, function 31 and placing a ONE on PD07. INSTRB will clock the LOAD/VFY MODE FF output to ZERO selecting the display bus for output to the computer and placing the 710 addressable memory stores under setup bus control. However, the SETSTRB gate remains enabled and the computer can now load stores and examine them. This mode is terminated by addressing Module 1, function 31, placing a zero on DOR7 and generating INSTRB.

The clock to the verify and load verify flip flops is brought out as CMRSTSTRB (computer reset strobe). It is used to generate a simulator and frame sync reset.

The external start stores select the frame or subframe rate pulse for an external start to the EMR 2763.

4.4.2 Card Reader Interface (Figure 4-27)

The card reader presents eight parallel data lines; $\overline{\text{CRDATA 1-8}}$, a strobe - $\overline{\text{CRSTROBE}}$ and $\overline{\text{CARDPRSNT}}$ (card present) to the 710. These inputs must be interfaced to the 16-bit setup bus which controls all modules within the 710 and any external units connected to the setup bus.

The format which the card reader presents to the interface is first, the number of instructions, (functions) which will be presented and the module address and, second, the address of the first instruction and finally the instructions themselves in sequential order. A maximum of 32 instructions can be loaded into each module and a $\overline{\text{CRSTROBE}}$ is presented with each instruction.

Control of the various stores, counters, strobes, etc., is maintained by the control counter which is incremented from 00 to 11 with the first few $\overline{\text{CRSTROBE}}$'s. The counter then remains at 11 until all instructions on the card have been entered. Termination of $\overline{\text{CARDPRST}}$ generates a latched reset to the control counter, returning CNTRCNT to 00, and the instruction counter. The set strobe control flip flop is also reset at this time. The Motor Inhibit Clamp ensures that the card reader motor turns off when no card is present.

When $\overline{\text{CARDPRST}}$ goes low, the resets to the control counter, instruction counter and set strobe control flip flop are removed. Following presentation of the module address on CRDATA 1-3 and the max instructions on CRDATA 4-8 a $\overline{\text{CRSTROBE}}$ occurs. The trailing edge generates CRSTRBDLY which loads the max instruction and module stores through the DECODE-00 gate. The trailing edge of CRSTRBDLY clocks the control counter output to 01 and further clocks to these stores are inhibited. Note that the function stores

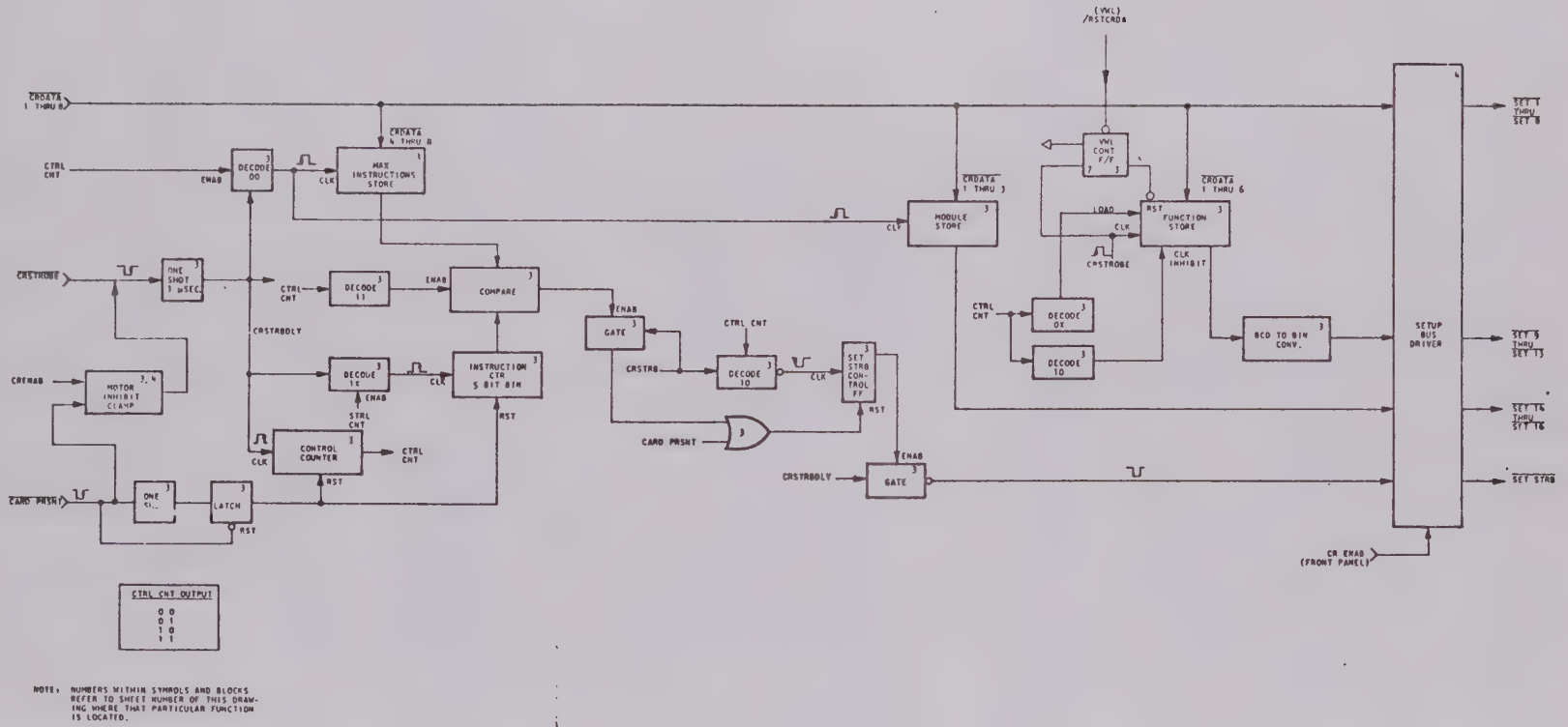


Figure 4-27. Card Reader Interface Functional Block Diagram

were loaded by CRSTROBE. This particular entry into the function store is meaningless and will be corrected by a subsequent load prior to actually using the function store output.

The address of the first instruction is now placed on CRDATA 1-6 and the leading edge of CRSTROBE will enter this address into the function store because the load input to this store is active. The trailing edge of CRSTRBDLY now increments the control counter output to 10 enabling the instruction counter clock and set strobe control flip flop clock. It also disables the clock and load of the function store. The first instruction is now placed on CRDATA 1-8. The leading edge of the next CRSTROBE clocks the set strobe control flip flop and enables the SETSTRB gate. CRSTRBDLY now generates SETSTRB which enters the instruction on SET 1-8 into the addressed function and module on SET 9-16. The trailing edge of CRSTRBDLY increments the control counter to 11 and also increments the instruction counter. The 11 output of the control counter removes the clock inhibit from the function store and enables the instruction comparator. At this point the control counter remains at 11 regardless of further strobes until it is reset to 00 by the trailing edge of CARDPRST.

The second instruction is now placed on CRDATA 1-8. The leading edge of the next CRSTROBE increments the function store to the address of the second instruction, CRSTRBDLY generates SETSTRB and the trailing edge of CRSTRBDLY increments the instruction counter. This sequence continues until the instruction counter reaches the maximum instruction store value and enables the set strobe control flip flop reset gate. The next CRSTRB will reset the flip flop which inhibits further SETSTRB's. Although additional CRSTROBE's occur after this they have no effect on the 710 stores. After the card reader CARDPRST returns to a ONE level and resets the control counter and instruction counter.

When loading a variable word length program the Variable Word Length Card generates a reset card reader pulse (RSTCRDA) each time the function store is incremented to 10. This pulse resets the function store to 00 which is then incremented thru 10 when another reset pulse is generated. This feature allows up to ten variable word programs to be loaded from one programming card.

4.5 SUBFRAME SYNCHRONIZERS (FIGURE 4-28)

The 710 can optionally include one or two completely independent subframe synchronizers. The synchronizers are logically identical except for the module address used to enable the parameter stores. Both synchronizers are contained on one card. Each synchronizer can be programmed to operate in any one of three modes. The FCC mode provides for recognition of a complemented frame synchronized pattern to indicate the end of a subframe. The URC mode recognizes a unique pattern of four to 32 contiguous bits, of up to four segments of from two to 15 bits to indicate the end of the subframe. The SFID mode recognizes an incrementing or decrementing binary count of from two to 512 in up to nine contiguous bits, either LSB or MSB first. All subframe synchronizers have a sync strategy (Search, Verify, Lock and Check) similar to the frame synchronizer.

The following paragraphs describing the operation of functional circuits of Subframe Synchronizer Card are applicable to both synchronizers.

Note

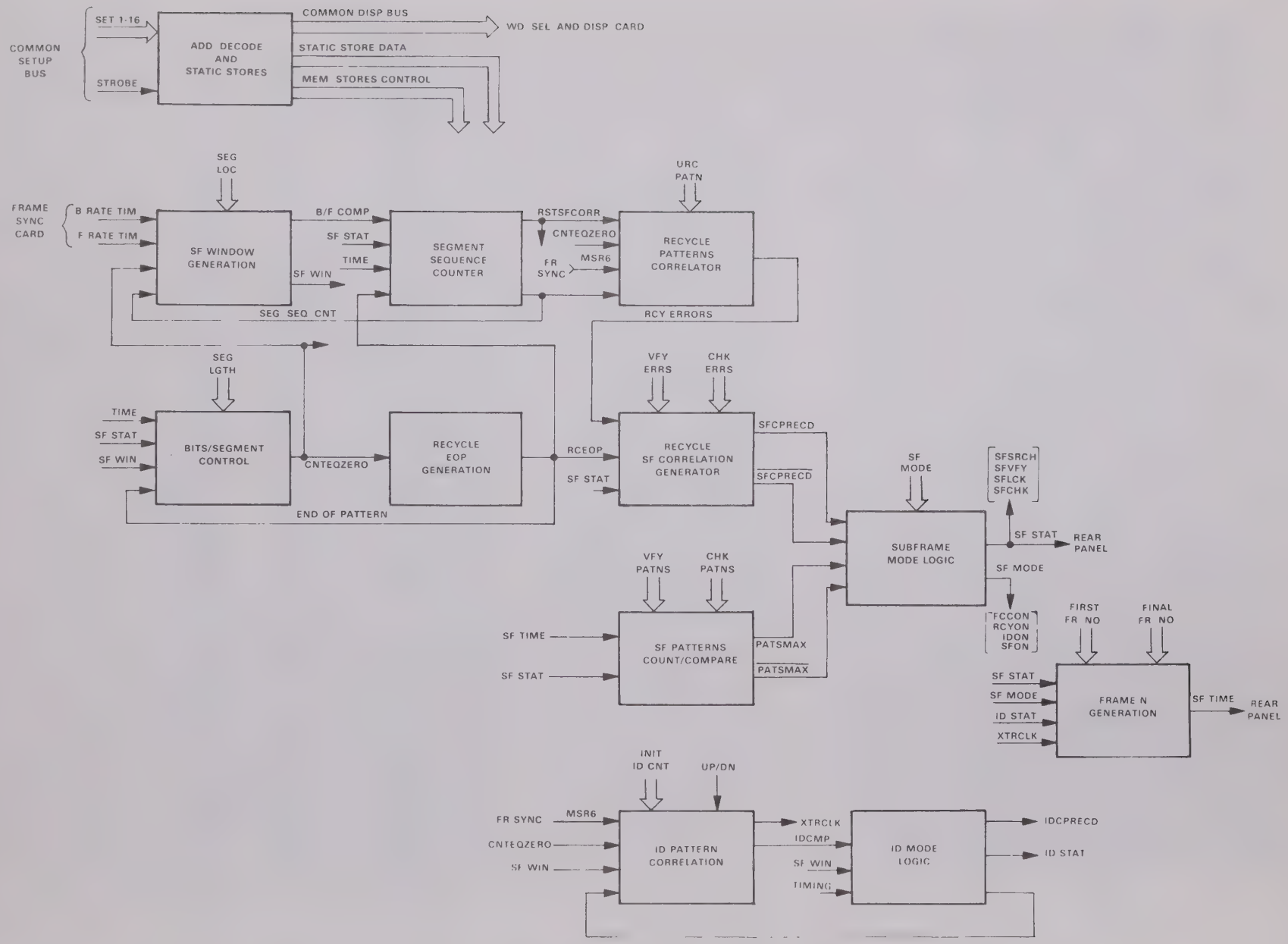
The numbers in symbols and blocks of the individual circuit diagrams refer to the sheet number the Subframe Synchronizer Card schematic diagram (Section 6-Drawing No. 34599) where that particular function for SF1 is located. The sheet number for SF2 a second identical subframe synchronizer can be found by adding 12 to these numbers.

4.5.1 Address Decoder, Data Buffers, and Static Stores (Figure 4-29)

$\overline{\text{SET 16}}$ through $\overline{\text{SET9}}$ are decoded to provide six static store addresses; SFADRO-SFADR3, SFADR8, SFADR9 and four memory enable addresses, MEMLOAD 4-7, 16-19, 20-23, 24-27. $\overline{\text{SET8}}$ through $\overline{\text{SET1}}$ are buffered and applied to all stores.

There are six static stores. The address decoder enables one of the six. $\overline{\text{SFSTRB}}$ loads the enabled store with the data on SETSF8-SETSF1 when the $\overline{\text{SETSTRB}}$ line goes low.

The decoded address also enables the display bus driver associated with the load store to display the store content.


COMMON SETUP BUS
SET 1-16
STROBE
ADD DECODE AND STATIC STORES
COMMON DISP BUS
WD SEL AND DISP CARD
STATIC STORE DATA
MEM STORES CONTROL
SEG LOC
FRAME SYNC CARD
B RATE TIM
F RATE TIM
SF WINDOW GENERATION
B/F COMP
SF STAT
TIME
SF WIN
SEGMENT SEQUENCE COUNTER
RSTSFCORR
CNTEQZERO
FR SYNC
MSR6
URC PATN
RECYCLE PATTERNS CORRELATOR
SEG SEQ CNT
RCY ERRORS
SEG LGTH
TIME
SF STAT
SF WIN
BITS/SEGMENT CONTROL
CNTEQZERO
RECYCLE EOP GENERATION
END OF PATTERN
VFY ERRS
CHK ERRS
RCEOP
SF STAT
RECYCLE SF CORRELATION GENERATOR
SFCPRECD
SFCPRECD
SF MODE
SFSRCH
SFVFY
SFLCK
SFCHK
SUBFRAME MODE LOGIC
SF STAT
REAR PANEL
SF MODE
VFY PATNS
CHK PATNS
SF TIME
SF STAT
SF PATTERNS COUNT/COMPARE
PATSMAX
PATSMAX
FCCON
RCYON
IDON
SFON
FIRST FR NO
FINAL FR NO
SF STAT
SF MODE
ID STAT
XTRCLK
FRAME N GENERATION
SF TIME
REAR PANEL
INIT ID CNT
UP/DN
FR SYNC
MSR6
CNTEQZERO
SF WIN
ID PATTERN CORRELATION
XTRCLK
IDCMP
SF WIN
TIMING
ID MODE LOGIC
IDCPRECD
ID STAT

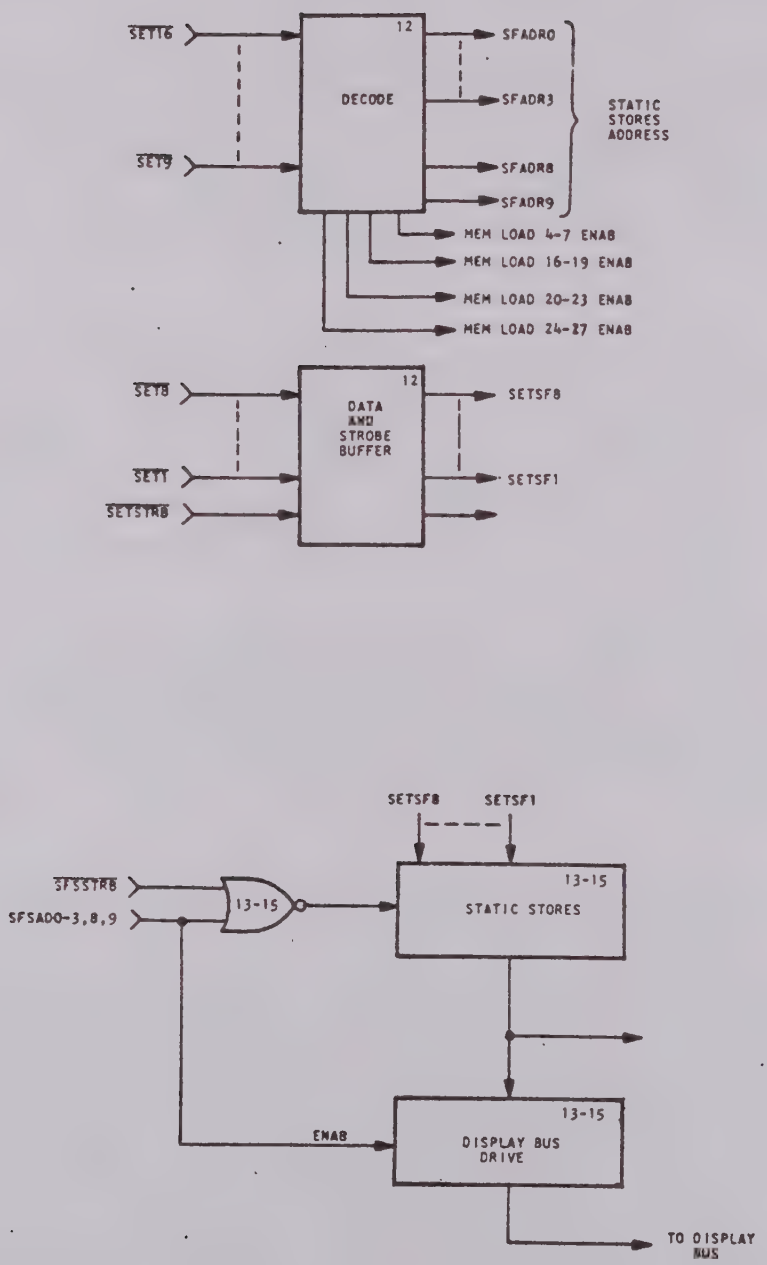


Figure 4-29. Address Decoder, Data Buffer and Static Stores Functional Block Diagram

4.5.2 Subframe Window Generation (Figure 4-30)

When operating in the URC (unique recycle code), a subframe window is opened each frame. In fact, the subframe sync pattern can be divided into as many as four segments located anywhere within the frame and the subframe window is then opened several times each frame.

The pattern segment location memory is a 16 bit x 4 word store which contains the first bit location within a frame of each pattern segment. The store is loaded from the SF SETUP bus when memory load addresses 16 through 23 are decoded. When the front-panel switch READ STORE is depressed, or when the computer is examining stores (in computer mode only), the load address is also used as the read address and the store contents are placed on the display bus.

Normally, the SEQ CNT 1-2, a two bit counter output, controls the read address. It places the first pattern segment location on the memory output. The bit per frame counter output is compared with this location and generates BF COMP (bit/frame compare) which is one bit time wide. At M BIT (mid bit time) the SF window FF is set producing SF WIN (subframe window). This window remains set until CNT EQ ZERO (count equal zero) from the bits/segment logic occurs. One-half bit time after SF WIN occurs, SF WIN DLY (subframe window delay) is set.

BF COMP increments the sequence counter and therefore the memory read address, placing the 2nd segment location on the comparator input. When the bits/frame counter reaches this number another BF COMP and corresponding SF WIN will be generated. In this manner, as many as four pattern segment locations are detected and corresponding SF windows are generated each frame period.

4.5.3 Segment Sequence Counter (Figure 4-31)

This is a two-bit counter which controls the pattern segment location memory output and the segment length memory output. It increments the read addresses of these stores from 00, corresponding to segment one location and length, through 11 which addresses segment four location and length. It can be reset by several signals. $\overline{CN+2}$, a timing line from the frame sync initializes the counter following frame synchronization. $\overline{RCEOP}$ (recycle end of pattern) occurs following the final segment location which was programmed. Note that the final segment is not necessarily the fourth segment. For example, a subframe sync pattern comprised of 15 or less adjacent bits requires that only the first segment be programmed. When the subframe synchronizer is in ID mode, a hard reset on the sequence counter holds the counter output at 00 and prevents counting. The first segment location address is now used as the first bit location of the ID pattern and the first segment length address is used as the ID pattern length.

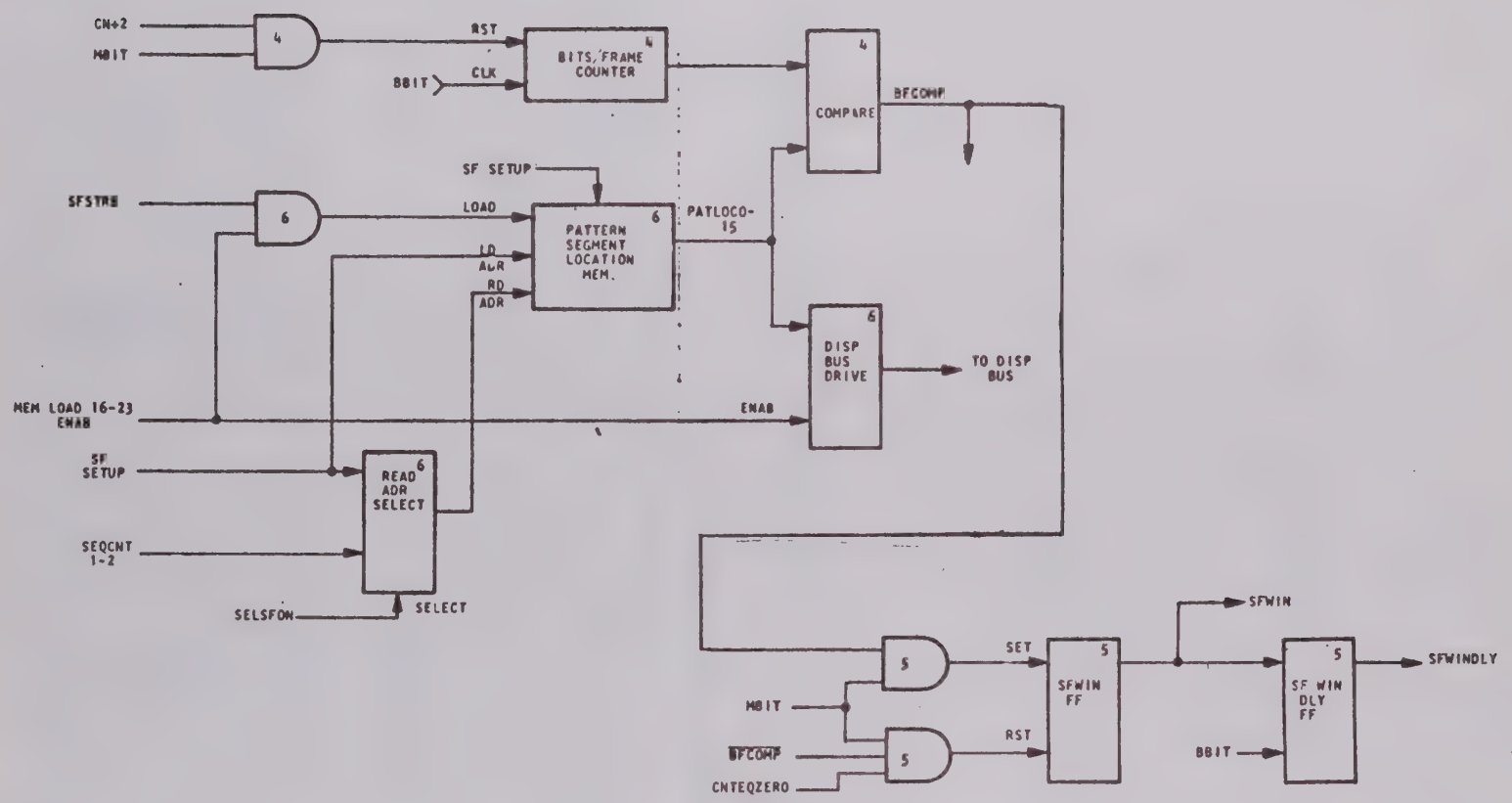


Figure 4-30. Subframe Window Generation Functional Block Diagram

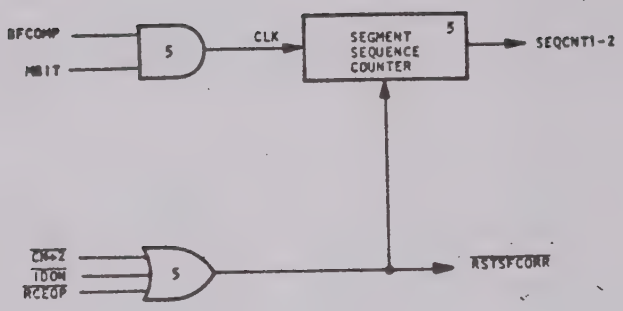


Figure 4-31. Segment Sequence Counter Functional Block Diagram

4.5.4 Bits/Segment Control (Figure 4-32)

This circuit controls the width of the SF window. The segment length memory contains four 4-bit words representing the number of bits in each pattern segment. It is loaded from the subframe setup lines by the SFSTRB when the memory load enable 24-27 is active. The read address, SEGLNG 1 - 2 (segment length 1 and 2), comes from the SFSETUP lines when READ STORES switch is depressed (or computer is examining stores), or from the sequence counter output (SEQ CNT 1-2) when operating. When memory load enable 24-27 is active (in program mode and stores 24-27 are addressed), the memory output drives the display.

A bits/segment counter which has been loaded with the segment length begins decrementing when SF WIN occurs. When the output - CNTEQZERO (count equal zero) reaches zero SF WIN is reset. At this time the next segment length has already been placed on the bits/seg counter input and a load pulse now enters this value into the counter. The load pulse can be generated by several signals. CN+2 · MBIT provides initialization following frame synchronization. RCEOP insures that the first segment length is loaded following reset of the sequence counter to first segment address. $\overline{\text{SFWIN}}$ · SFWINDLY loads the subsequent segment length into the counter when the previous segment window terminates. In the case of a segment occurring immediately after

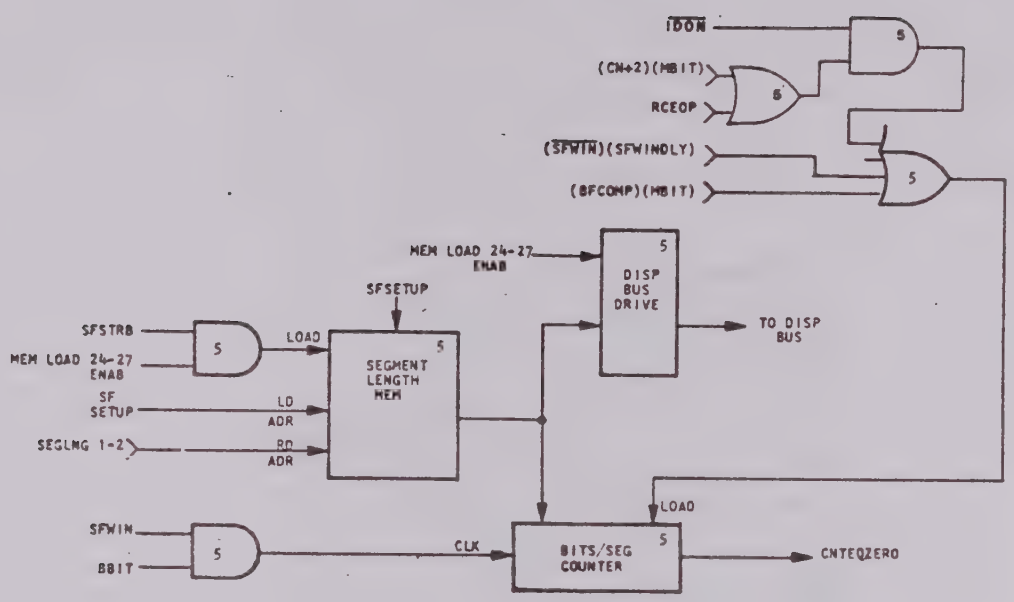


Figure 4-32. Bits/Segment Control Functional Block Diagram

another segment, SFWIN does not terminate but is held through the adjacent segment, thus, SFWIN · SFWINDLY will not occur to load the bit/seg counter. SFWINDLY·BFCOMP·MBIT loads the counter in this situation.

4.5.5 Recycle EOP Generation (Figure 4-33)

RECEOP indicates the final pattern segment has terminated and several counters can be reset or loaded in preparation for the subsequent frame. It also generates the RCYCPRECD (recycle correlation pulse received) pulse assuring pattern bit error criteria has been met.

There are two situations to consider when generating RCEOP. The first is when less than four pattern segments are used. In this case, termination of SFWIN of the final segment loads ZERO into the bit/segment counter (see Bit/seg Control discussion) since the subsequent, unused segment lengths were programmed to ZERO. CNTEQZERO therefore remains at a ONE level and RCEOP is generated by the following B BIT and terminated by M BIT. In the second situation, all four segments are used. Therefore, the bits/segment counter is never loaded with ZERO and CNTEQZERO will terminate before B BIT can set the RCEOP. In this case the max segment count is detected and generates RCEOP. When the BFCOMP for segment three occurs it clocks the sequence counter to segment four address (11). This address is decoded and when BFCOMP for segment four occurs, SEQCNTMAX is set

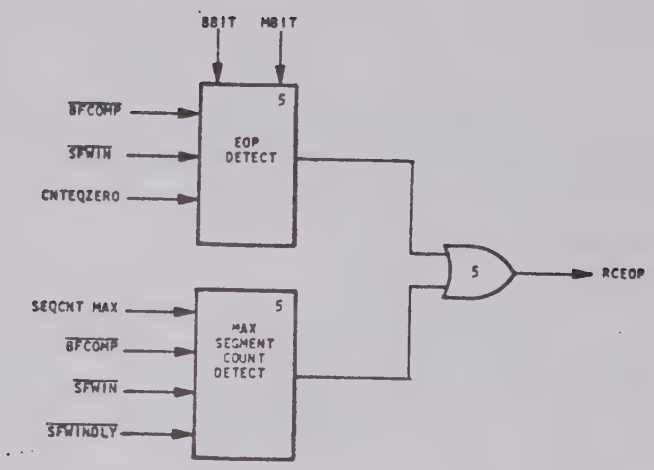


Figure 4-33. Recycle EOP Generation Functional Block Diagram

to a ONE level. This signal is gated with $\overline{\text{BFCOMP}}$, $\overline{\text{SFWIN}}$ and $\overline{\text{SFWINDLY}}$ to generate RCEOP when SFWINDLY terminates. $\overline{\text{BFCOMP}}$ and $\overline{\text{SFWIN}}$ prevent errors prior to SFWINDLY going to a ONE level.

4.5.6 Recycle Pattern Correlator (Figure 4-34)

This logic compares the received subframe sync pattern bit-by-bit with the stored pattern and generates a clock pulse each time a non-compare occurs.

The recycle pattern content memory is an eight bit X 4 word store containing the expected subframe sync pattern. It is loaded from the subframe setup store lines. When the READ STORE switch is depressed (or the computer is examining stores), the load address also controls the read address and the memory output drives the display. In normal operation, the memory read address comes from the pattern bit sequence counter. This is a 5-bit binary counter which increments from ZERO to 31 (if using 32 pattern bits). It is clocked during SFWINDLY by M BIT and reset by $\overline{\text{RSTSFCORR}}$ from the segment sequence counter logic. The three least significant bits of the counter generate a mux address and the two most significant bits are the pattern content memory read address. The counter increments from 00-000 through

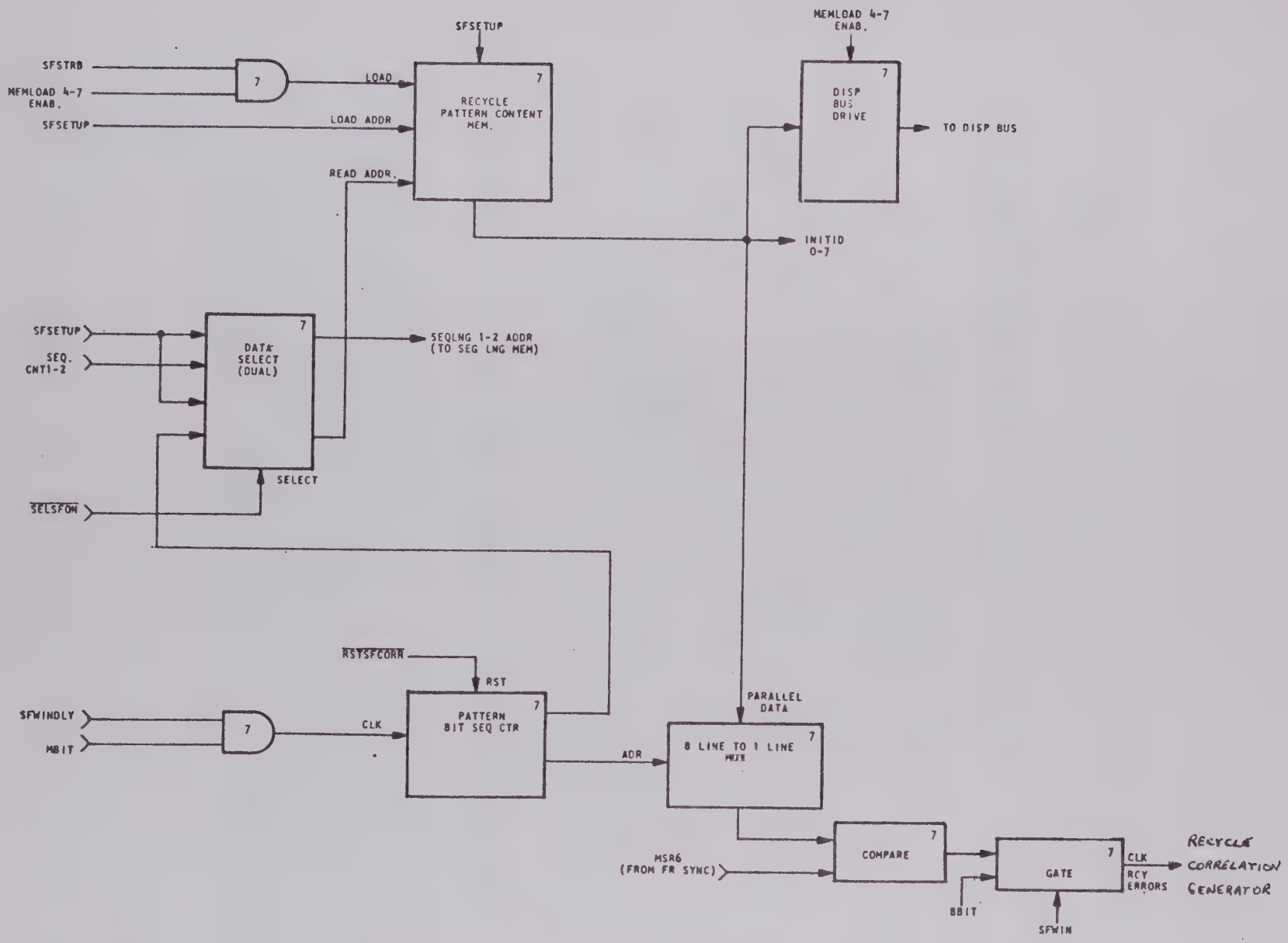


Figure 4-34. Recycle Patterns Correlator Functional Block Diagram

00-111 placing the eight bits of memory location 00 on the mux output. Next, the counter increments through 01-000 to 01-111 placing the eight bits of location 01 on the mux output. In this manner a maximum of 32 pattern bits can be programmed. When RSTSFCORR occurs, indicating end of pattern, the counter is reset and starts over next frame.

The pattern bit mux output is compared with the incoming serial data stream (from MSR6 in frame sync). Any non-compares during SFWIN time generate clock (error) pulses which go to the SF Correlation Pulse Generator.

In ID mode the pattern content store is held on address ZERO, and the store output is used to program the initial ID count to the ID predicting counter.

4.5.7 Recycle SF Correlation Generator (Figure 4-35)

This circuit compares the observed errors in the pattern to the allowable error stores and sets RCYCPRECD low when an acceptable pattern occurs. The recycle bit error counter is a four-bit binary counter which is clocked each time a non-compare occurs in the recycle pattern correlator logic. It is reset by RSTSFCORR each frame. The counter output which represents the number of errors in the pattern, is compared to the search/verify allowable error stores or the lock/check allowable error stores depending upon the SFLORC signal from the mode logic. Each frame time at CN+4 the RCYPATNRECD flip flop is set forcing RCYCPRECD to a ONE level. If the comparator output is a ZERO (indicating the counter output is less than the error store), when RECOP clocks the flip-flop, RCYCPRECD is set to ZERO level. If the counter output is equal to or greater than the error store number, the flip flop output remains at a ONE level when clocked, indicating a missed pattern.

When the subframe is in FCC or ID mode, or when the frame synchronizer is in search, the set input to the RCYPATNRECD flip flop is held and RCYCPRECD cannot go low.

RCYCPRECD is one of three inputs to a NOR-gate which outputs SFCPRECD (subframe correlation pulse received). FCCRECD is generated in FCC mode where the frame synchronizer, not the subframe synchronizer, detects the subframe pattern. FCCP resets the FCC RECD FF placing FCC RECD at ZERO level. The trailing edge of CN-2 of the next frame will clock FCCRECD back to a ONE level. When not in FCC mode, a set is held on the flip flop holding the output at a ONE level. The third input to the NOR-gate is from the ID mode logic. The gate output goes to the subframe mode logic.

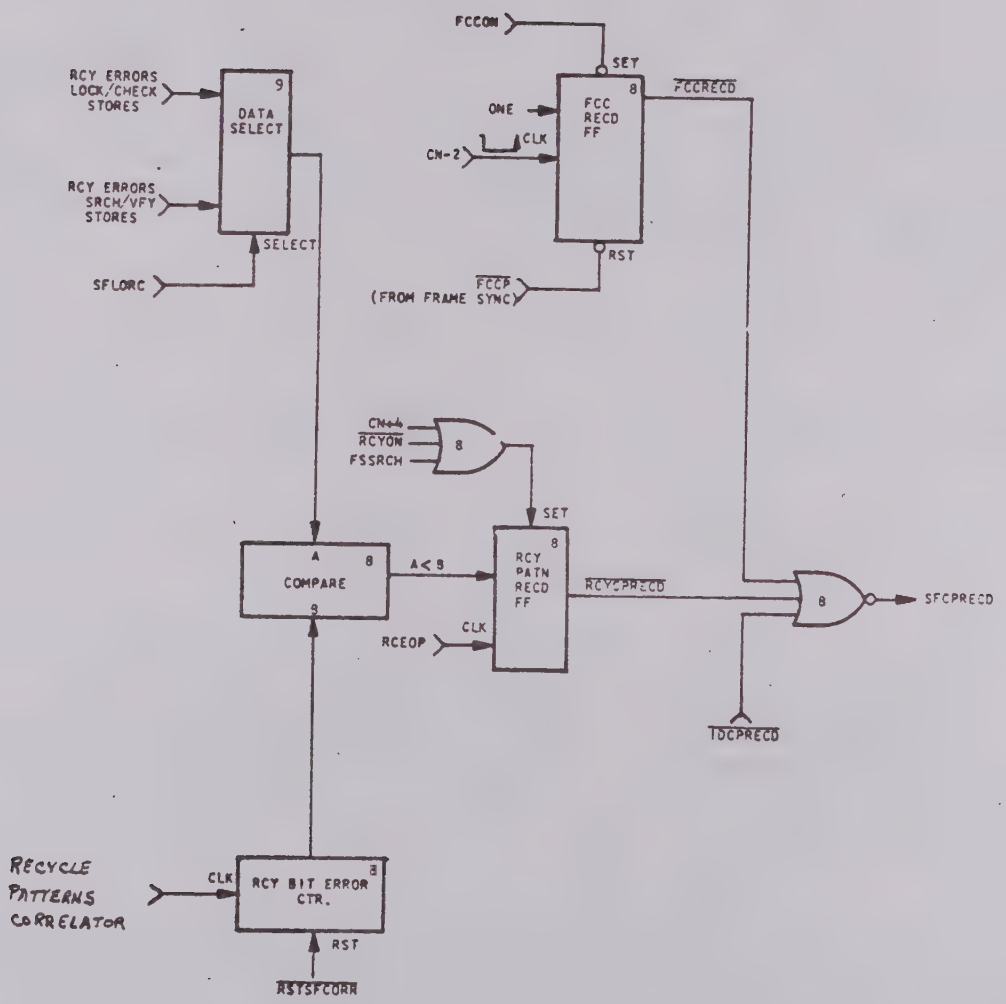


Figure 4-35. Recycle SF Correlation Generator Fun ctional Block Diagram

4.5.8 Subframe Patterns Count/Compare (Figure 4-36)

The subframe synchronizer can check a programmable number of patterns prior to moving out of the verify or check modes. This logic counts those patterns and generates PATSMAX (patterns max) which goes to the mode logic.

When the subframe is in search or lock modes, a reset is held on the subframe patterns counter and PATSMAX is not used. in the URC or FCC modes, the counter is clocked by CN+3 MBIT during the last frame of the subframe (FRNFF=1). The counter output is compared to the verify pattern stores or the check pattern stores depending upon which mode the subframe synchronizer is in. PATSMAX goes to a ONE level with a compare. Note that when the subframe is in verify or check mode, it will be going to search or lock mode depending upon SFCPRECD. In either case, the subframe patterns counter will be reset to ZERO.

In the ID mode, patterns are occurring each frame, not subframe. Therefore, the clock gate is always enabled and the counter is clocked at a frame rate.

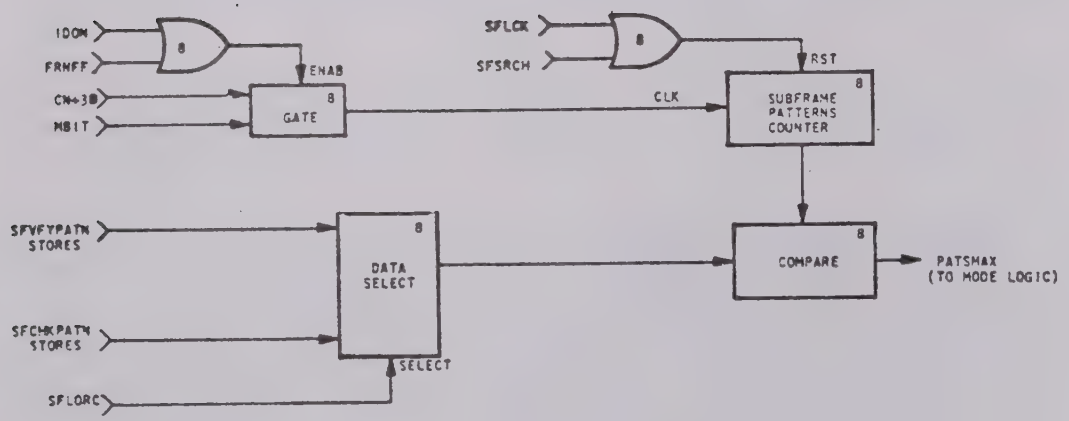


Figure 4-36. Subframe Patterns Counter/Comparator Functional Block Diagram

4.5.9 Subframe Mode Logic (Figure 4-37)

The mode logic consists of four flip flops; search, verify, lock and check, the control logic inputs to these flip flops and the clock circuit for the flip flops.

All four flip flops are clocked at CN+3 time, however, only one will be set to a ONE level as determined by the control inputs to each flip flop. The CN+3 clock goes through a gate which is enabled by several signals.

When the subframe is first turned on or when it is reset, FRNDLY which normally enables the gate is not being generated. FRSTPATN (first pattern) which is generated once, when the subframe is in search and the first SFCPRECD occurs, provides the first enable for the CN+3 gate. Subsequent enables are provided by FRNDLY which occurs once each subframe following the last frame of the subframe. In the case of ID mode, once the subframe has left search, the gate is enabled all the time and CN+3 clocks the mode logic each frame.

The search flip flop can be set by three conditions (other than SFRST). First, if the subframe is in search and SFCPRECD does not occur, a ONE appears on the data input and search flip flop output remains at ONE when clocked. Second, if the subframe is in verify and SFCPRECD does not occur, the search flip flop is set to a ONE by the clock. Third, if the subframe is in lock or check and after waiting for the number of patterns programmed a SFCPRECD does not occur, the search flip flop will be set to a ONE.

The verify flip flop can be set by two conditions. First, if PATS MAX has not been set, the first pattern received will set the verify flip flop. Note that if verify patterns were programmed to ZERO, PATS MAX would be set and the verify flip flop would not be set by the first pattern received. The second condition is when the subframe is in verify, PATS MAX has not yet occurred and SFCPRECD does occur. In this case, the synchronizer is remaining in verify for the programmed number of patterns before advancing to lock.

The lock flip flop can be set by three conditions. First, if the number of verify patterns was programmed to ZERO, PATS MAX would be set and the first received pattern (FRSTPATN) would set the lock flip flop. Second if the synchronizer is in verify for a number of patterns before advancing a SFCPRECD after PATS MAX is set will set the lock flip flop. Finally, if the synchronizer is in lock or check and SFCPRECD occurs, the lock flip flop is set.

The check flip flop is set by one condition. That is when the synchronizer is in lock or check, PATS MAX is not set and SFCPRECD does not occur. When in this mode if SFCPRECD occurs before reaching PATS MAX, the synchronizer returns to lock. However, if PATS MAX is reached and SFCPRECD does not occur, the synchronizer reverts to search mode.

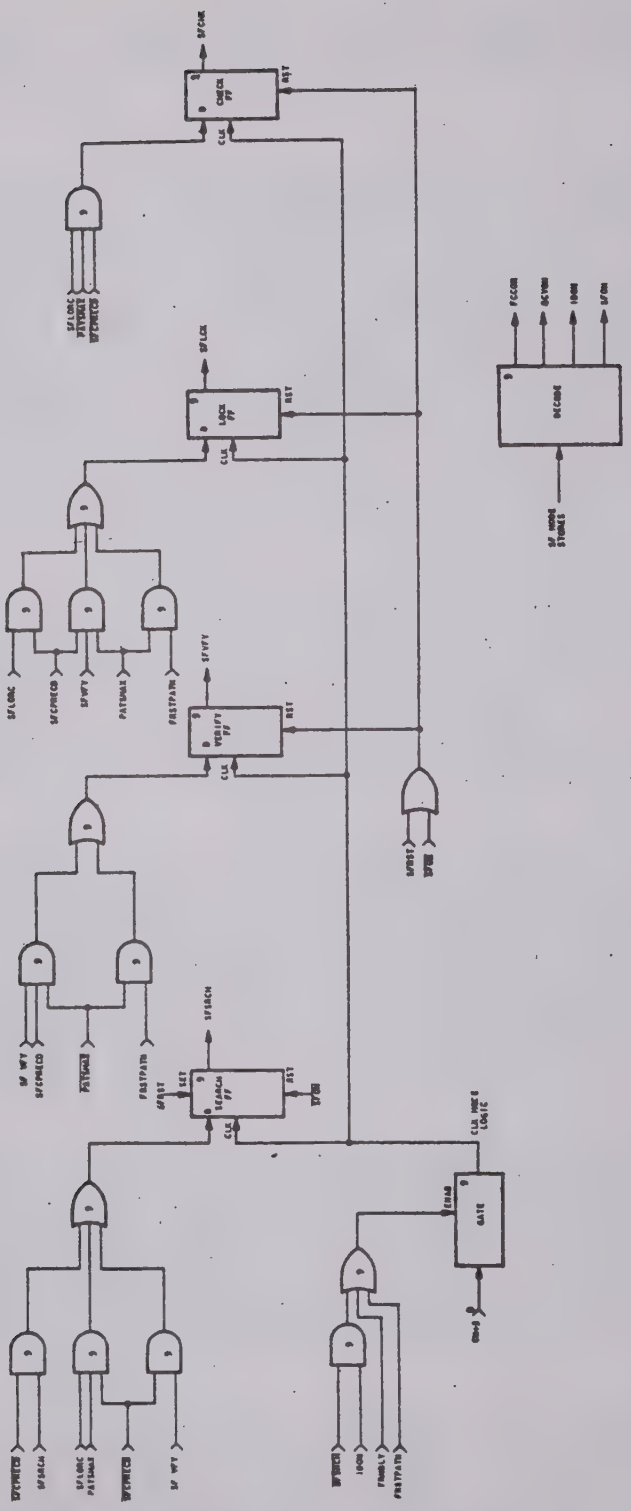


Figure 4-37. Subframe Mode Logic Functional Block Diagram.

The subframe mode stores are decoded to provide control signals for the three possible modes of operation; FCC, URC, ID and whether the subframe has been programmed on (SFON).

4.5.10 ID Pattern Correlation (Figure 4-38)

This circuit stores the incoming serial ID pattern number which may be aligned MSB or LSB first and compares this number to the internal predicing counter to generate an ID COMP (ID compare) if they agree.

No matter whether the ID word is occurring MSB or LSB first in the data stream, the transposer always converts it from serial to parallel and presents it to the input pattern store with LSB left oriented. When programmed for MSB first, the data stream from MSR6 of the frame sync is clocked into the shift register left-to-right by B Bit. This occurs only during SFWIN and SFWINDLY when the ID word is occuring. Outside SFWIN and SFWINDLY a reset is held on the shift register. When programmed for LSB first, the shift register clock is disabled and the set enables are used to place data in the register starting at the left position and moving right. When BF COMP occurs indicating the first bit location of the ID word, a ONE is placed on the data input to the shift-one register. A clock gate is also enabled and remains so during SFWIN. M BIT clocks the ONE left to right through the register, generating individual set enables to the ID shift register. If the incoming data (MSR6) is at a ONE level, B Bit will store a ONE in the enabled register stage. If MSR6 is a ZERO, the enabled stage remains at ZERO. At the end of the ID word, CTREQZERO will be set to a ONE level (see Bit/Segment Control logic). CNTEQZERO is gated with SFWINDLY and M BIT to strobe the ID shift register data into the input pattern store.

During initial search mode, a load is held on the predicting counter and the initial ID number is loaded into the counter. Following the first IDEOP (ID end of pattern) which occurs on the trailing edge of SFWINDLY, the ID mode logic moves to fast search and CLK FR CTR begins clocking the predicting counter at bit rate. The counter increments or decrements according to the up/down stores. When the counter matches the received ID word number an ID CMP is generated. ID CMP generates XTRACLK which provides one more clock pulse to the CLKFRCTR line incrementing the predicing counter and terminating ID COMP. At this time, the mode logic leaves fast search and the predicting counter output is setting on the next ID word number to be received.

4.5.11 ID Mode Logic (Figure 4-39)

The ID mode logic goes through four possible stages while incrementing the frame counter and predicting counter up to the received ID word number.

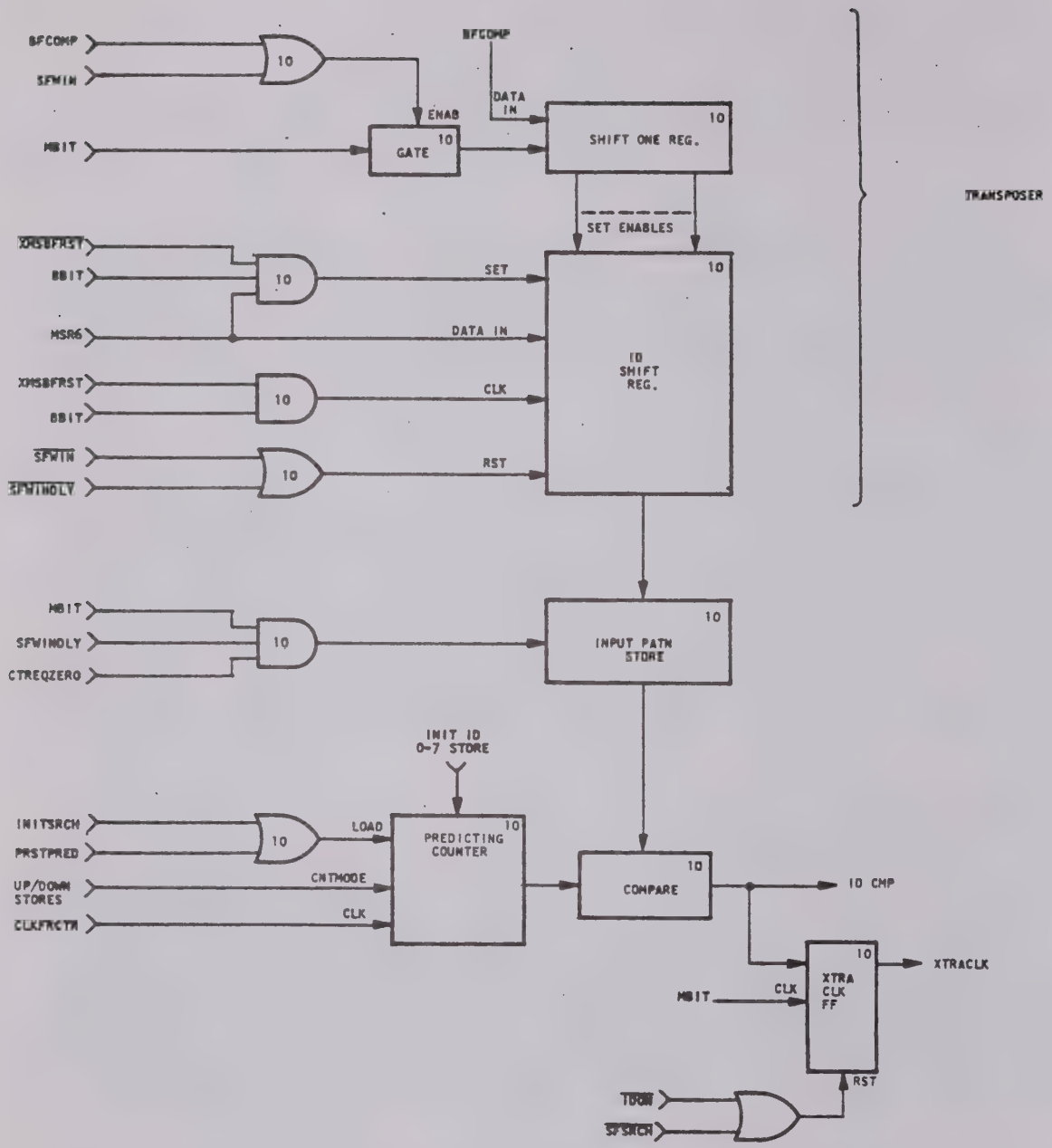


Figure 4-38. ID Patterns Correlation Functional Block Diagram

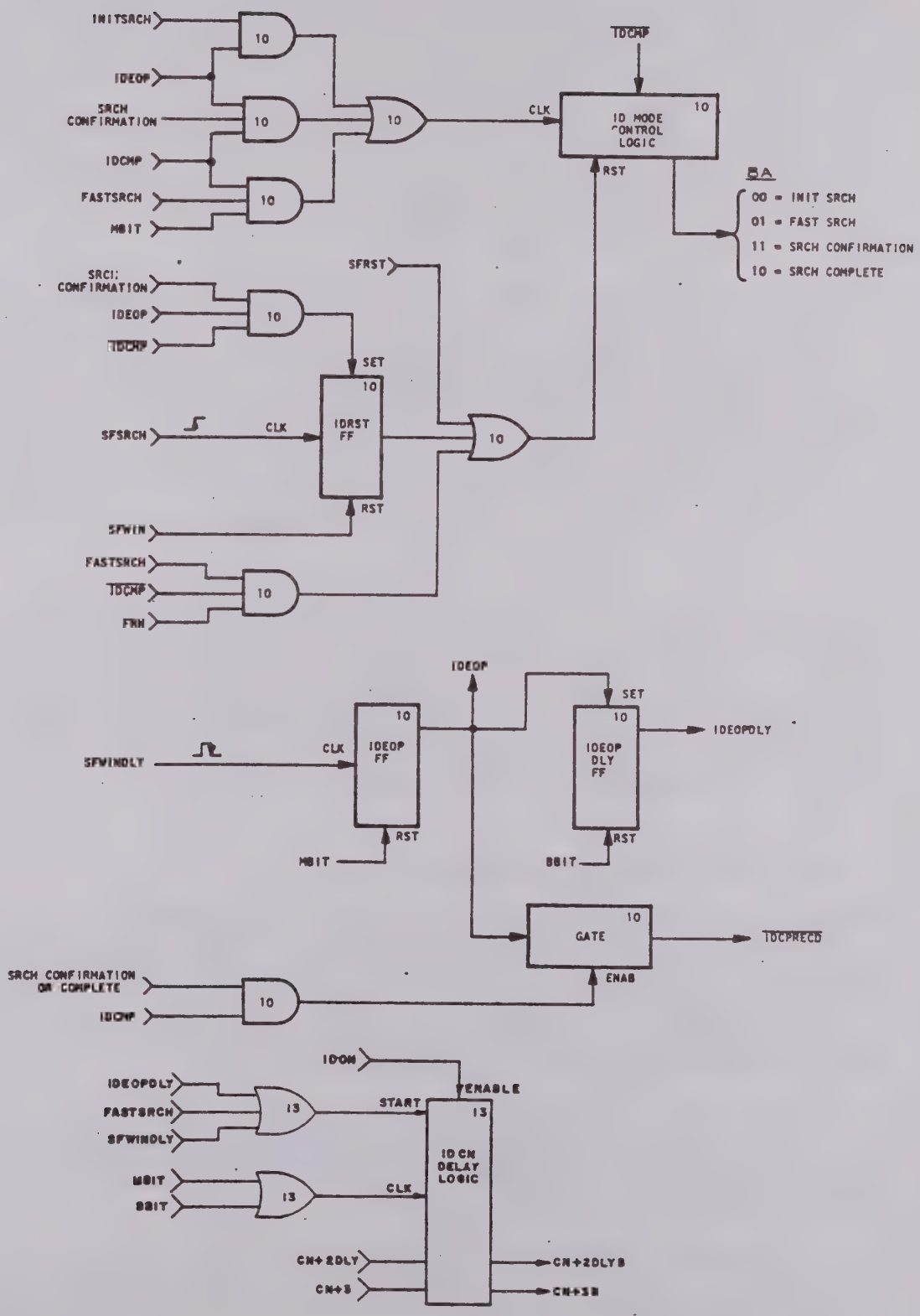


Figure 4-39. ID Mode Logic Functional Block Diagram

In initial search the predicting counter and frame counter are loaded with initial values. Clock pulses are occurring, but the counters are held by the load condition. When IDEOP occurs (trailing edge of SFWINDLY), the received ID word is present on the comparator input in the ID Pattern Correlation logic. INIT SRCH and IDEOP clock the ID mode logic to fast search. The load to the predicting counter and frame counter is removed and the counters are clocked at bit rate until an IDCMP occurs. The following M Bit gated with FAST SRCH and IDCMP clocks the ID mode logic to search confirmation. If ID CMP does not occur before receiving FRN (last frame) the mode logic is reset to INIT SRCH.

After reaching search confirmation, the bit rate clock is inhibited and XTRACLK has incremented the predicting counter and frame counter to the expected ID word number of the subsequent frame. At IDEOP, if an IDCMP occurred, the ID mode logic moves from search confirmation to search complete. However, if an IDCMP did not occur, the ID RST FF is set causing the ID mode logic to revert to initial search. The flip flop is reset by the next SFWIN. Once the mode logic is in search complete it is reset to initial search only if the subframe synchronizer reverts to search mode. The rising edge of SFSRCH will clock the ID reset FF to reset the ID mode logic.

The trailing edge of SFWINDLY generates IDEOP which is reset by M Bit one-half bit time later. IDEOPDLY occurs at the same time but remains one-half bit time longer than IDEOP. When IDEOP occurs, the ID mode logic is in search confirmation or search complete and an IDCMP has geen generated, IDCPRECD (ID correlation pulse received) will be generated. This pulse goes to the SF correlation generator where it is used to set SFCPRECD when the synchronizer is in the ID mode.

4.5.12 Frame N Generation (Figure 4-40)

The frame counter is loaded from the initial frame number store, counts up to the final frame number store and generates $\overline{\text{FRN}}$. When the synchronizer is in FCC or URC modes, the frame counter is initially loaded by FRSTPATN. Subsequent loads are accomplished by FRN. When the synchronizer is in ID mode FRSTPATN is inhibited and INITSRCH provides the first load pulse. Subsequent loads are again accomplished by FRN.

The clock pulses for the frame counter come from several sources. In FCC or URC modes, the inhibit to the CN+2DLY gate is removed and this pulse gated with B Bit clocks the counter at the beginning of each frame. All other clock inputs are inhibited.

If the synchronizer is in ID mode, the CN+2 DLY pulse is inhibited if the subframe is in search mode or if the FRSTPATN (first SFCPRECD) occurred during the present frame. FRSTPATN will be reset at the beginning of the subsequent frame and CN+2 DLY will clock the counter thereafter unless the subframe returns to search mode.

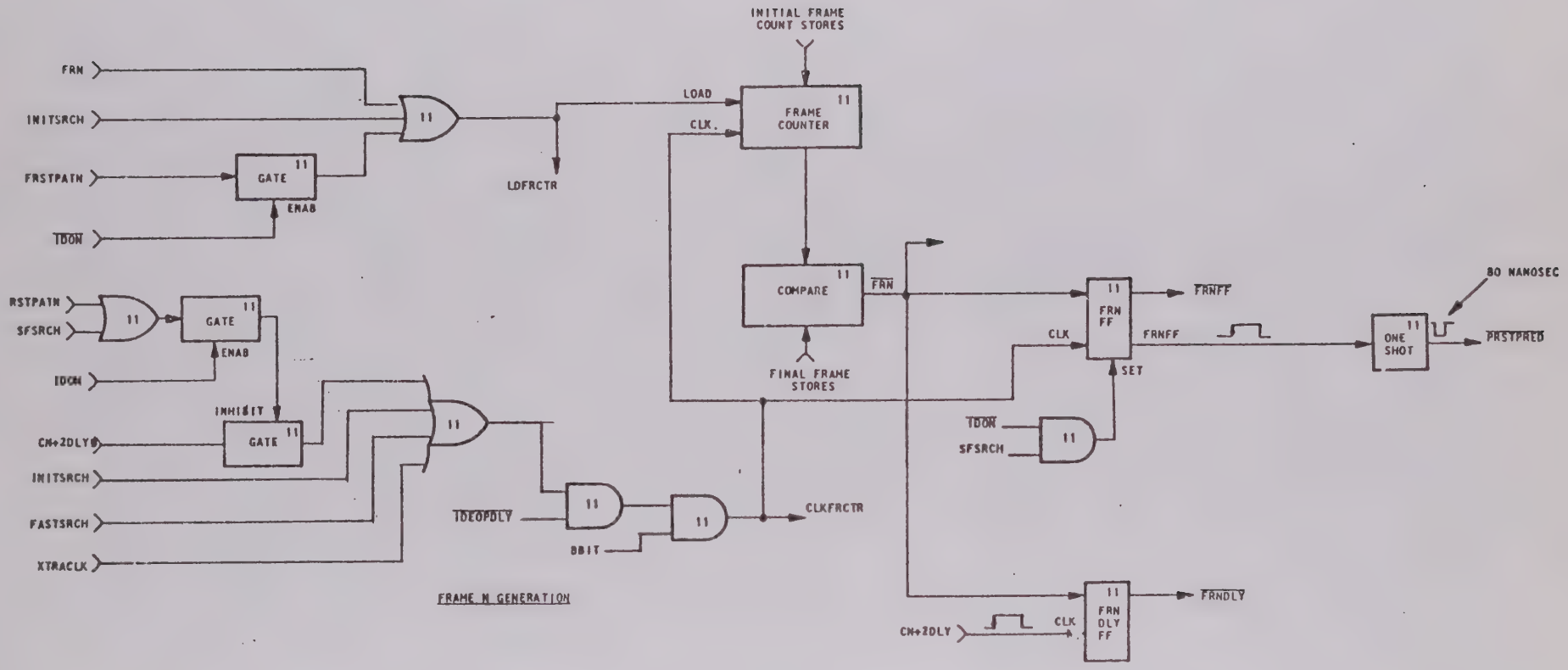


Figure 4-40. Frame N Generation Functional Block Diagram.

During the time CN+2DLY is being inhibited, clock pulses to the counter are controlled by INITSRCH, FASTSRCH and XTRACLK. In INITSRCH, B Bit is clocking the counter but the load pulse holds it at the initial frame number. When the ID mode logic changes to FASTSRCH, B Bit begins incrementing the counter each bit time. When the frame counter and predicting counter reach the received ID word number, fast search is terminated and the ID CMP generates one additional clock by setting XTRACLK long enough to allow an additional B Bit. The counters are now at the expected ID word number and this is the reason FRSTPATN blocks the next CN+2 DLY pulse. All clock control lines are gated with IDEOPDLY to prevent race conditions while the ID mode logic is changing modes.

FRNFF is generated one frame later than FRN (during the first frame of the subframe). In the FCC andURC modes FRNFF is held at a ONE level in SFSRCH. In ID mode it is not held. The leading edge of FRNFF triggers a one-shot to produce PRSTPRED (preset predicting counter) which loads the initial ID number into the predicting counter. FRNDLY is triggered by the leading edge of CN+2DLY at the end of FRN. It is used to enable the CN+3 to the subframe mode logic.

4.5.13 SF1/SF2 Display Control Select (Figure 4-41)

The front panel display can be controlled from SF1 or SF2. Therefore, the necessary timing and status signals from both subframe synchronizers are input to a data selector which is controlled by front panel selection of SF1 or SF2.

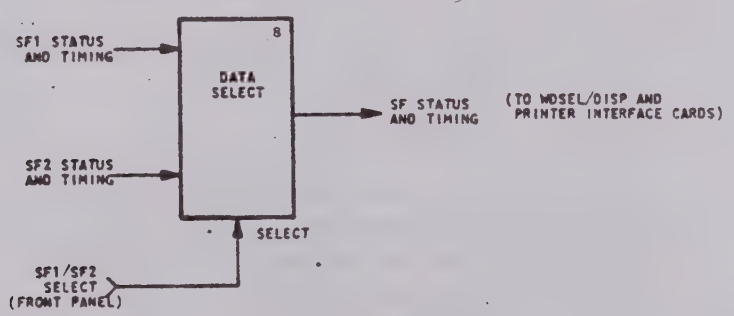


Figure 4-41. SF1/SF2 Display Selection Control

4.6 PCM SIMULATOR (Figure 4-42)

The optional PCM simulator is contained on two cards: Simulator 1 and Simulator 2. Simulator 1 includes the VCO/clock generator, ID word generator, pseudo-random generator and output amplifier circuit. Simulator 2 contains the parameter stores, address decoder, word enable generation logic, EOW, EOF, and EOSF generation logic, parallel-to-serial converter and polarity control logic.

The internal optional simulator provides a serial data stream using up to eight word types; Words A, B, C, D, E, F, G and H. The A, B, C, D, E and F data values are fully programmable. The G word data is the words/frame count and the H word data is a pseudo-random sequence. This sequence provides a serial, random one/zero pattern output. The simulator is programmable as an 11-bit generator in which case a 2047 bit pattern is generated before repeating, or a 16-bit generator that produces a 65,535 bit pattern before repeating. The A and C words can be programmed to word lengths independent of the lengths of other words. The C, D, E and F words can be placed in the main frame or subframe. All words can be programmed into any word location in the format. In addition, the F, G or H word can be used as the filler (common) word.

The simulator can generate an ID word one to eight bits in length, LSB or MSB first, which can be located anywhere within the D word. The initial ID count can be programmed and incremented or decremented each frame or subframe depending upon location of the D word.

The simulator clock frequency is controlled by a phase lock loop comprised of a VCO, predivider and programmable divider, phase detector/filter, and reference oscillator. A deviation input allows frequency modulation of the simulator clock. The simulator can provide serial NRZ-L, NRZ-M, NRZ-S, RZ, BiØ-L, BiØ-M, BiØ-S, DM-M, or DM-S, all under program control.

The following paragraphs describe the operation of the functional circuits contained on Simulator 1 and Simulator 2 cards.

Note

The numbers within symbols and blocks of the individual circuit diagrams refer to the sheet number of Simulator 1 Card schematic diagram (Section 6 - Drawing No. 28047) or Simulator 2 Card schematic diagram (Section 6 - Drawing No. 29340) where that particular function is located.

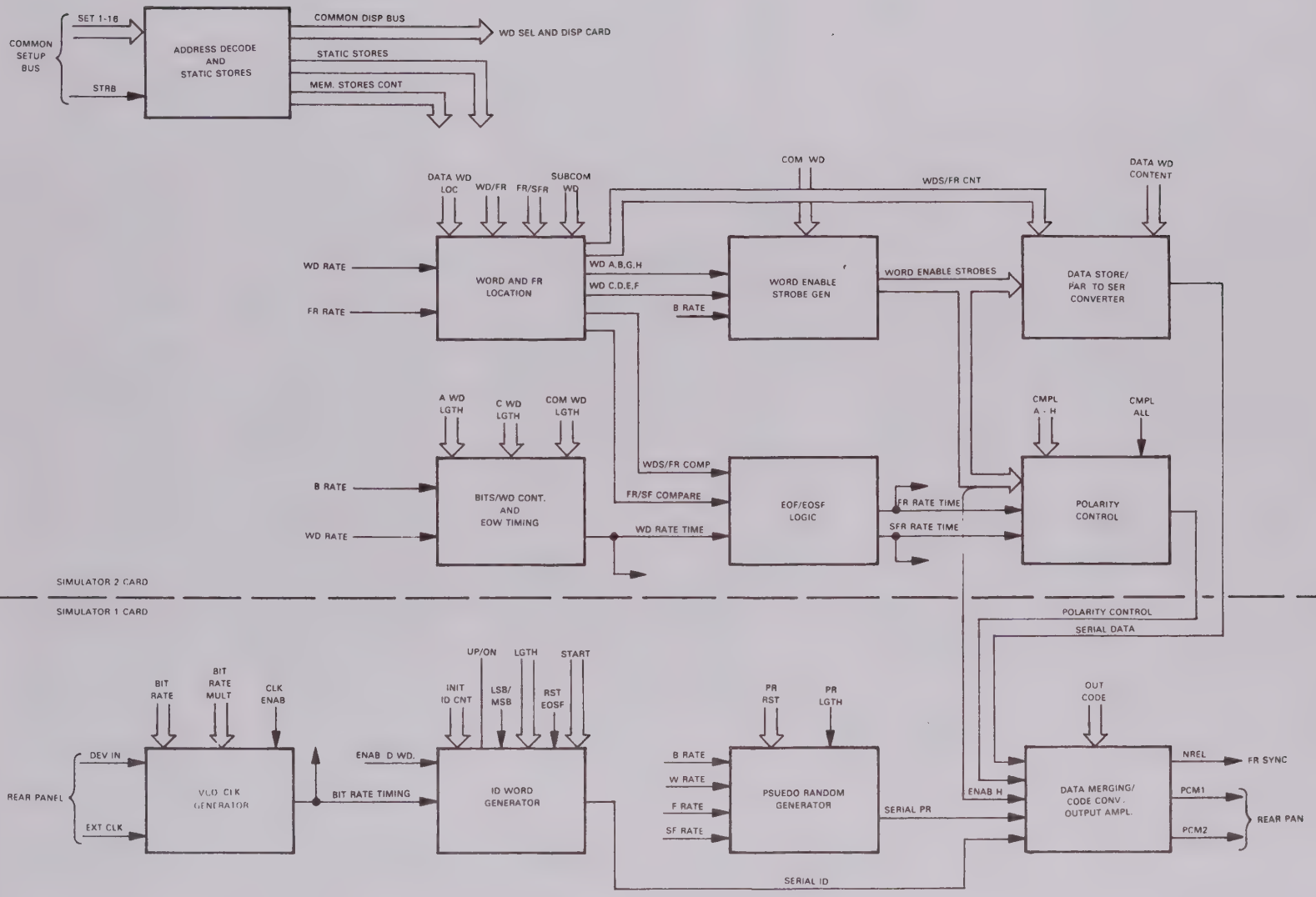


Figure 4-42 PCM Simulator Overall Block Diagram

4.6.1 Program Control and Static Stores (Figure 4-43)

The simulator has a total of 50 parameter stores to be set up. $\overline{\text{SET 16}}$ through $\overline{\text{SET 9}}$ are decoded to provide these store addresses. Fourteen addresses, SIMADR 0 through 13 enable static stores. Four addresses SIMADR 48 through 51, load the E word and F word content memories. The LOAD MEMADR (two bits) combined with SMEMDEV0 through 7 provide the remaining 32 addresses. SMEMDEV0 through 7 are narrow pulses occuring when $\overline{\text{SET STRB}}$ goes low. EMEMDEV0 through 7 enable the display drivers associated with each store. When the store (function) is selected in program mode, the store contents are displayed. $\overline{\text{SET8}}$ through $\overline{\text{SET1}}$ are buffered and applied to all store inputs.

4.6.2 VCO/Clock Generator (Figure 4-44)

The simulator clock frequency is controlled by a phase lock loop composed of a VCO, predivider and programmable divider, phase detector/filter, and reference oscillator. A deviation input allows frequency modulation of the simulator clock.

The VCO output which ranges from 12 MHz to 24 MHz, depending upon the selected bit rate, is input to a predivider which provides division by 1, 2, 3, or 5 depending upon the value of the MSD (most significant digit) setting. The frequency is further divided by the programmable divider. Essentially, this is a decrementing BCD counter that initially loads the contents of the bit rate stores, is decremented to zero by the predivider output, generates an output pulse, reloads the contents of the bit rate stores and continues this cycle. The repetition rate of the programmable divider output when the loop is in equilibrium will be 400 Hz (or more correctly, equal to the reference frequency input to the phase comparator). It should be noted that the repetition rate of this output is 400 Hz, however, the duty cycle is generally not 50%.

A free running 80 kHz oscillator output is divided down to 400 Hz and becomes the reference input to the phase comparator. The phase comparator responds to time differences in the negative-going transitions of the two inputs. Perturbations in the programmable divider output due to bit rate changes cause phase errors which, in turn, changes the DC error correction voltage out of the filter/amplifier. This voltage is applied to the VCO control input and causes the VCO frequency to change in the proper direction to cancel the phase error.

The deviation amplifier has a gain of -.33. This provides a deviation sensitivity of 1%/volt. The amplifier output is summed into the VCO control voltage input and changes the VCO frequency. To prevent correction of this frequency change by the loop, the reference frequency is simultaneously deviated by the same percentage. Therefore, the phase comparator inputs will remain in step preventing any change in the error correction voltage level.

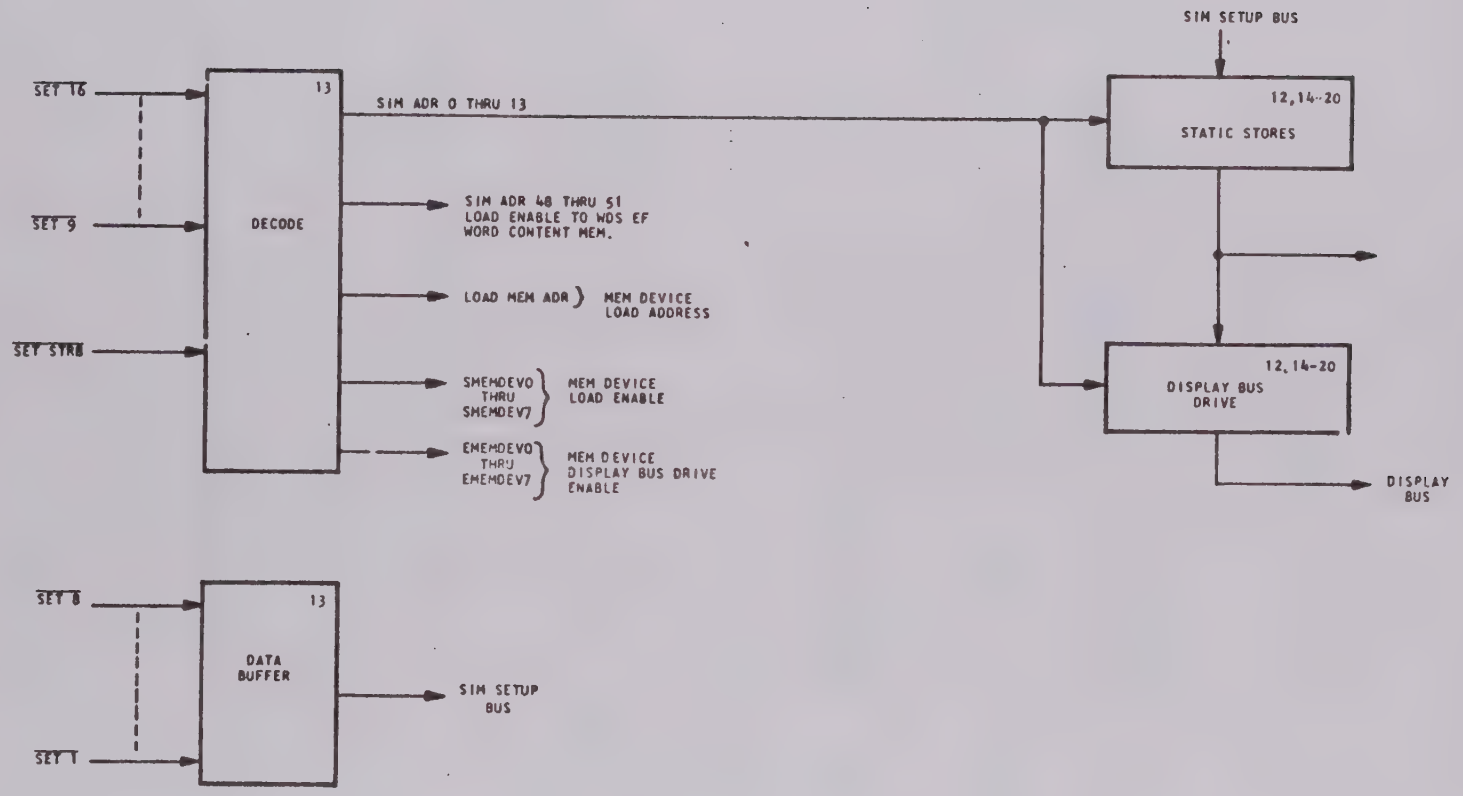


Figure 4-43. Program Control and Static Stores (Card 2)

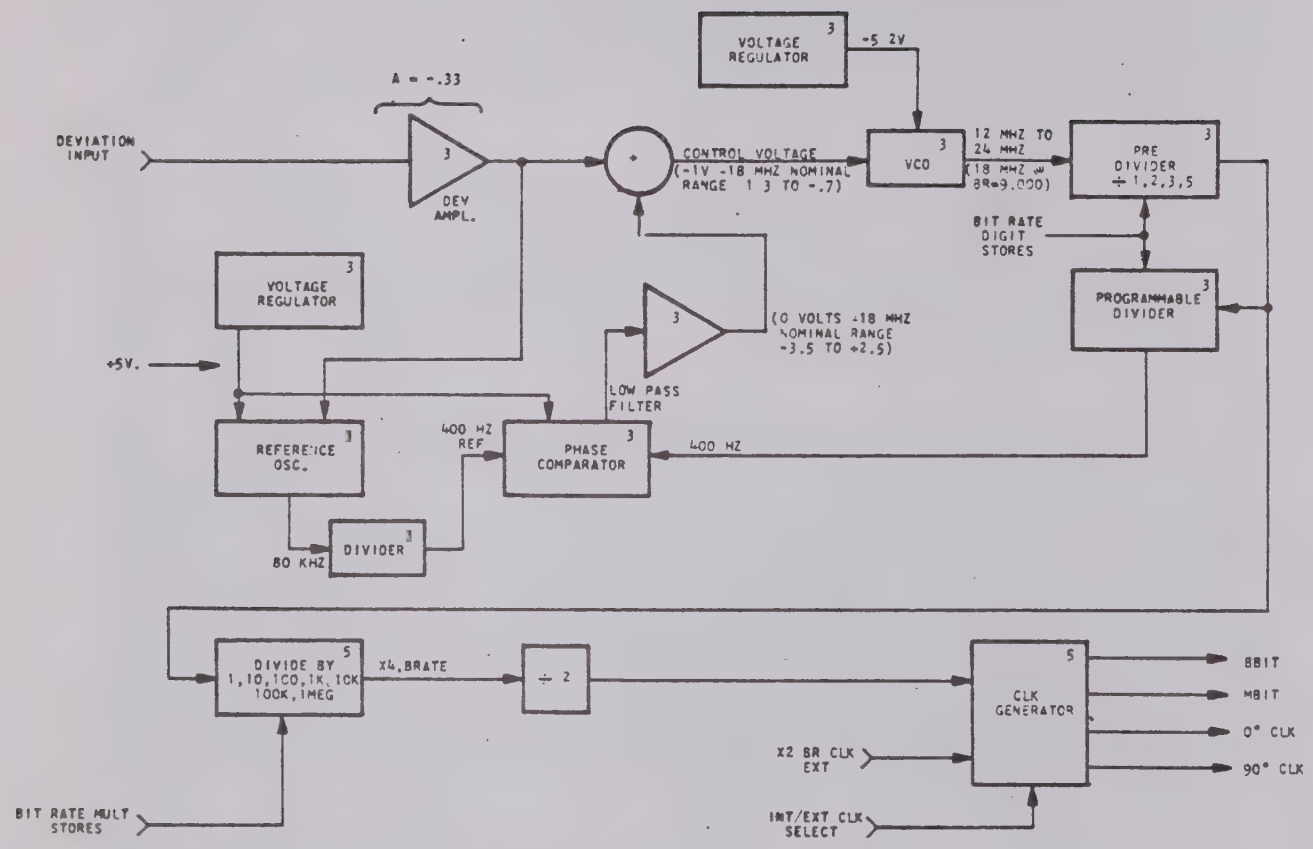


Figure 4-44. VCO/Clock Generator (Card 1) Functional Block Diagram

A separate +5 volt regulator supplies power to the reference oscillator and the phase comparator in order to minimize changes in their operating characteristics due to power supply perturbations. The VCO requires a -5.2 volt supply because it is MECL logic.

The predivider output is routed to a decade divider which is controlled by the bit rate multiplier stores. It performs division by 1, 10, 100, 1K, 10K, 100K, or 1M. The output of this divider is divided by two, to supply a X2 clock to the clock generator.

The clock generator selects the X2 clock from the divider or an external X2 clock and generates two symmetrical bit rate clocks, 0° and 90°, and two 1/4 bit wide pulses, B Bit and M Bit. B Bit coincides with the rising edge of 0° clock and M Bit coincides with the rising edge of 90° clock.

The following table shows the relationship of the VCO frequency, the predivider setting and the predivider output as a function of the MSD contained in the bit rate stores:

MSD	VCO Freq. (MHz)	Predivider	Predivider Output Freq. (MHz)
5	20	1	20
4	16	1	16
3	12	1	12
2	16	2	8
1	12	3	4
9	18	5	3.6
8	16	5	3.2
7	14	5	2.8
6	12	5	2.4

4.6.3 Pseudo-Random Generator (figure 4-45)

This circuit provides a serial, random one/zero pattern output which is used as the H word data. The generator is continuously clocked by M Bit whether used or not in the output format. It is programmable as an 11-bit generator in which case a 2047 bit pattern is generated before repeating or a 16-bit generator which produces a 65535 bit pattern before repeating. The generator preset (load) is programmable for none, EOF or EOSF. For the case of no preset, the generator runs out to maximum and simply repeats. When programmed for EOF or EOSF preset, the coincidence of the selected preset and BN causes the generator to return to the initial state and begin again. When the simulator is reset from the front panel, B Bit and SIMRSTDLY return the generator to its initial state and insure that it starts up on the first bit of a word, not at some other time in the word. The pseudo-random output goes to the data merging logic.

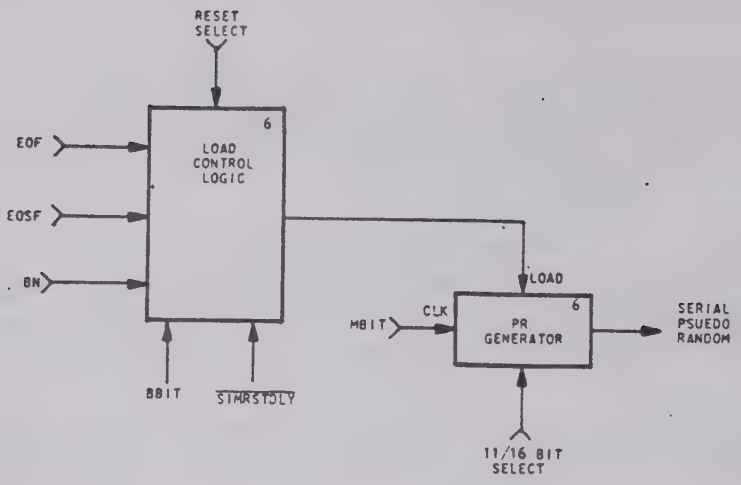


Figure 4-45. Pseudo-Random Generator (Card 1)

4.6.4 ID Word Generator (Figure 4-46)

The simulator can generate an ID word one to nine bits in length, LSB or MSB first, which can be located anywhere within the D word. It can be incremented or decremented each frame or subframe depending upon location of the D word. The initial ID count can be programmed and the counter can be reset by EOSF or not reset at all.

The ID word generator logic remains quiescent until ENAB D WD occurs. At BN time following ENAB D WD the ID control line goes active. Also, the ID DATA generator is loaded from the initial ID count stores if FR CMP is present or incremented (decremented) if FR CMP is not present. The ID DATA generator remains at this count until another ENAB D WD occurs. The ID Control enables the set gate to the ID ENAB FF. When the bits/word counter compares with the ID start store (defines 1st ID bit location within D word) the FF is set and EN SER ID becomes active. This signal loads the ID length counter. The number loaded into the counter depends upon whether the ID word is to be shifted out MSB or LSB first. When programmed to MSB first, the ID word length store content is loaded into the counter which is decremented to zero and generates a compare with the gate output which is all ONES. (Exclusive OR comparator.) When programmed to LSB first, ZEROS are loaded into the counter which increments to the ID length store content and generates a compare with the gate output which is the complement of the ID length stores. The compare resets the ID ENABLE FF terminating further operation of the ID word generator logic. The ID length counter output is also applied to the MUX address control logic. When programmed to

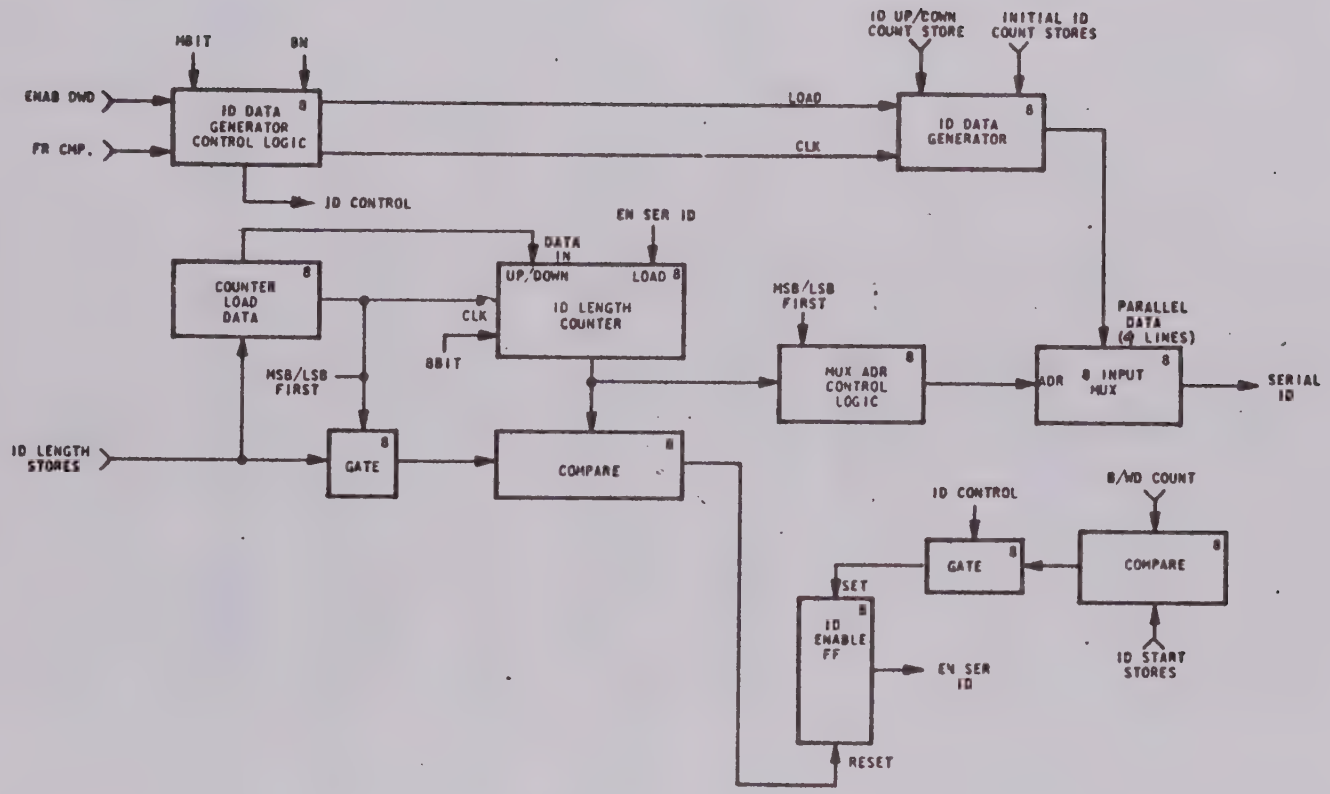


Figure 4-46. ID Word Generator (Card 1) Functional Block Diagram

MSB first, the mux address starts at the maximum address (can be 2 thru 8 depending upon ID word Length) and decrements to zero. The address sequentially places each of the parallel data inputs on the SERIAL ID output line.

4.6.5 Word and Frame Location (Figure 4-47)

The ABGH word location memory is a 16-bit x 4 word store containing the location (in BCD) of these four words. Data is loaded into the memory from the simulator setup bus by the memory address. At the beginning of each word time, as the present word is undergoing parallel to serial conversion at the output, LOCADR (local address) begins incrementing at bit rate. This address is a two-bit binary count. Sequentially the A, B, G and H word locations are read into a comparator. The other comparator input is the word/frame count. The comparator output goes to the Word Enable Strobe logic. If a compare occurs, LOCADR stops incrementing and the word location which caused the compare remains on the memory output lines holding the compare until the next word time. The memory output is also input to the display bus driver and can be displayed in the program mode.

The CDEF word location memory and compare operation is identical to the ABGH word operation and in fact is tested for a compare at the same time. Thus, in 4 bit periods eight word locations are checked.

Words CDEF also have subframe capability and the frame location memory for these words is compared to the frame counter to generate a frame compare. Otherwise the operation is identical to the ABGH word operation described above.

The word count is also compared with the programmed words per frame to generate WD CMP.

The C WD, D WD, E WD, F WD enable operation is identical to the ABGH enable with the additional requirement of a frame compare if the word is programmed for subcommutation.

If the local address counter reaches max and no compare is generated, the common word is enabled. The common word store determines whether the G, H, or F word is enabled.

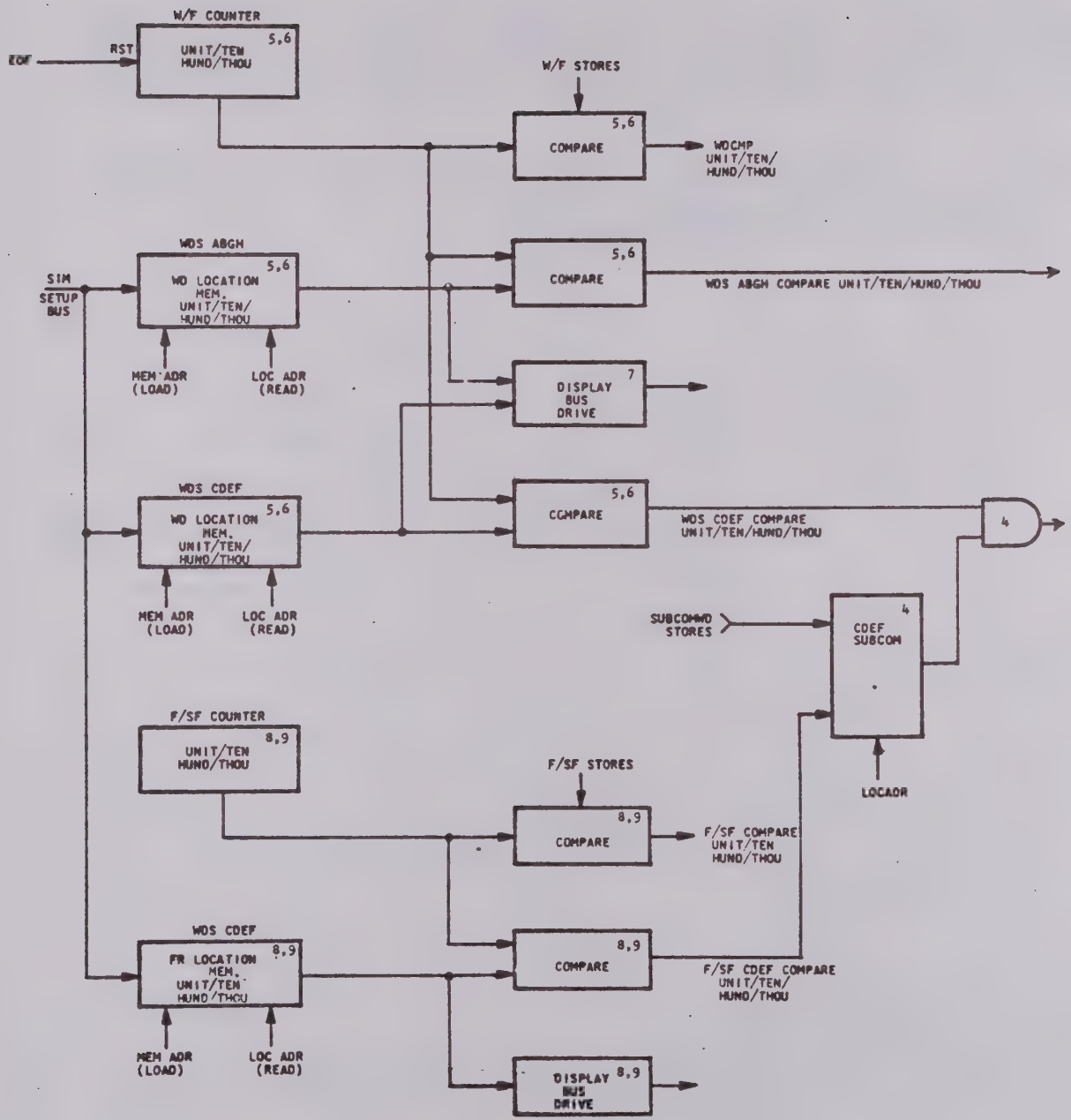


Figure 4-47. Word and Frame Location (Card 2) Functional Block Diagram

4.6.6 Word Enable Strobe Generation (Figure 4-48)

This logic receives the word and frame compares from word and frame location logic and generates the appropriate word enable pulse or in the absence of a compare the programmed common word is enabled.

The local address counter is a two-bit counter which is reset to zero at the end of a word and increments at bit rate up to maximum count unless inhibited earlier by a compare. If the counter reaches maximum, the clock is inhibited until the next word time.

The ABGH compare is applied to the enable input of a decoder. LOCADR routes this enable to the appropriate output, A WD, B WD, G WD, H WD (the word which generated the compare).

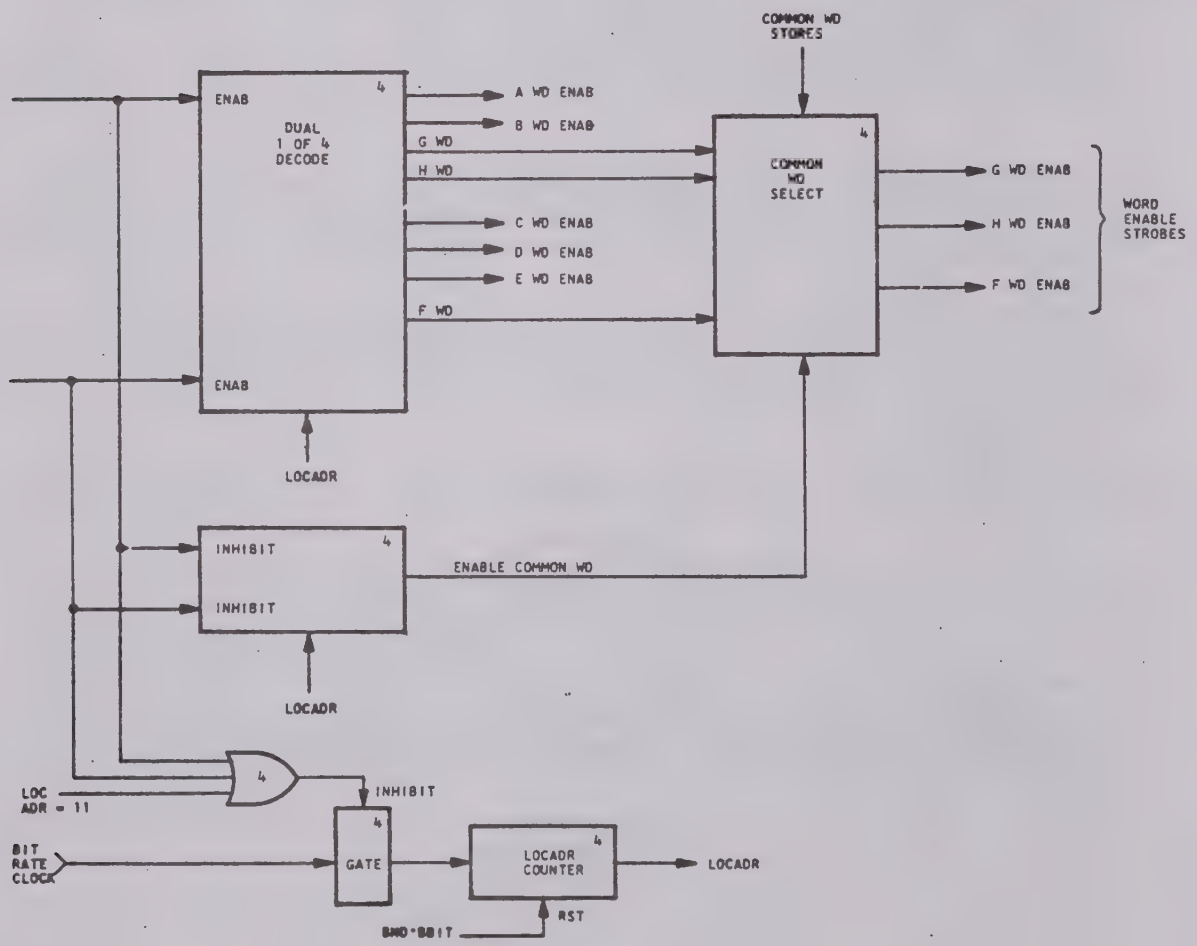


Figure 4-48. Word Enable Strobe Generator (Card 2)

4.6.7 Bits/Word Control and EOW Generation (Figure 4-49)

The word length memory contains the A word, C word and common word lengths. The A WD ENAB and C WD ENAB lines determine which word length is placed on the memory output. If neither the A WD or C WD is enabled, the common length is output. At the beginning of each word time, the word length is stored. The store output is compared to a bit/word counter. The compare (BN-1) initiates a series of bit wide EOW pulses. BN-1 DLY pulse resets the bit/word counter.

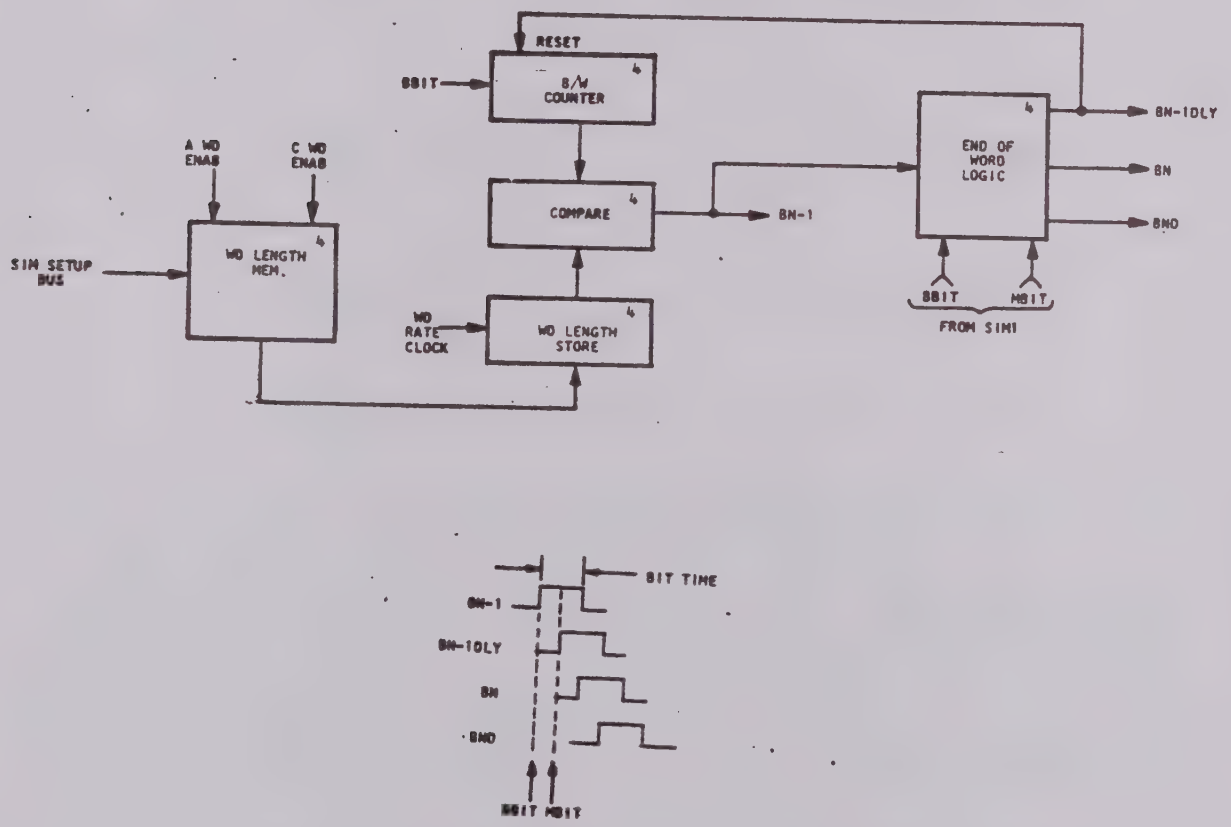


Figure 4-49. Bits/Word Control and EOW Generator (Card 2)

4.6.8 EOF and EOSF Timing Circuits (Figure 4-50)

Coincidence of WD CMP and the leading edge of BND sets the EOF pulse one half bit time before the end of the frame. It remains set until one half bit time before the end of word one of the following frame. EOF provides the lead pulse to the word counter and provides a reset to the pseudo-random generator (if programmed).

Coincidence of FR CMP, WD CMP and BND generate the EOSF pulse. This pulse is identical to EOF except it occurs only after the last frame of the format. EOSF provides the load pulse to the frame counter and provides a reset to the pseudo-random generator (if programmed).

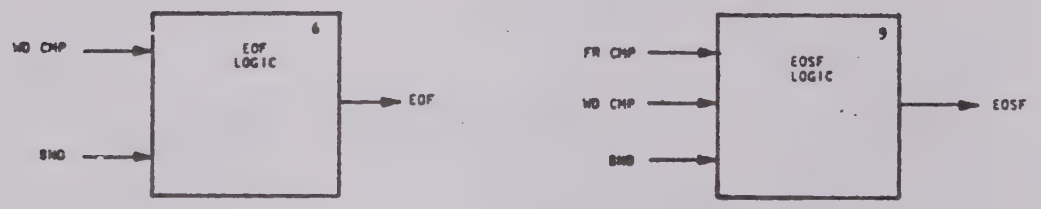


Figure 4-50. EOF and EOSF Timing Generator (Card 2)

4.6.9 Data Stores and Parallel-to-Serial Conversion (Figure 4-51)

The ABCD data word content memory is a 16-bit x 4 word store containing the data value of these four words. The data is loaded from the simulator setup bus by the memory address (LOAD). The ABCD word enable decoder generates a two bit address whose value depends upon which word is enabled. Assuming the E, F, or G words are not enabled, this address places the appropriate data word on the memory bus input to the parallel-to-serial converter.

The EF data word content memory control and operation is identical to the ABCD memory. If the G word is enabled, the BCD word count is buffered and applied to the memory bus.

The memory bus is connected to the display bus driver and allows display of these memory contents.

The parallel-to-serial converter which can accommodate a maximum of 16 bits is constantly shifting data out at bit rate. The serial data output is applied to the data merging logic on card 1.

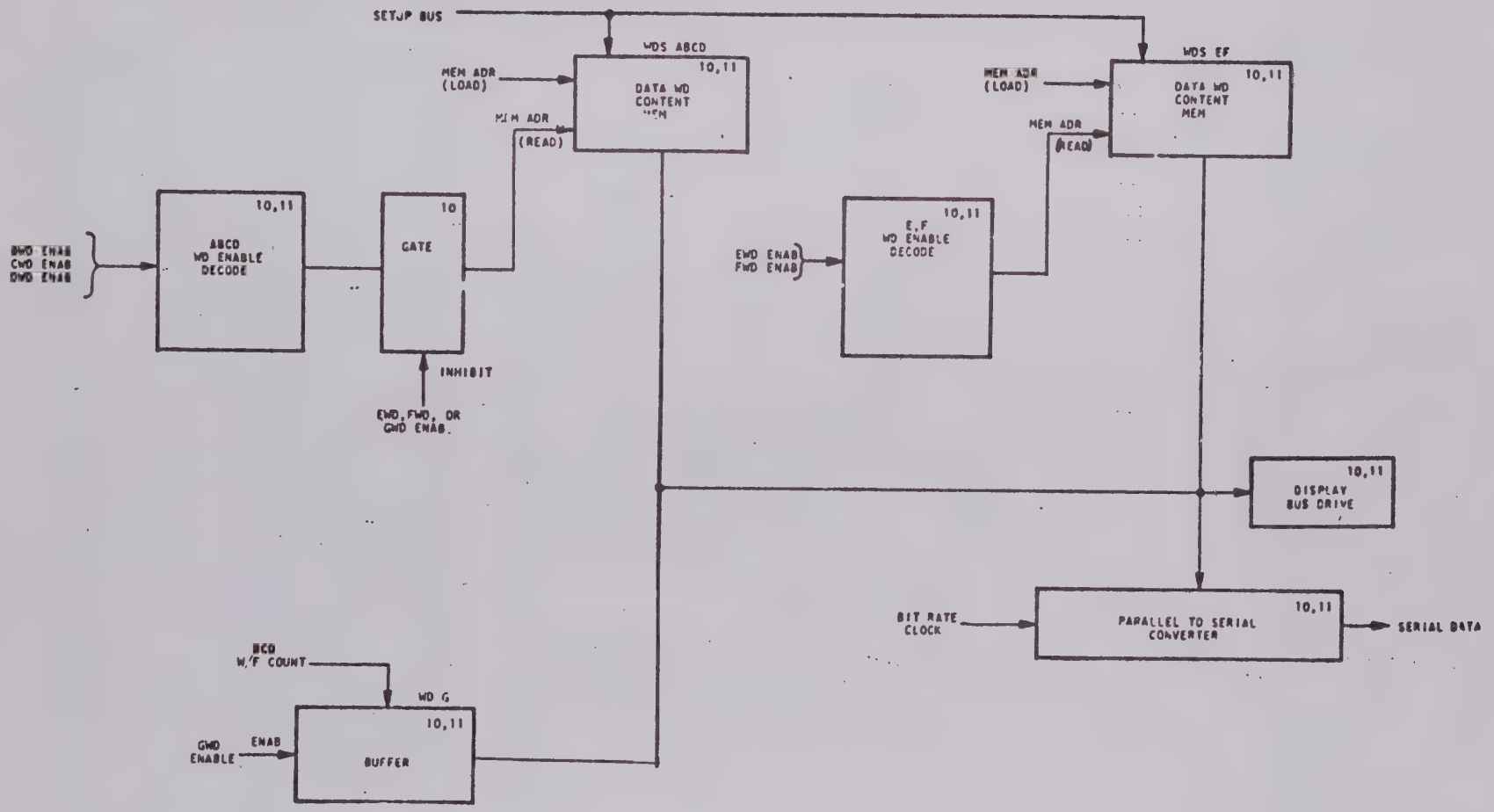


Figure 4-51. Data Stores and Parallel-to-Serial Converter (Card 2)

4.6.10 Output Polarity Control (Figure 4-52)

This logic provides a means of complementing any one or combination of the eight types of data words for one frame of N frames. The invert word stores (one for each word type) are combined with the word enable strobes to produce a change in the polarity control line during one frame of N frames. For example, if the A word invert store is active, one frame in N frames when the A word enable occurs, the polarity control line will change state. This inverts the data output on the Simulator 1 card.

In the invert all words store is active, an entire frame of data is inverted every N frames.

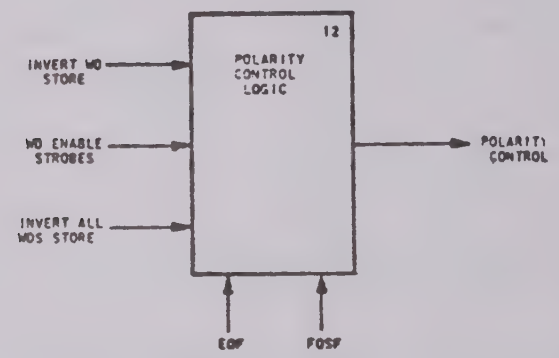


Figure 4-52. Polarity Control Logic (Card 2)

4.6.11 Data Merging, Code Conversion and Output Amplifier (Figure 4-53)

The serial data stream from the parallel-to-serial converter, the serial pseudo-random data and the serial ID output are merged into a single data stream by the mux logic. When the ENAB H WD and EN SER ID are not active, the serial data is being placed on the mux output. When ENAB H WD goes active, the pseudo-random stream is placed on the mux output and when EN SER ID goes active, the serial ID word is placed on the mux output.

This output is NRZ-L data. The simulator can provide NRZ-L, NRZ-M, NRZ-S, RZ, Biø-L, Biø-M, Biø-S, DM-M, or DM-S, all under program control. The code converter performs this function. The NRZ-L output from the converter is buffered and sent to the frame synchronizer (the frame sync only accepts NRZ-L data). The serial PCM which is in the code

selected by the PCM CODE, stores goes to two line drivers which can drive 100Ω impedances at TTL levels. One drives the internal bit synchronizer and the other is routed to the rear panel (PCM2). The serial PCM is also routed to an output amplifier through the data blanking logic. This output (PCM1) is adjustable (on card) to provide 0 to 1 volt rms amplitude and ±100% baseline offset. The data enable input (TTL level) to the rear panel provides a means of blanking the PCM1 output. When blanked, the PCM1 output is clamped to baseline level. Noise can be summed into the output amplifier from a rear-panel connector.

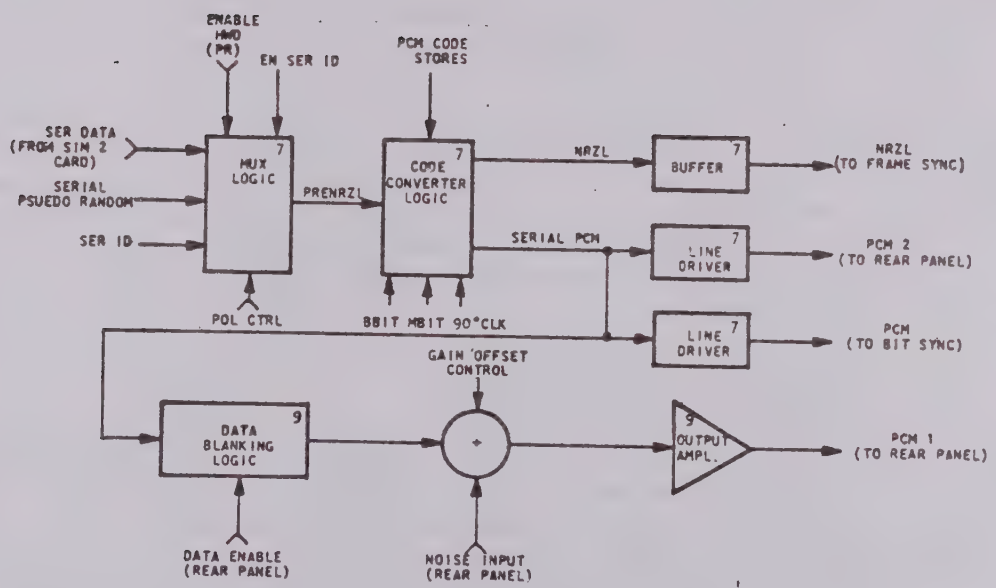


Figure 4-53. Data Merging, Code Conversion and Output Amplifier Circuits (Card 1)

4.7 VARIABLE WORD LENGTH CARD

4.7.1 GENERAL

Formats with variable word lengths (VWL) in the range of three to 16 bits per word and frame lengths up to 2048 words can be handled. A 2048 word x 6 bit random access memory (RAM) is added to the decommutator on an optional basis. To accept VWL, three standard instructions must be loaded for each VWL position in the format. Two of these words contain the word number at which the VWL occurs, and the third contains the actual length of the word. The contents of the VWL RAM may be displayed on the front panel by loading the RAM address (Instructions 0-0 and 0-1) and then addressing Instruction 0-2. The programmed length for that word (and the PDD bit, see below) will be displayed as PRESENT DATA on the front panel.

A programmable data distribution (PDD) capability is provided as part of the VWL hardware. This function allows for the programming of all the words in a frame which are to be output or which are to be deleted from the output. Using an additional bit of the VWL RAM (therefore using the same loading and verification method as described above), each word has the capability of being deleted from or sent to a second output port. A setup bit (Instruction 1-23) determines whether the dynamic RAM PDD bits are to be interpreted as "enable output" or "delete from output" each time the RAM is addressed. This function can be applied to any of the 2048 words addressable by the RAM; from the time of master RAM clearing, only those words selected for PDD action (output or no output) need be programmed.

4.7.2 Block Diagram Description (Figure 4-54)

The variable word length memory must be cleared whenever a new VWL program is to be loaded. This is accomplished by either a Power-On Reset or by a programmed clear (Memory Address 1, Function Address 31, Bit 4=1). The clear pulse sets both an Enable Clear Flip-Flop and an Inhibit Flip-Flop in the control logic circuits (Refer to sheet 7 of Figure 34307 in Section 6). With the Inhibit Flip-Flop set, the 710 is forced to the search mode. This prevents erroneous output data during the VWL clear and load cycles. The Enable Clear Flip-Flop enables grounded inputs to the Memory Data Switch and enables the Clear Oscillator in the Control Logic. The oscillator provides the memory address counter clock pulses and the memory write pulses during the clear cycle. The memory address counter, which is reset at the start of the clear cycle, is incremented through its total capacity (2047) by the clock pulses. Each count enables a corresponding memory location causing logic zero levels to be loaded into the memory locations. Stepping the address counter to a count of 2048 produces a pulse which resets the Enable Flip-Flop. This in turn inhibits the oscillator circuit and prepares the VWL Card for a load cycle.

The data address decoder and buffers decode the three instructions associated with each variable word length parameter. The first instruction (MA0, DA0) causes the two most significant BCD values (thousands and hundreds) to be loaded into the word location stores.

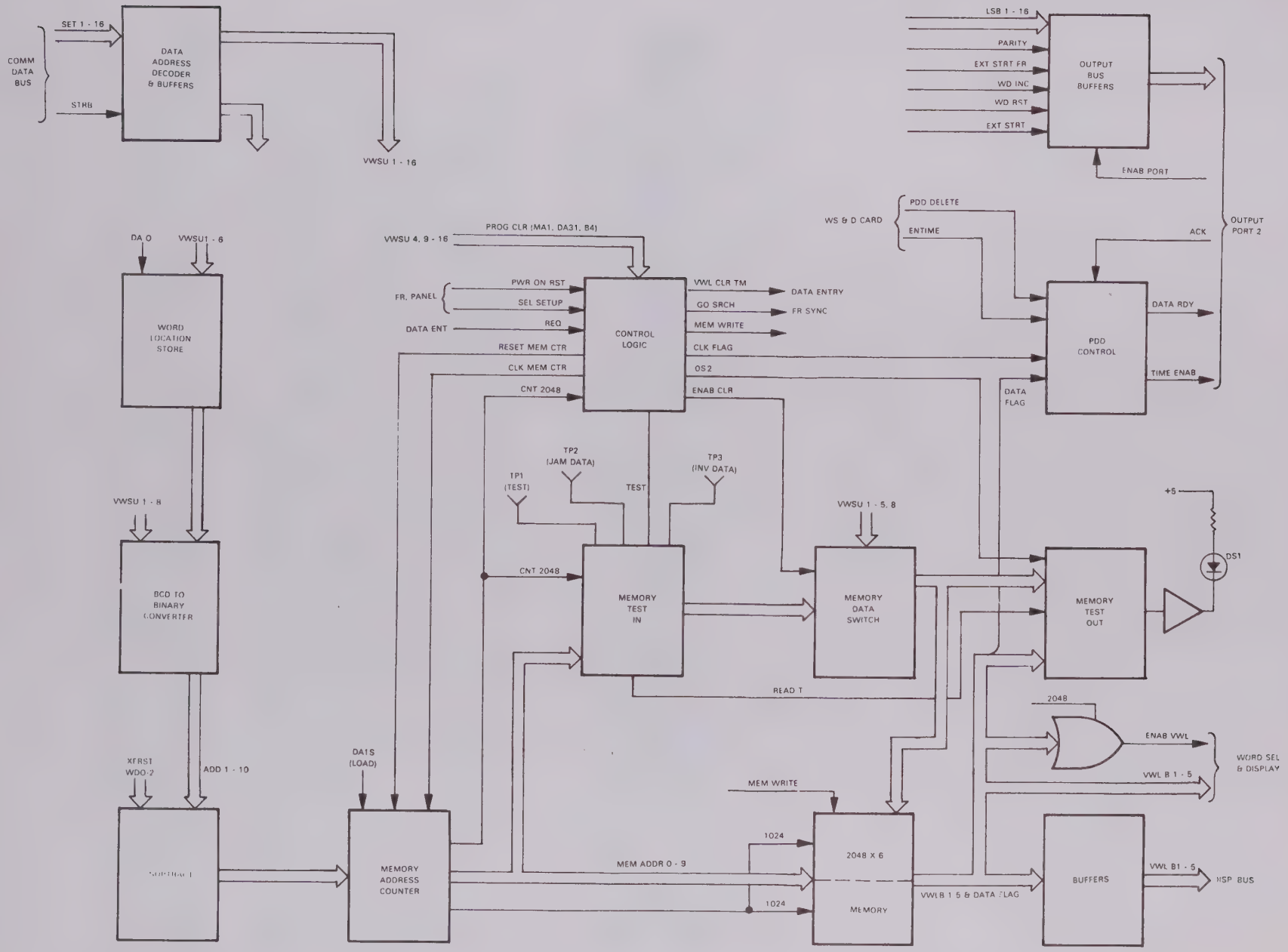


Figure 4-54 Variable Word Length Card Block Diagram

NOTE

Since the maximum word location number is 2048 only the two least significant bits of the thousands BCD value are stored.

The stored BCD values are applied to a BCD-to-binary converter together with the units and tens BCD values in the second VWL instruction. The resultant eleven-bit binary value representing the programmed word location of a variable length word is applied to a subtractor circuit. The subtractor subtracts the stored first word number (MA1, DA22, Bits 4-7) from the binary word location. This is done so that the total memory capacity, 2048 words, may be utilized.

NOTE

The first word number (1 ST WD NR) must be programmed before the VWL memory is loaded.

The output of the subtractor is loaded into the memory address counter by the trailing edge of the Data Address 1 pulse (DA1S). The stored location enables a corresponding location in the random access memory. The data values of the third VWL instruction (VWSU 1-5, 8) which represent the VWL bit length and the PDD bit, are coupled through the memory data switch (D1-5, D8) and loaded into the enabled memory location by Data Address 2 (DA2S) pulse. The bits per word count for each variable length word in the VWL program format are loaded into the programmed memory locations. The last DA2 pulse in a program loading cycle resets the inhibit flip-flop in the control logic thereby allowing the 710 to advance to the lock mode.

During normal system operation the memory address counter is reset at the end of each frame by CN+1 and is incremented by BN word rate pulse. Each count enables a corresponding location in the 2048 RAM memory. The bit values in the enabled memory location (word length for that location) are applied to the program word length selector on the word select and display card and to a bit detection gate. This gate monitors the five word length bit position in each memory location and generates a $\overline{\text{ENAB VWL}}$ pulse whenever a 1-bit is detected in a memory location. The $\overline{\text{ENAB VWL}}$ pulse causes the VWL value to be used as the word length in the word rate time timing Logic (refer to paragraph 4.3.4) If the words per frame exceed the memory capacity the $\overline{\text{ENAB VWL}}$ is inhibited by the address counter exceeding a count of 2048.

The VWL Card contains circuits for performing a test of the RAM memory. When this feature is exercised a pattern of test data is loaded into each memory location during the load cycle. The memory is then read and compared to the pattern. A difference between the memory output and the test pattern causes LED indicator DS1 to light. The memory test procedure is outlined in paragraph 5.2.5 .

MAINTENANCE

SECTION 5

MAINTENANCE

5.1 GENERAL

This section contains information to aid in troubleshooting and repairing the Model 710 PCM Decommutator. This information is intended to supplement the theory of operation descriptions contained in Section 4, so that isolation and repair of a malfunction can be performed with maximum efficiency. Included in this information are a trouble shooting guide, visual and operational checkout procedures and system timing diagrams.

5.2 TROUBLE SHOOTING

In the event an abnormal condition is detected in the Model 710 the following general method of isolating the trouble is recommended:

a. Verify the physical and programming setup of the 710 as outlined in Section 3, Installation and Operation.

b. Perform a visual inspection (paragraph 5.2.2).

c. Perform an operational checkout procedure (paragraph 5.2.3).

d. If erroneous indications are obtained during the checkout procedure, isolate the source of the failure using the circuit descriptions provided in Section 4 and the 710 schematic, assembly and wiring diagrams (Section 6).

e. When a defective component is located, refer to Section 6, Parts Lists, for replacement information.

f. Repeat the procedure used to isolate a malfunction to verify that it has been corrected.

5.2.1 Special Tools and Test Equipment

Two extender cards are provided with the Model 710 for extension of printed wiring board assemblies from the main chassis for test and maintenance procedures. The individual extender cards are identified as follows:

Assembly	Assy. No.	Purpose
Full Width Extender Printed Wiring Assy.	33118	Extends Frame Sync Word Select and Display Subframe Sync., or Simulator Cards.
Single Wide Extender Printed Wiring Assy.	34617	Extends Data Entry Card and Variable Word Length Card

The following standard test equipment is recommended for checkout of the Model 710:

Equipment	Model
Oscilloscope	Tektronix 475
DVM	DCT 370
VOM	Simpson 260
Card Reader	HP 11310A
Noise Generator	Elgenco 610A
Frequency Counter	HP 5300A
Function Generator	HP 3310A
DC Source	MV IDON
Binary Display	EMR 2757 (Modified)

5.2.2 Visual Inspection

The Model 710 should be subjected to a regular inspection program similar to that recommended for other types of electronic equipment. The following inspection should be performed periodically as a means of preventive maintenance or, if a malfunction occurs, to aid in isolation of the trouble.

a. Inspect front and rear panel components for signs of damage

b. Inspect printed-circuit cards and mating connectors for mechanical damage or component discoloration.

c. Inspect wiring for loose or broken connections.

5.2.3 Power Circuits Checkout Procedures

CAUTION

Remove AC power from the 710 whenever removing or installing printed-circuit cards. Failure to do so may result in card damage.

a. Verify an open circuit between signal ground and chassis ground on the rear panel.

b. With all cards removed from the 710, apply AC power. Using a DVM verify DC voltages at the following points: (Refer to Drawing 32945, Power Wiring Diagram, in Section 6 as a troubleshooting aid.)

NOTE

The ±15 VDC levels are produced by ±15 VDC Power Supply PS2 and are present only when the Simulator option is contained in the 710.

Connector No.	Digital Grd.	+5V	+15V	-15V
J5	1, 51	2, 52		
J6	50, 100	49, 99		
J7	1, 51	2, 52		
J8	50, 100	49, 99		
J9	1, 51	2, 52	3, 53	4, 54
J10	50, 100	49, 99	48, 98	47, 97
J11	1, 51	2, 52		
J12	50, 100	49, 99		
J13	1, 51	2, 52		
J14	50, 100	49, 99		
J16	61, 126	60, 125		

Information pertaining to +5VDC Power Supply PS1 (Powertec Model 9E5-50C-17) is provided in Appendix A of this manual. Schematic and assembly diagrams and the parts list for ±15V Power Supply PS2 are contained in Section 6.

5.2.4 Operational Checkout Procedures

Operational checks for the Model 710 consist of the program setup verification procedure, paragraph 3.2.2.2, for verification of the program setup circuits and the word selection and display procedure, paragraph 3.2.2.3, for comparison of a selected PCM output word to a corresponding known PCM input word. Since during normal operation most input word values, except for sync words, are unknown or variable, a sample program is given in Figure 5-1. This sample program provides for exercising the 710 with known data values. Figure 5-2 illustrates the punched card format for the sample program.

To checkout the 710 using the sample program proceed as follows:

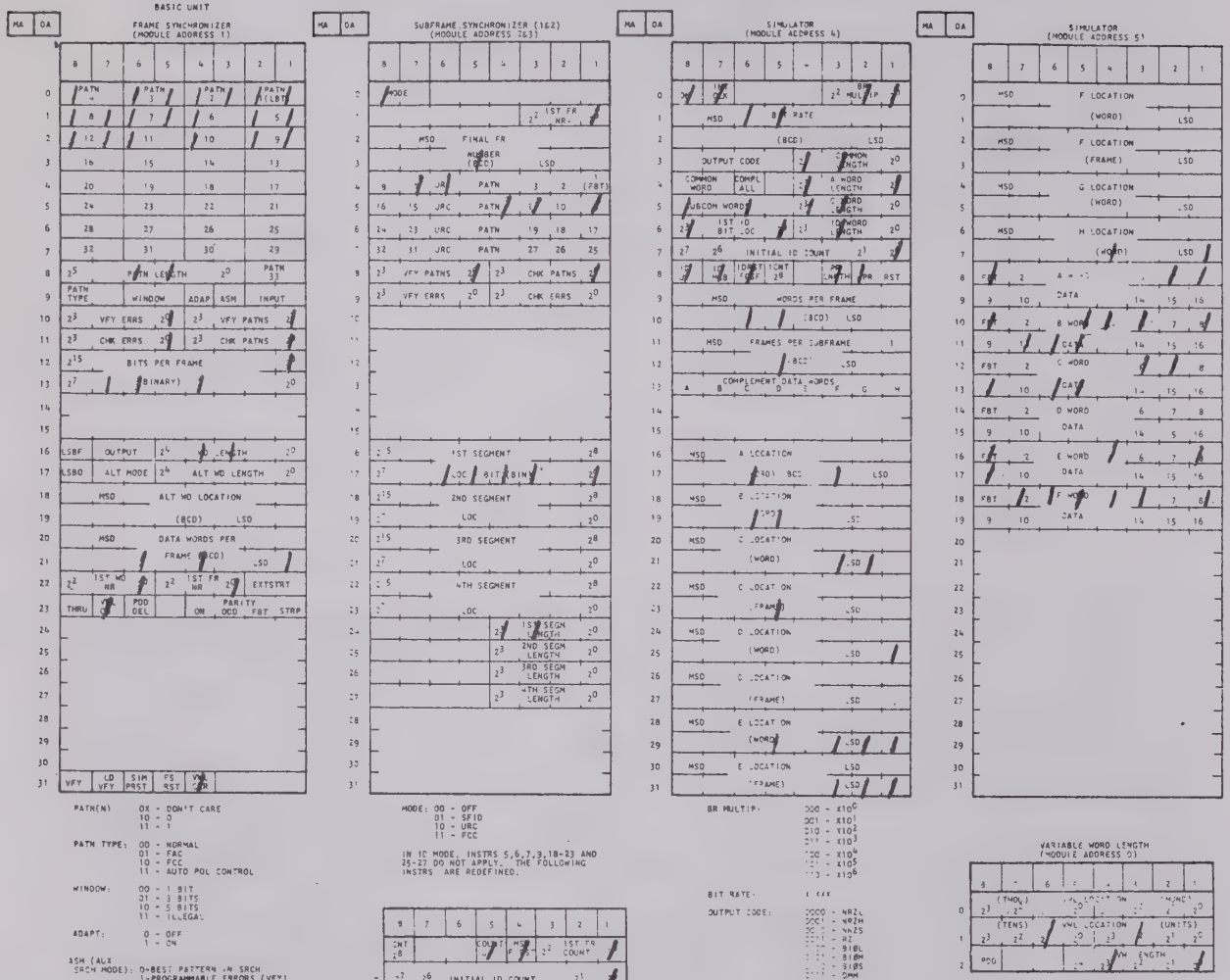
a. On the front panel place the INPUT SOURCE FRAME SYNC switch in the SIML mode.

b. Load the sample program either manually (paragraph 3.2.2.1) or using prepunched program cards (paragraph 3.2.4).

c. Verify the program setup (paragraph 3.2.2.2) and reprogram any erroneous instructions.

d. If reprogramming does not correct error indications refer to the applicable schematics in Section 6 and troubleshoot the program setup circuits.

(Module Address Assigned on a System Basis)



PATN(N): 0X - DON'T CARE
10 - 0
11 - 1

PATN TYPE: 00 - NORMAL
01 - FAC
10 - FCC
11 - AUTO POL CONTROL

WINDOW: 00 - 1 BIT
01 - 3 BITS
10 - 5 BITS
11 - ILLEGAL

ADAPT: 0 - OFF
1 - ON

ASM (ALT SRCH MODE): 0-BEST PATTERN IN SRCH
1-PROGRAMMABLE ERRORS (VFY)

LSBF: 0 - INPUT MSB FIRST
1 - INPUT LSB FIRST

LSBO: 0 - OUTPUT MSB ALIGNED
1 - OUTPUT LSB ALIGNED

OUTPUT: 00 - DATA ONLY
01 - FS PATN
10 - STATUS

ALT MODE: 00 - NO ALT LNGTH
01 - ONE ALT LNGTH
10 - REPEATING ALT LNGTH WORDS. IN THIS MODE, INSTR NR '8 INDICATES HOW OFTEN THE ALT LNGTH REPEATS, AND INSTR NR '9 INDICATES WHERE THE ALT LNGTH STARTS BOTH IN BCD.

ERT STRT: 00 - FR RATE EXTERNAL START
01 - SF1 RATE EXTERNAL START
10 - SF2 RATE EXTERNAL START
11 - NO EXTERNAL START

THRU: 1-THRUPUT MODE ON (SER-TO-PAR CONVERSION WITHOUT SYNC)

VWL ON: 1-VWL OPTION ENABLED

PDD DEL: PDD DELETE. USED WITH PDD (MA 0, DA 2) AS FOLLOWS:

PDD	PDD DEL	PORT 2 PARALLEL DATA OUTPUT
0	0	WORD DELETED
0	1	WORD OUTPUT
1	0	WORD OUTPUT
1	1	WORD DELETED

PARITY ON: 1-PARITY ON, CHECK FOR ERRORS
0-PARITY OFF, GENERATE PARITY BIT

PARITY ODD: 1-ODD PARITY
0-EVEN PARITY

PARITY EBT: 1-PARITY TRANSMITTED FIRST
0-PARITY TRANSMITTED LAST

PARITY STRP: 1-STRIP PARITY BIT FROM THE PARALLEL DATA OUTPUT
0-OUTPUT PARITY BIT WITH DATA WORD

MODE: 00 - OFF
01 - SFID
10 - URC
11 - FCC

IN IC MODE, INSTRS 5,6,7,9,18-23 AND 25-27 DO NOT APPLY. THE FOLLOWING INSTRS ARE REDEFINED.

INSTR	
0	MODE
1	1ST FR NR
2	MSD FINAL FR NUMBER (BCD) LSD
4	JR PATN 3 2 (FBT)
5	JRC PATN 19 18 17
6	JRC PATN 27 26 25
8	VFY PATNS, CHK PATNS
9	VFY ERRS, CHK ERRS
16	1ST SEGMENT LOC
17	1ST SEG BIN
18	2ND SEGMENT LOC
20	3RD SEGMENT LOC
22	4TH SEGMENT LOC
24	1ST SEGM LENGTH
25	2ND SEGM LENGTH
26	3RD SEGM LENGTH
27	4TH SEGM LENGTH

INSTR	
0	INIT FR CK
1	MSD BIT RATE
2	(BCD) LSD
3	OUTPUT CODE, COMMON LENGTH
4	COMMON WORD, COMPL ALL, A WORD LENGTH
5	SUBCOM WORD, B WORD LENGTH
6	1ST ID BIT LOC, ID WORD LENGTH
7	INITIAL ID COUNT
8	IDENT CONT, ID RST EOSF, PR LENGTH, PR RST
9	MSD WORDS PER FRAME
10	(BCD) LSD
11	MSD FRAMES PER SUBFRAME
12	(BCD) LSD
13	COMPLEMENT DATA WORDS A B C D E F G H
16	MSD A LOCATION
17	(WORD) BCD LSD
18	MSD B LOCATION
19	(WORD) LSD
20	MSD C LOCATION
21	(WORD) LSD
22	MSD C LOCATION
23	(FRAME) LSD
24	MSD D LOCATION
25	(WORD) LSD
26	MSD D LOCATION
27	(FRAME) LSD
28	MSD E LOCATION
29	(WORD) LSD
30	MSD E LOCATION
31	(FRAME) LSD

BR MULTIP: 000 - $x10^0$
001 - $x10^1$
010 - $x10^2$
011 - $x10^3$
100 - $x10^4$
101 - $x10^5$
110 - $x10^6$

BIT RATE: BCD

OUTPUT CODE: 0000 - NRZL
0001 - NRZM
0010 - NRZS
0011 - RZ
0100 - BIOL
0101 - BIOM
0110 - BIOS
0111 - DMM
1000 - DMS

COMMON WORD: 00 - E WORD
01 - G WORD
10 - H WORD

COMPL ALL: 1 - ALL WORDS COMPLEMENT EVERY N FRAMES FOR N FRAMES DURATION

SUBCOM WORDS: 0000 - NO SUBCOM
0010 - C WD S/C
0100 - D WD S/C
0110 - E WD S/C
1000 - F WD S/C

ID RST EOSF: 0 - NO RST ON ID
1 - RST ID AT END OF SUBFRAME

PR LENGTH: 0 - 11 BIT GENERATOR
1 - 16 BIT GENERATOR

PR PRESET: 00 - NO PRST
01 - PRST AT END OF FRAME
11 - PRST AT END OF SUBFRAME

COMPL DATA WDS: 0 - NO COMPLEMENT
1 - COMPLEMENT RESPECTIVE DATA WORDS ONE FRAME EVERY N FRAMES

INSTR	
0	SUBFR CNT 28, COUNT MSB, 1ST FR COUNT
1	INITIAL ID COUNT
16	1ST ID PATN BIT
17	LOCATION (BIN)
24	ID PATN LENGTH

* VFY: 0 - NORMAL (NO VERIFY)
1 - VERIFY. SETUP STORES ON DATA OUTPUT BUS

* LD VFY: 0 - NORMAL
1 - STORES LOADED AND VERIFIED ON DATA BUS

*SIM PRST 0 - NO ACTION
1 - RESET SIM

*FS RST 0 - NO ACTION
1 - RESET FS

VWL CLR 1-CAUSES VWL PAM TO BE CLEARED (REQ'D PRIOR TO VWL SETUP). GENERATES PULSE ONLY-CANNOT BE EXAMINED.

**INPUT 00 - EXT 1
01 - EXT 2
10 - EXT 3
11 - INT SIM

*THESE BITS CANNOT BE EXAMINED / A FRONT PANEL OR MTA COMPUTER AND CAN BE LOADED ONLY BY THE COMPUTER.

**WHEN PROGRAMMING SETUP MODE - CONTROL OF THE LOCAL OR STEP POSITION INPUT TELEMETRY ON IS CONTROLLED DIRECTLY FROM THE FRONT PANEL INPUT SOURCE SWITCHES

VARIABLE WORD LENGTH (MODULE ADDRESS 0)

	8	7	6	5	4	3	2	1
0	(TWOS) VWL LOCATION ON (UNITS)							
1	(TENS) VWL LOCATION (UNITS)							
2	PDD				VW LENGTH			

*VWL LOCATION - BCD LOCATION OF VWL POSITION TO BE LOADED

VW LENGTH - BINARY VALUE OF VWL

PDD - (SEE PDD DEL BIT IN MA1, DA23)

(NOTE: WHEN USING CARD READER, INSTRUCTIONS 0-2 MAY BE REPEATED UP TO 10 TIMES ON ONE PROGRAMMING CARD)

*CANNOT BE DISPLAYED OR COMPUTER VERIFIED.

MA=MODULE ADDRESS (3 B TS), E.G., FR SYNC = 001, SF SYNC #2 = 010, SIMULATOR = 100, ETC

DA=DEVICE (OR GROUP) ADDRESS (5 B TS)

Figure 5-1. Program Sample No. 1 (Sheet 1 of 2).

PROGRAMMER: _____ DATE: _____

FORMAT WORKSHEET

PROGRAM: SAMPLE # 1
BIT RATE: 3.000
BIT RATE MULT: X 10^3
OUTPUT CODE: NRZL
WORD SIZE: 12-BITS

DATA ALIGN: MSB FIRST
DATA WDS/FR: 29
SUBCOM WDS/FR: 10:1-6 (URC)
10:1-17 (ID)
VWL - WORD 24 - 9 BITS

SIMULATOR (MA 4 & 5):

FUNCTION	SLM WD	WORD WD	LOCATION FR	BINARY DATA 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	FBT 1
VWL	A	24	-	-	-	-	-	-	-	-	0	1	1	0	0	0	0	0	1
FR SYNC	B	30	-	-	-	-	-	1	1	1	0	1	0	1	1	1	0	0	1
SF SYNC	C	6	10	-	-	-	-	1	1	0	1	0	1	1	0	0	0	0	0
ID	D	1	-	-	-	-	-	X	X	X	X	-	-	-	-	-	-	-	-
UNIQUE (SF2)	E	17	7	-	-	-	-	0	0	0	1	1	0	0	1	0	0	0	1
COMMON	F	-	-	-	-	-	-	0	0	0	0	1	0	1	1	1	1	1	0
--	G	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PR (MAIN)	H	9	-	-	-	-	-	P	S	E	U	D	O	R	A	N	D	O	M

MAIN FRAME (MA 1):
FIRST WD #: 1
BITS/FR: 357
ALT/WD: NONE

SF #1 (MA 2):
MODE: URO
FIRST FR #: 1
LAST FR #: 10

SF #2 (MA 3):
MODE: ID
FIRST FR #: 1
LAST FR #: 10

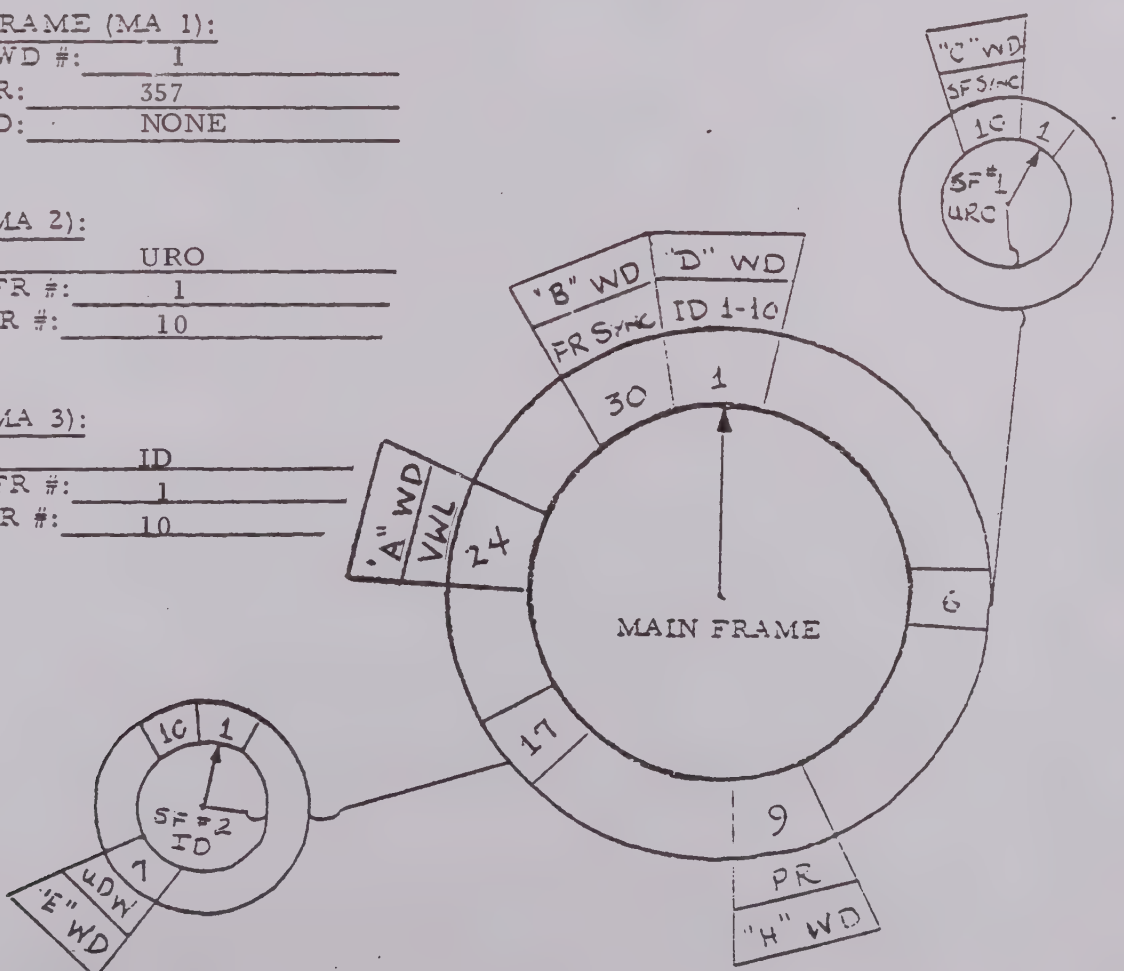


Figure 5-1. Program Sample No. 1 (sheet 2 of 2).

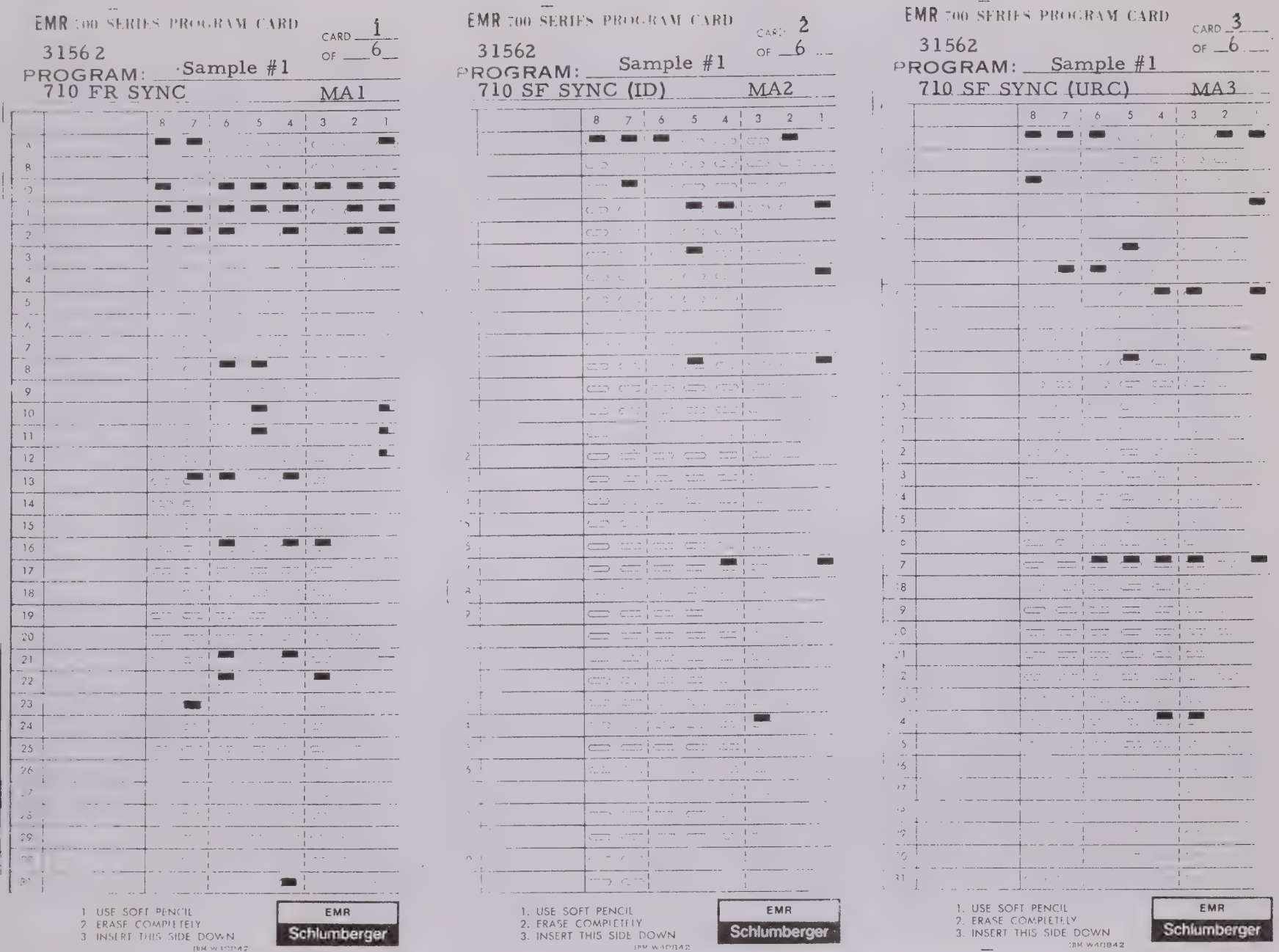


Figure 5-2 (Sheet 1 of 2). Program #1 Prepunched Card Format

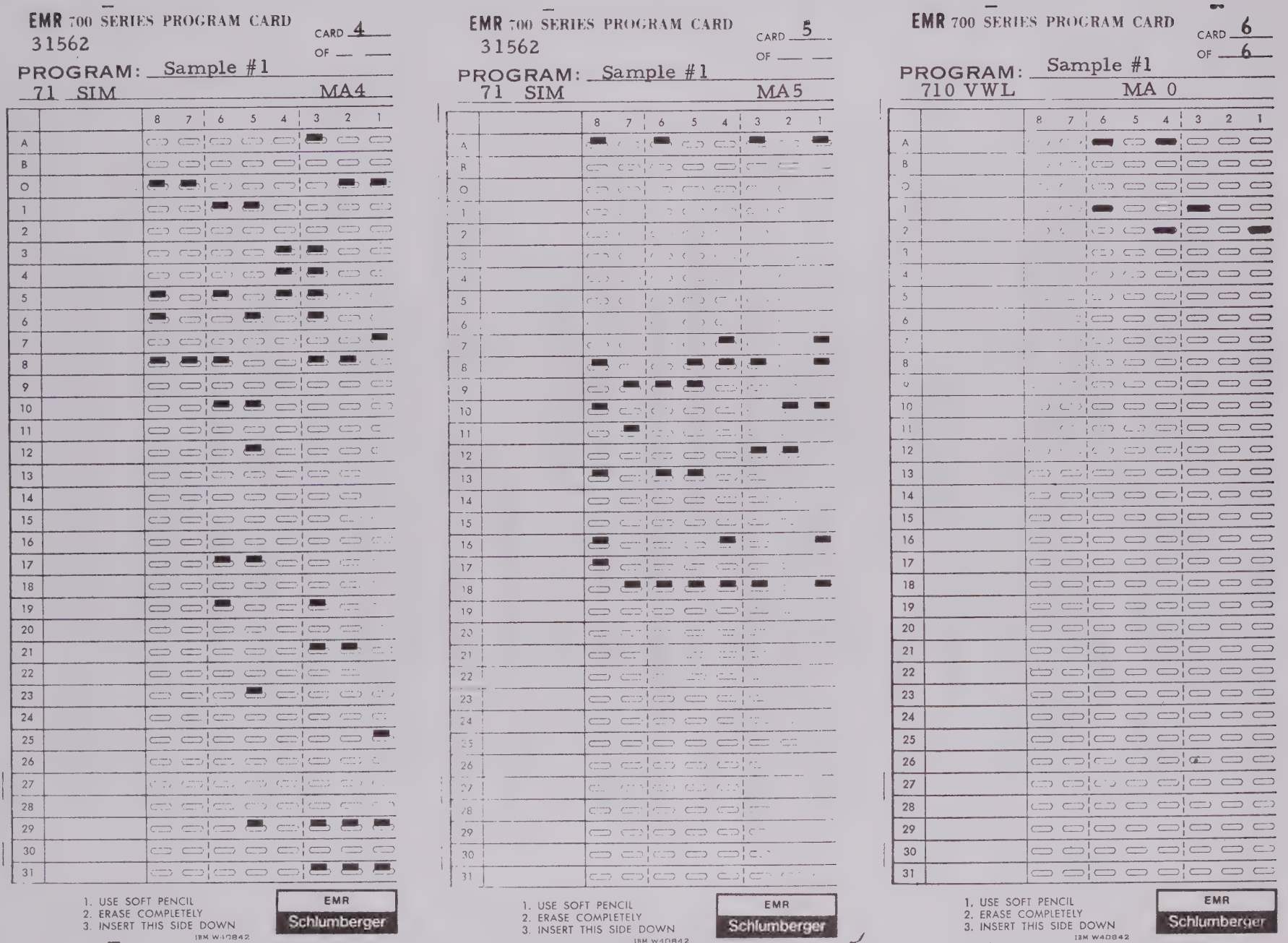


Figure 5-2 (Sheet 2 of 2). Program Sample #1 Prepunched Card Format

e. Using the word select and display procedure (paragraph 3.2.2.3) select output words for display on the front panel indicators and compare indications to known values from the sample program format. If errors occur refer to the appropriate circuits on the schematic diagrams and isolate the failure using standard troubleshooting procedures.

Test points are provided on the front panel for monitoring of primary input and output control signals of the Model 710. (Refer to Figure 3-2 and Table 3-2). Secondary test points are provided on the individual printed-circuit cards for monitoring internal timing and control signals. These test points provide a troubleshooting aid in localizing a failure to a specific circuit or component.

An additional maintenance aid to be used in conjunction with the operational checkout procedures are the 710 timing diagrams. These timing diagrams are identified as follows:

Figure 5-3 Simulator Word Selection Timing

Figure 5-4 Simulator ID Word Timing

Figure 5-5 Simulator Pseudo-Random Timing

Figure 5-6 Simulator Data Inversion Control Timing

Figure 5-7 Frame Sync Correlation Timing

Figure 5-8 Frame Sync Best Pattern Srch ⟶ Vfy.

Figure 5-9 Frame Sync Auto Polarity Control

Figure 5-10 Frame Sync Bit Slip

Figure 5-11 Frame Sync Error Accumulator and Display

Figure 5-12 Subframe Sync Recycle Correlation

Figure 5-13 Subframe Sync ID (LSB First) Correlation

Figure 5-14 Subframe Sync ID (MSB First) Correlation

Figure 5-15 Subframe Sync Recycle Mode Timing

Figure 5-16 Subframe Sync ID Mode Timing

Figure 5-17 Word Select and Display Output Timing (Data Only Output)

Figure 5-18 Word Select and Display Output Timing (Frame Sync Pattern Output)

Figure 5-19. Word Select and Display Output Timing (Status Word Output)

Figure 5-20. Word Selection and Display Timing

Figure 5-21. Variable Word Length and Parity Timing

Figure 5-22. Output Timing Diagram

5.2.5 Variable Word Length Memory Checkout Procedure

To check the variable word length memory locations proceed as follows:

a. Remove power from the 710.

b. Install the Variable Word Length Card on a Single Wide Extender PWA (Assy. No. 34617) and reapply power to the unit.

c. Ground test point TP1 on the VWL Card.

d. Jumper test point TP3 to TP4.

e. On the front panel, program a VWL CLR. (MA1, DA31, Bit 4=1).

f. Verify that LED indicator DS1 on the VWL Card is off.

g. Move the jumper from TP4 to TP5.

h. Repeat steps e and f.

i. Interchange the jumper boards in locations ZA1 and ZB1 on the VWL Card.

j. Move jumper from TP5 to TP4.

k. Repeat steps e thru h.

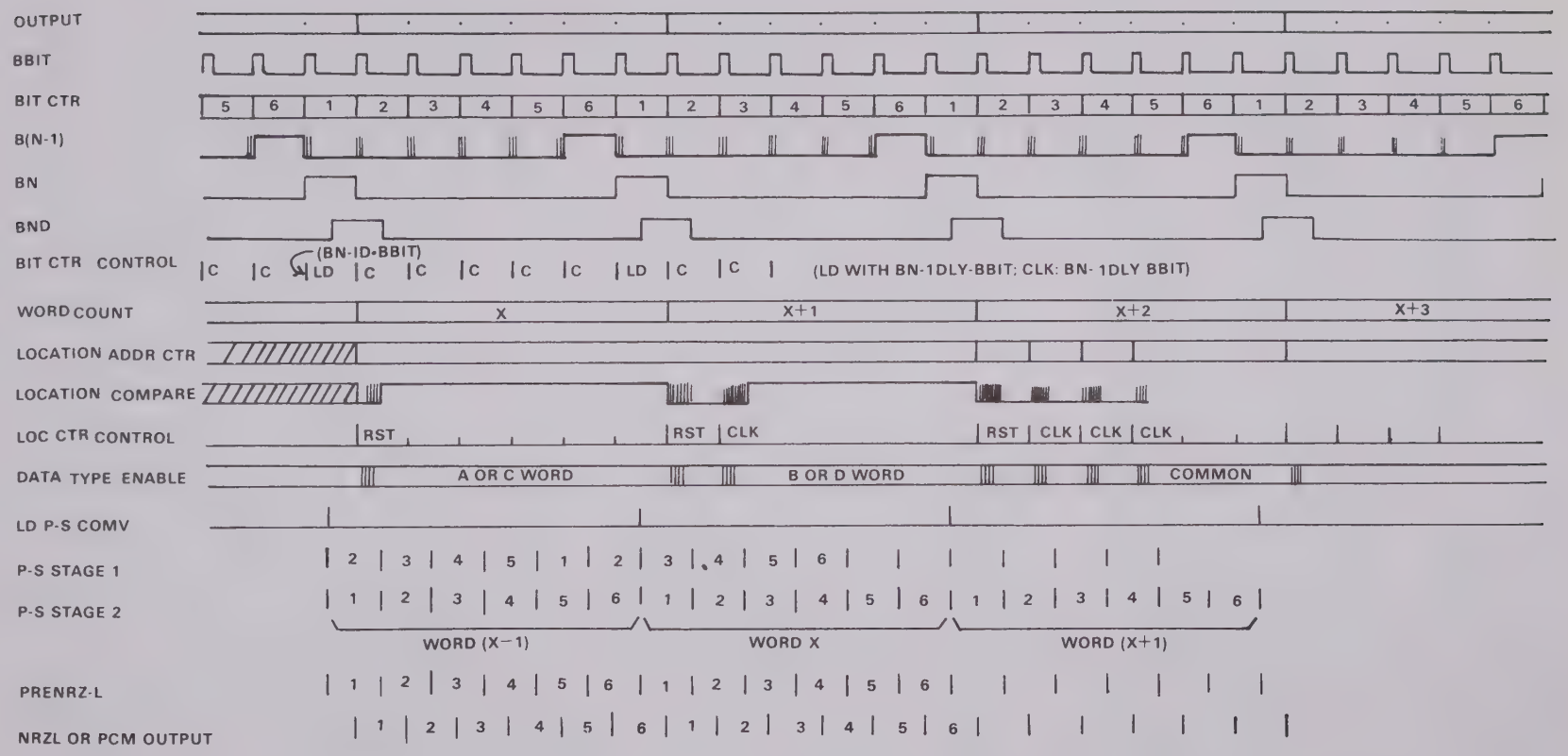


Figure 5-3. Simulator Word Selection Timing.

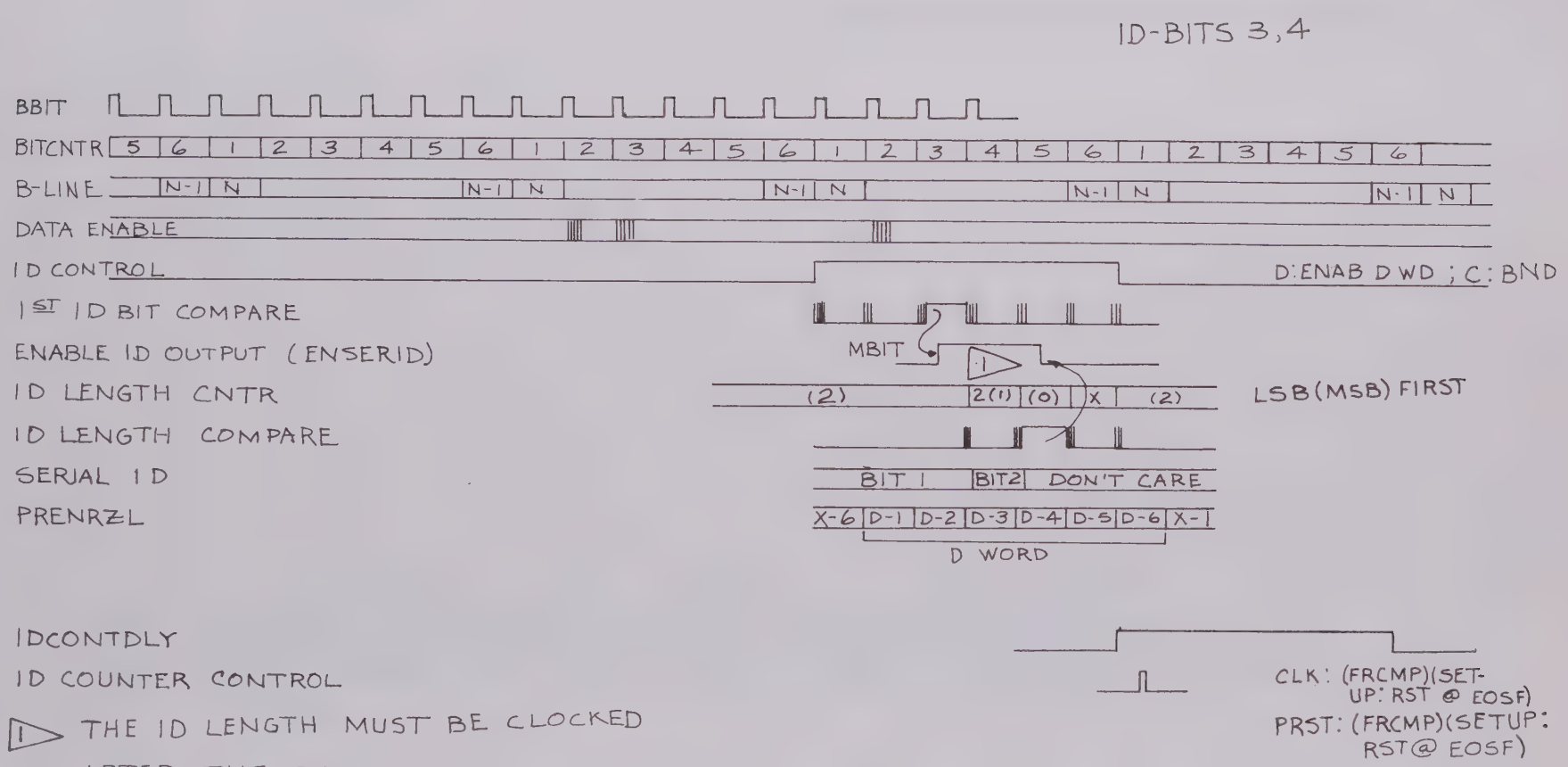


Figure 5-4. Simulator ID Word Timing.

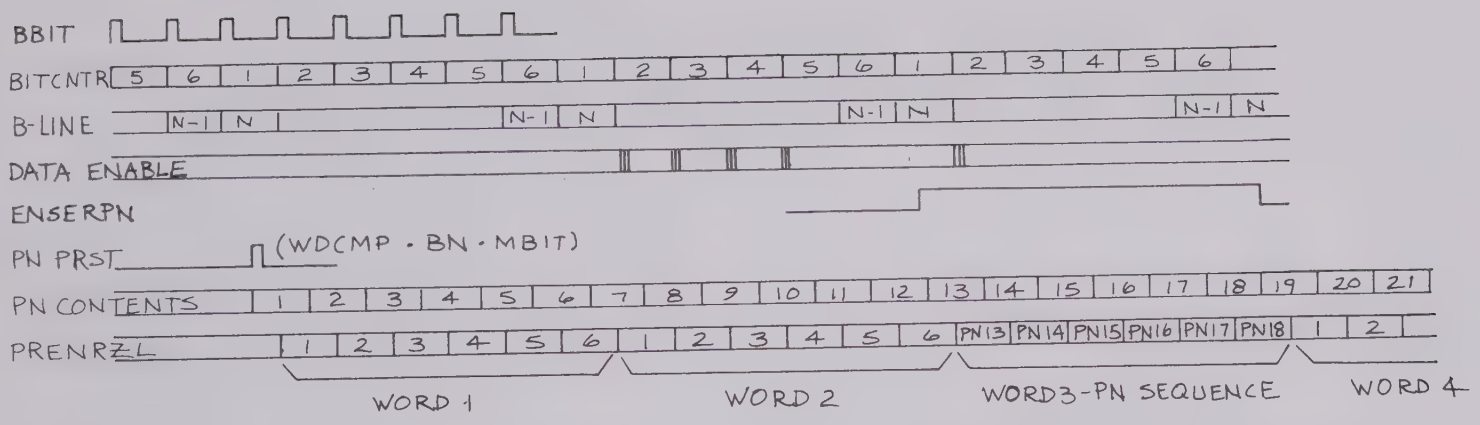


Figure 5-5. Simulator Pseudo-Random Timing.

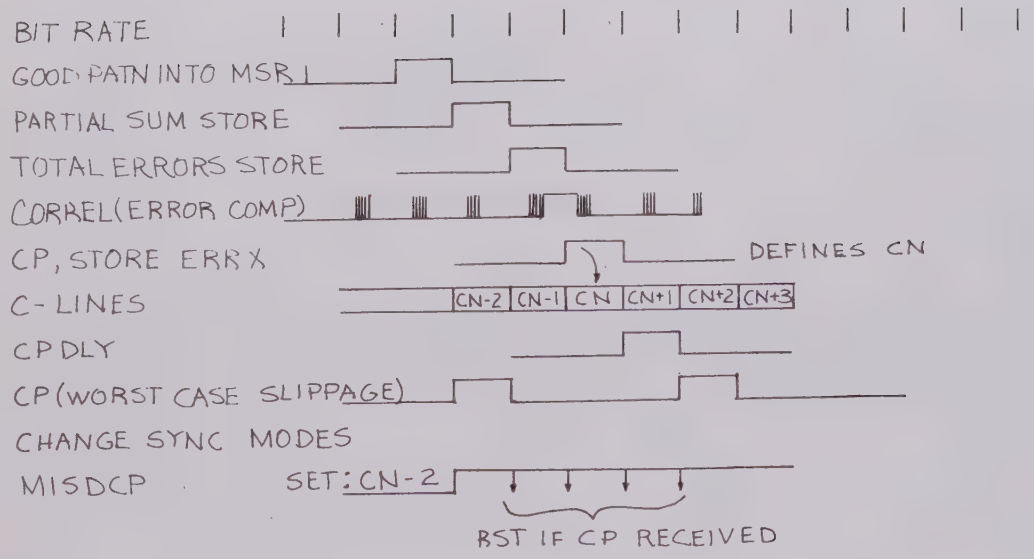
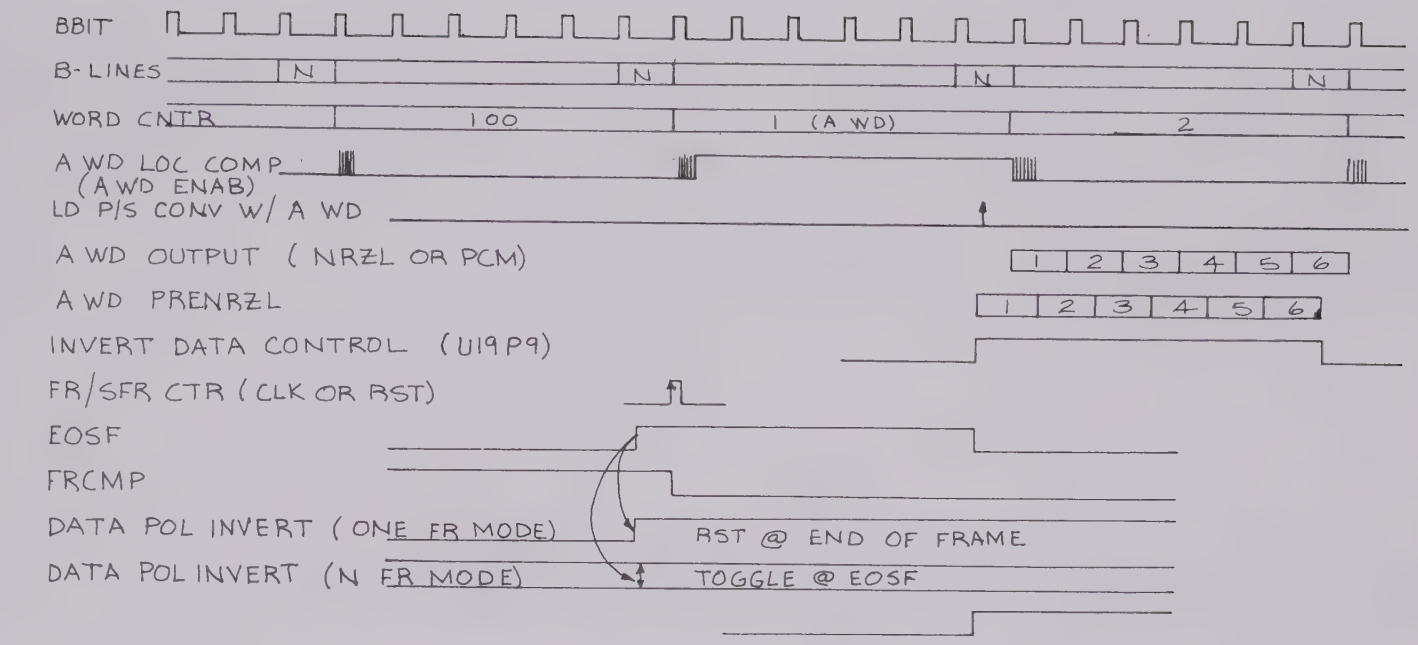


Figure 5-7. Frame Sync Correlation Timing.



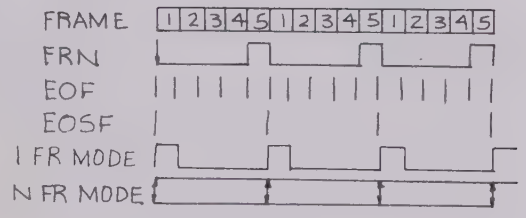


figure 5-6. Simulator Data Inversion Control Timing.

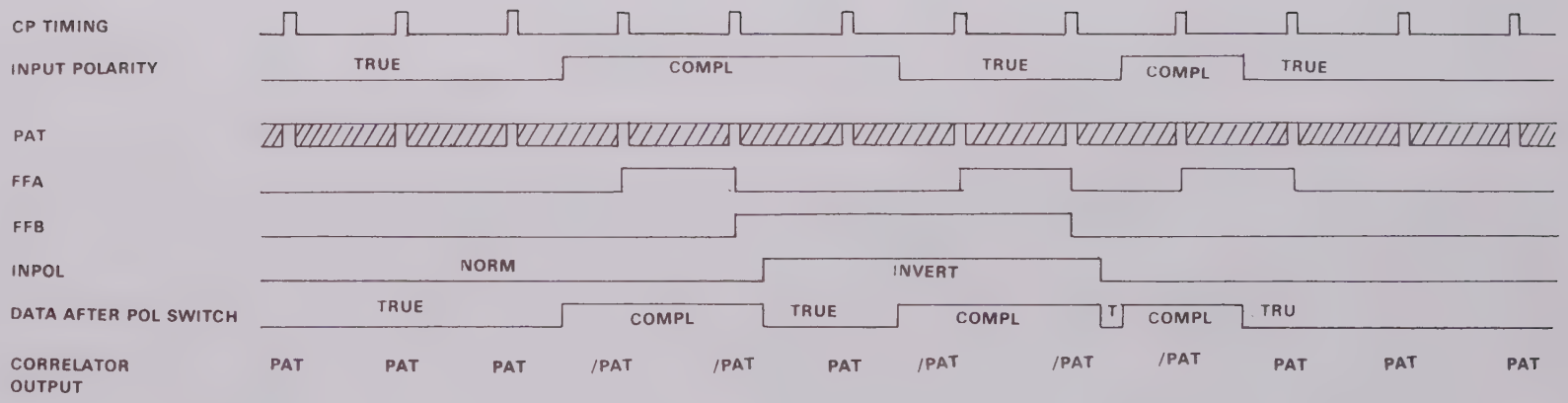
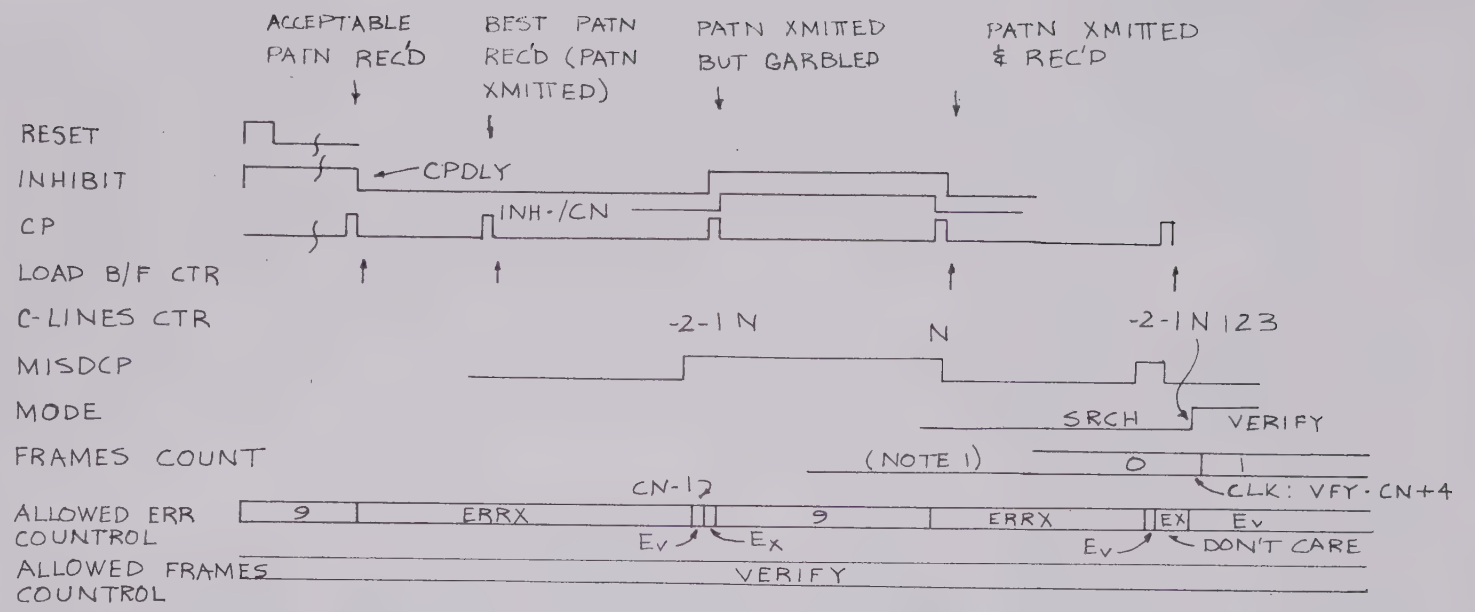


FIGURE 5-9. FRAME SYNC AUTO POLARITY CONTROL



NOTE 1: IF PROGRAMMING IS $F_V = 0$, FRSMAX = 1
DURING SRCH DUE TO GATING OF F_V DURING SRCH.
THIS ALLOWS DIRECT XFER FROM SRCH → LOCK.

NOTE 2: COMPLETE ERROR SWITCH GATING IS: 9 - INHIBIT
EC - CHK & LOCK
E_V - (SRCH · CN-1) + VFY
E_X - SRCH · /INH · /CN-1

Figure 5-8. Frame Sync Best Pattern Srch → Vfy.

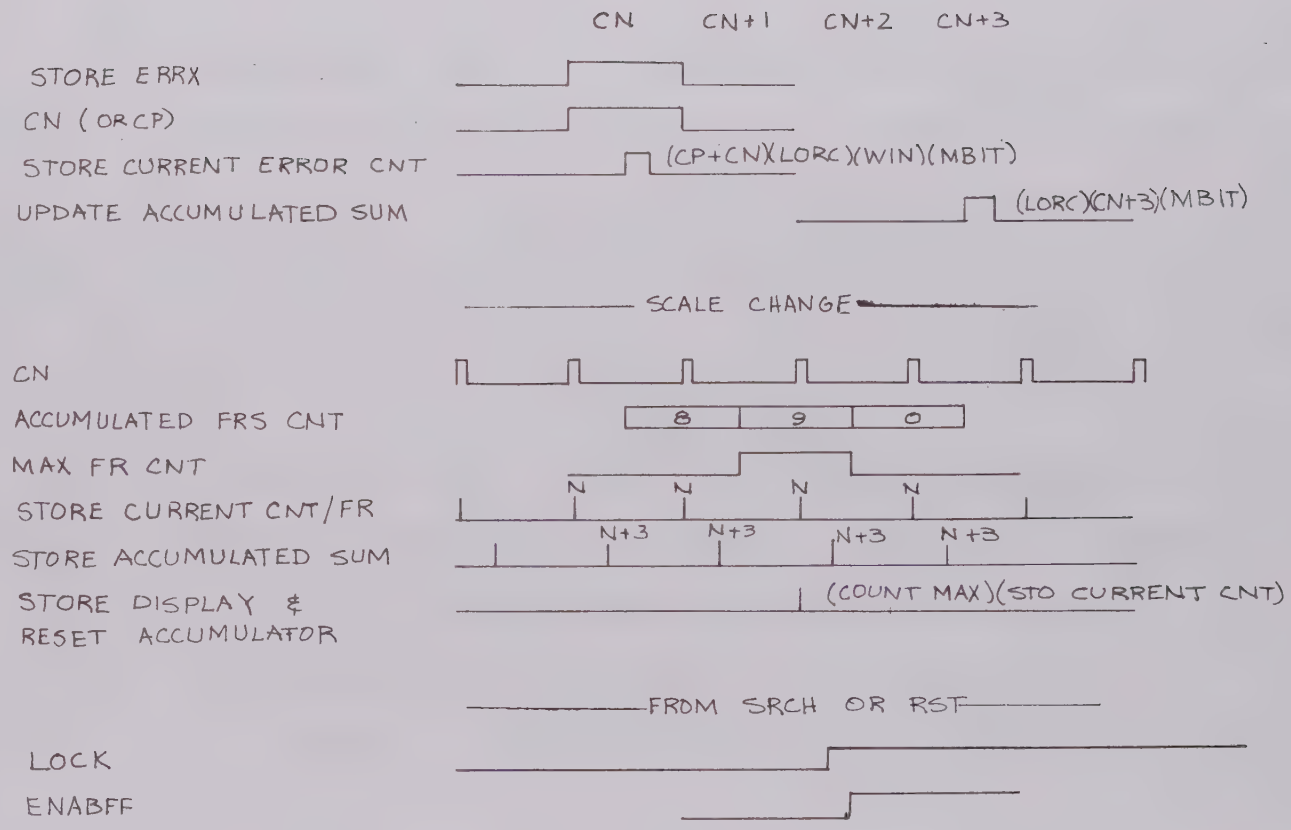


FIGURE 5-11. FRAME SYNC ERROR ACCUMULATOR AND DISPLAY.

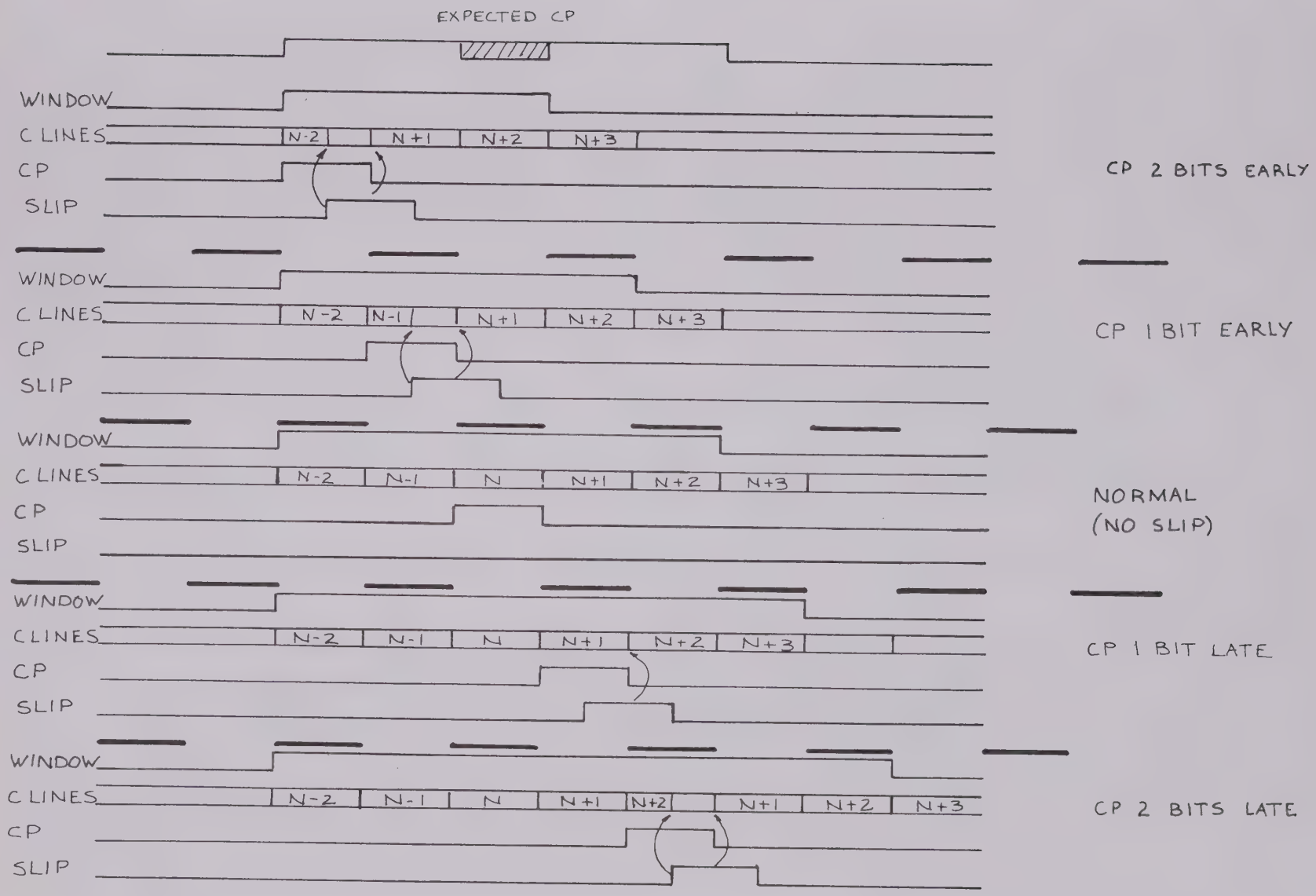
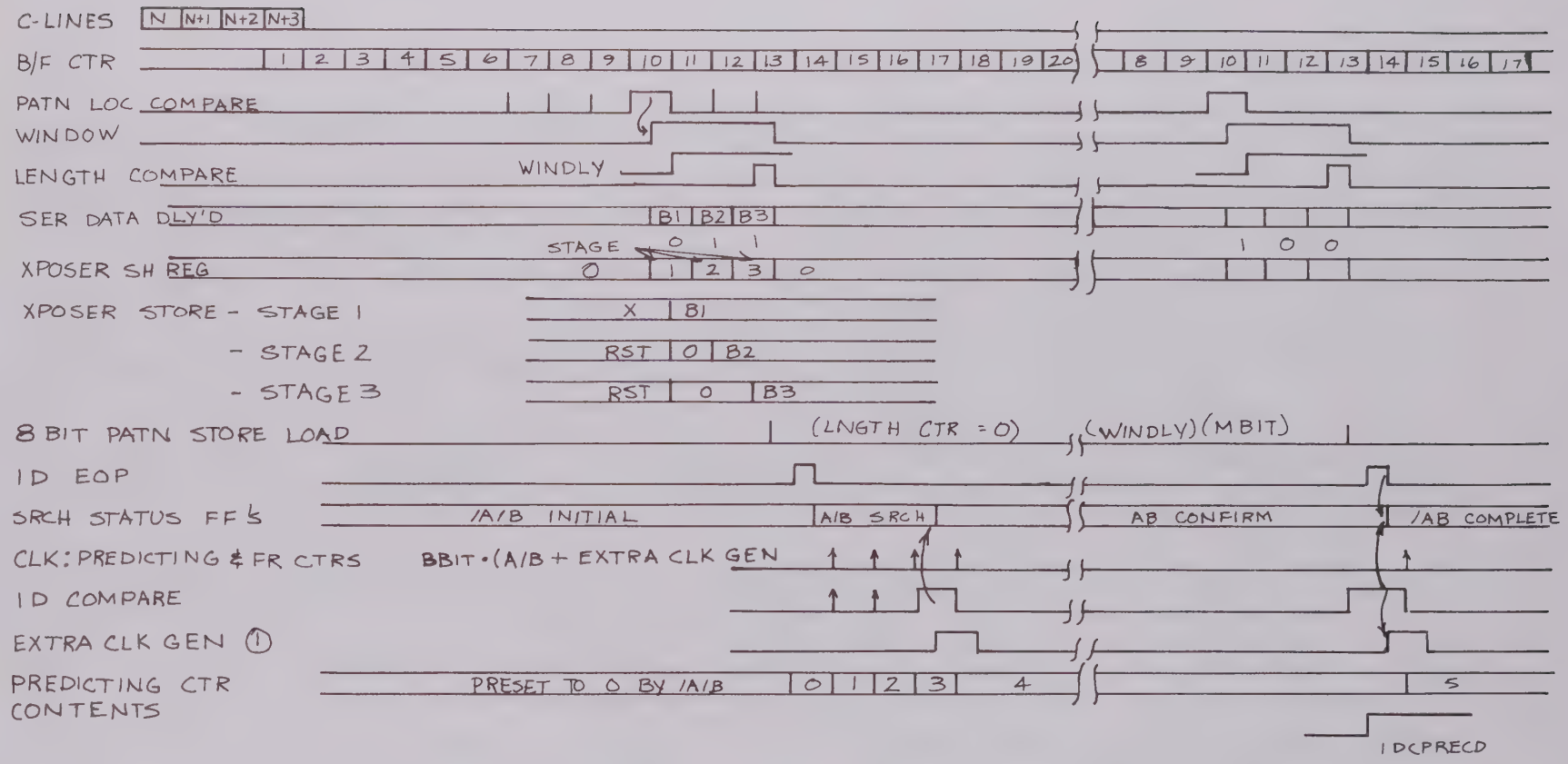


FIGURE 5-10. FRAME SYNC BIT SLIP.



① D: IDCMP, C: MBIT, R; / SRCH + / IDMODE
ASSUME ID COUNTS 0-7 & FIRST COUNT RECEIVED IS 3.

Figure 5-13. Subframe Sync ID (LSB First) Correlation.

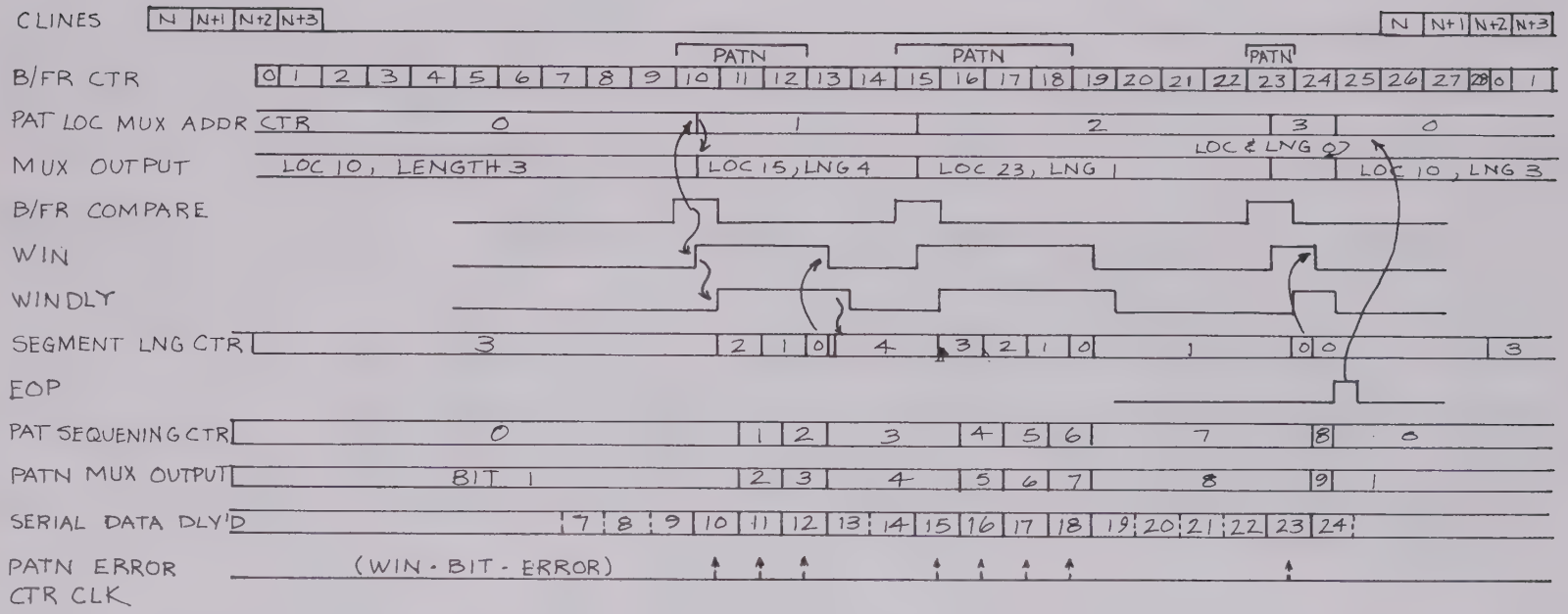
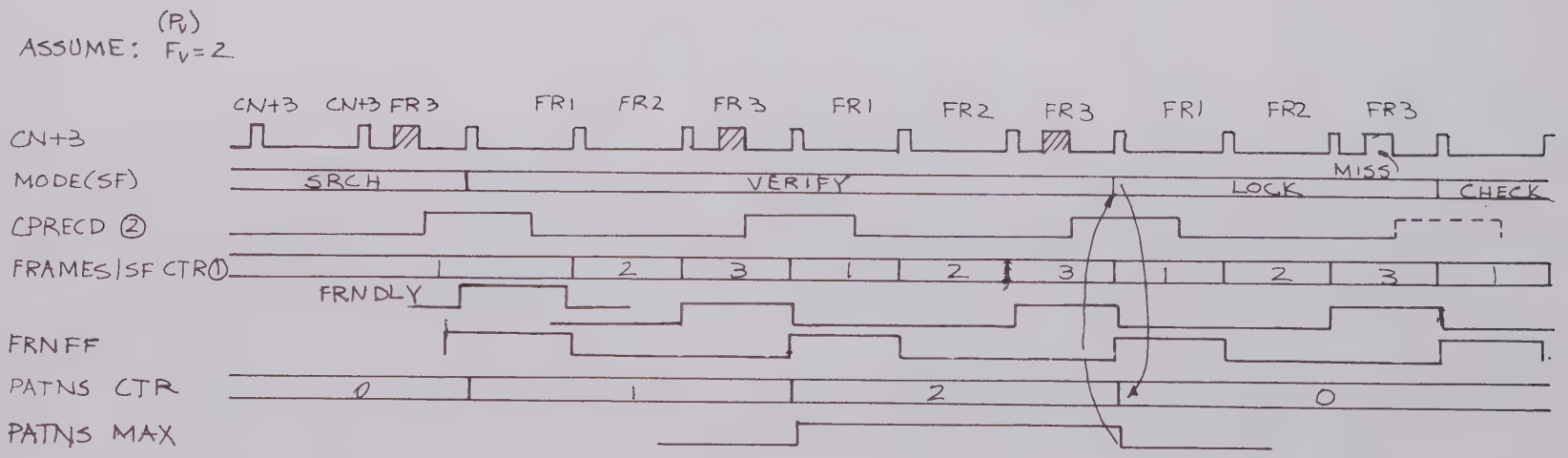


FIGURE 5-12. SUBFRAME SYNC RECYLCE CORRELATION



① CLK: /FRN · CN+3 ↑ ; PRST: (FRN · CN+3) + SFSRCH

② RCY → D: PATNCMP ; C: EOP ↑

RE 5-15. SUBFRAME SYNC RECYCLE MODE TIMING

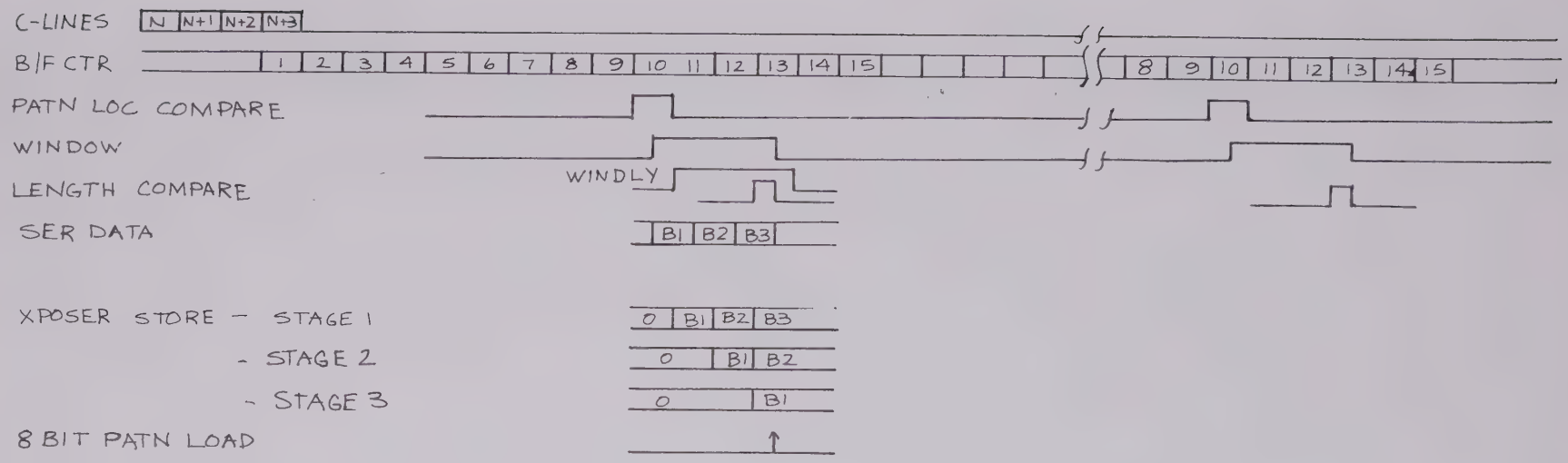


Figure 5-14. Subframe Sync ID (MSB Fisrt) Correlation.

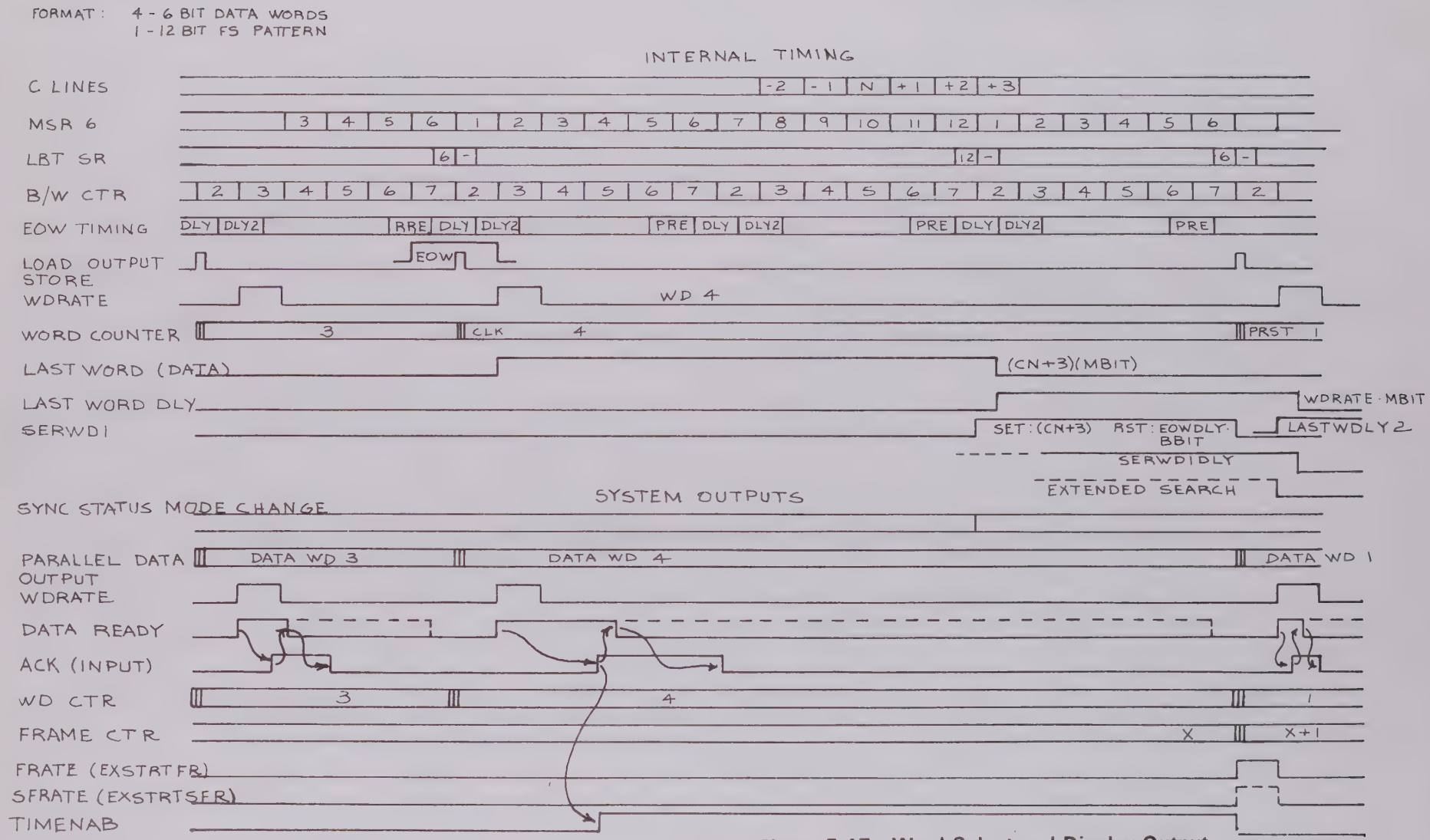


Figure 5-17. Word Select and Diaplay Output Timing. (Data Only Output).

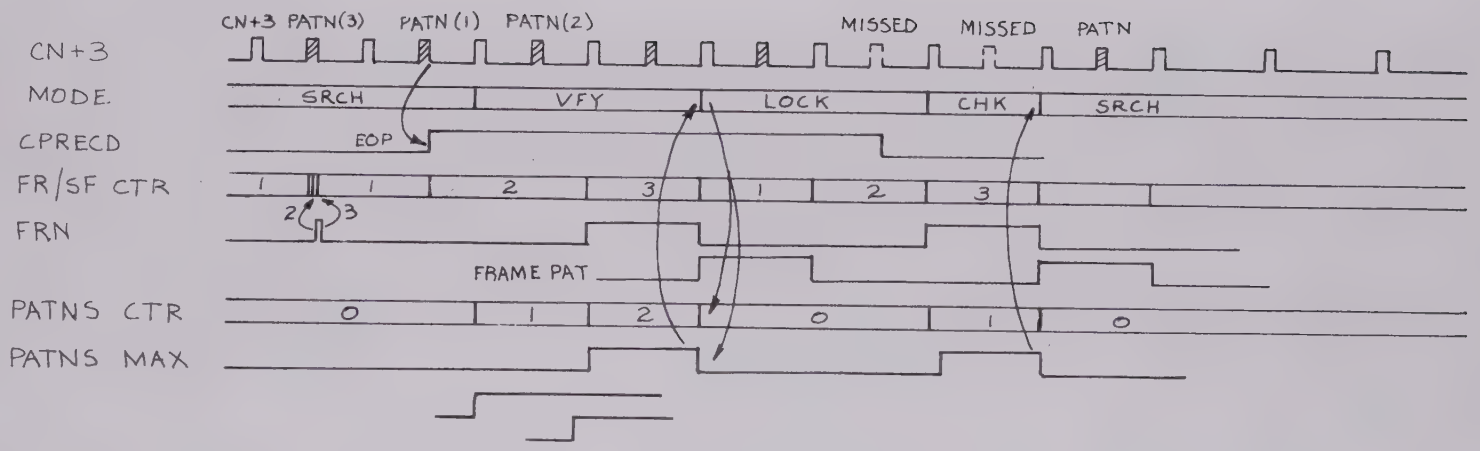
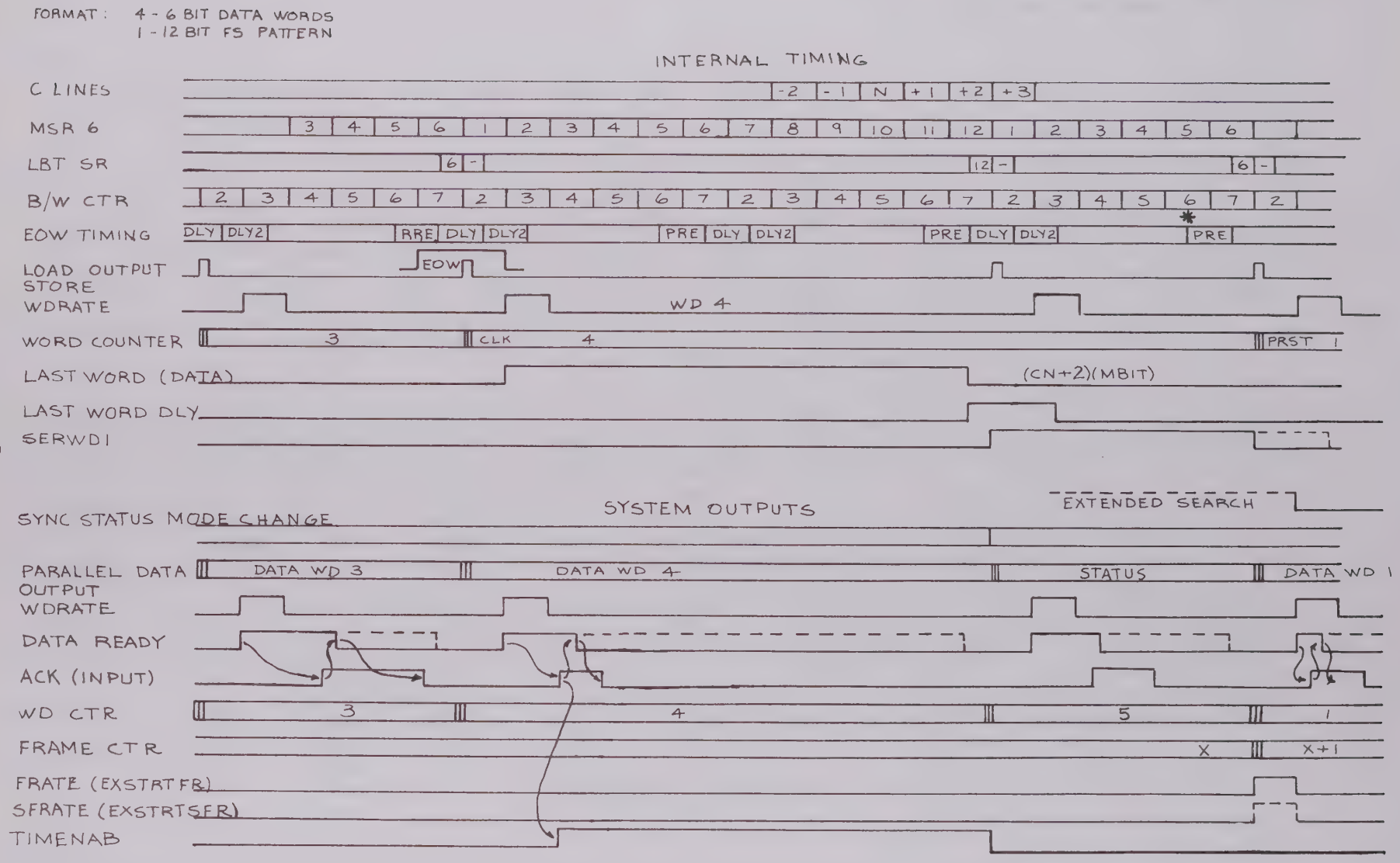


Figure 5-16. Subframe Sync ID Mode Timing.



*** Open Learning SRCH, EOW Timing is not generated until the end of SER WD 1**

Figure 5-19. Word Select and Display Output Timing (Status Word Output).

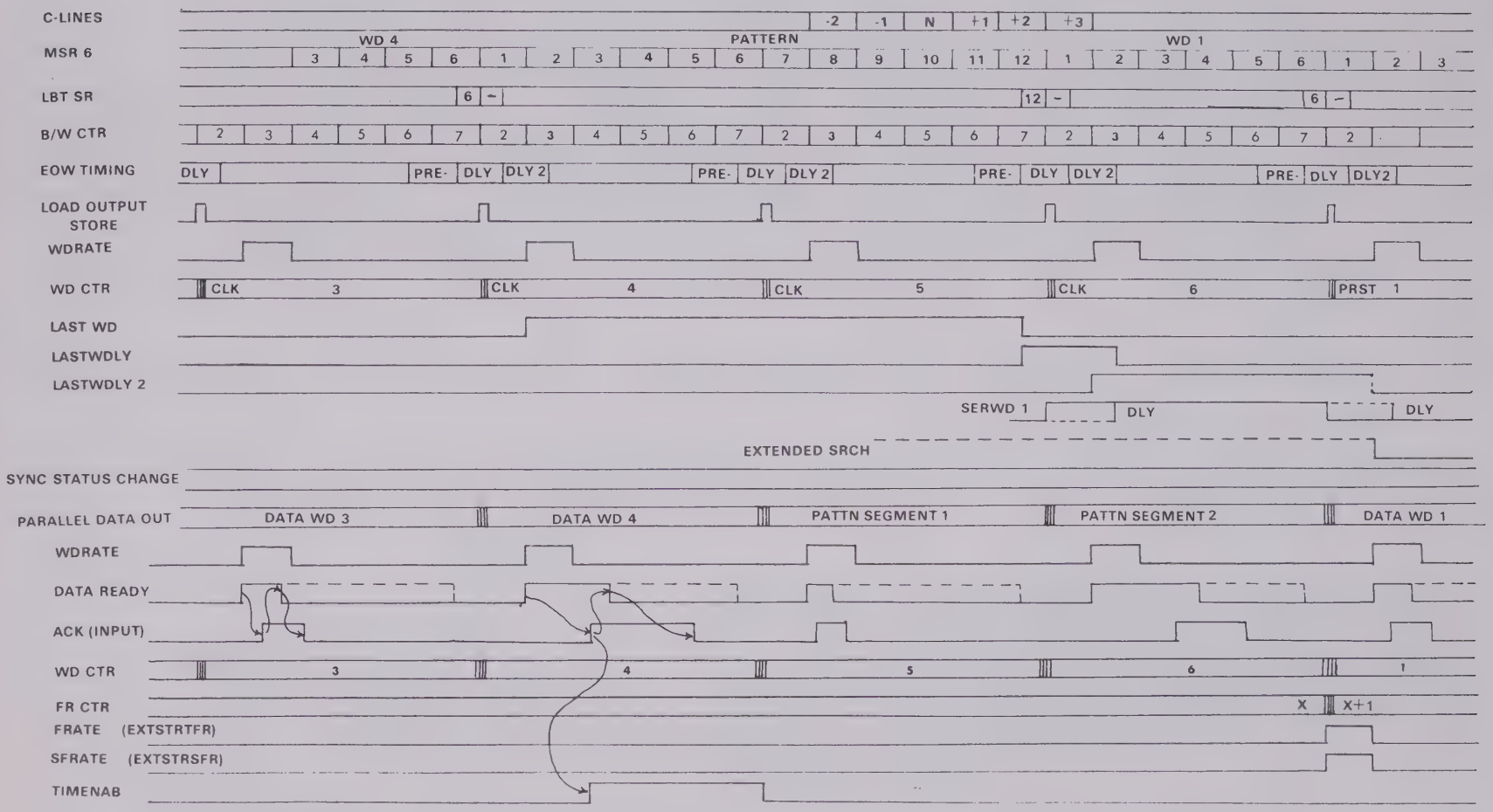


Figure 5-18. Word Select and Display Output Timing (Frame Sync Pattern Output)

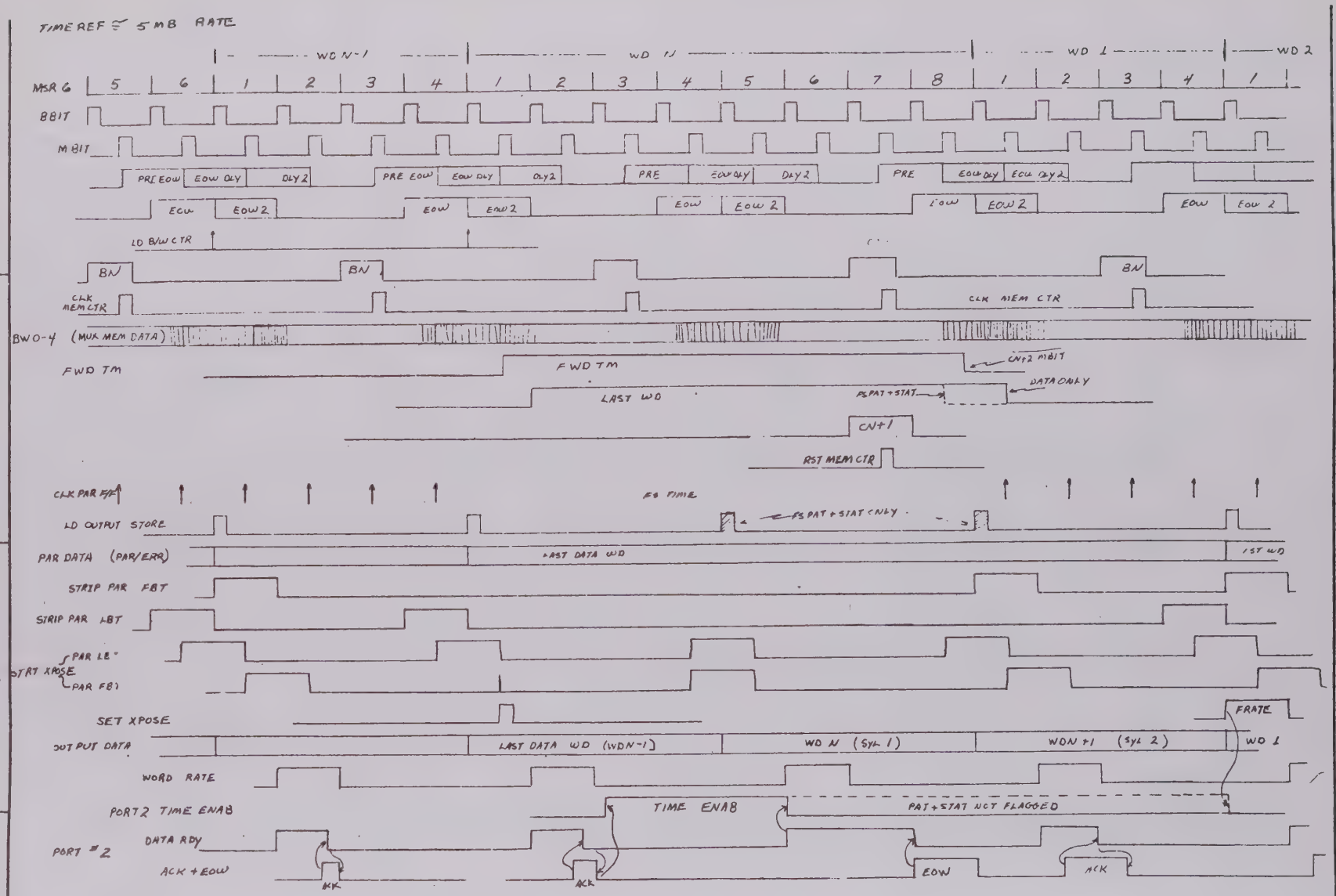


Figure 5-21. Variable Word Length and Variable Timing.

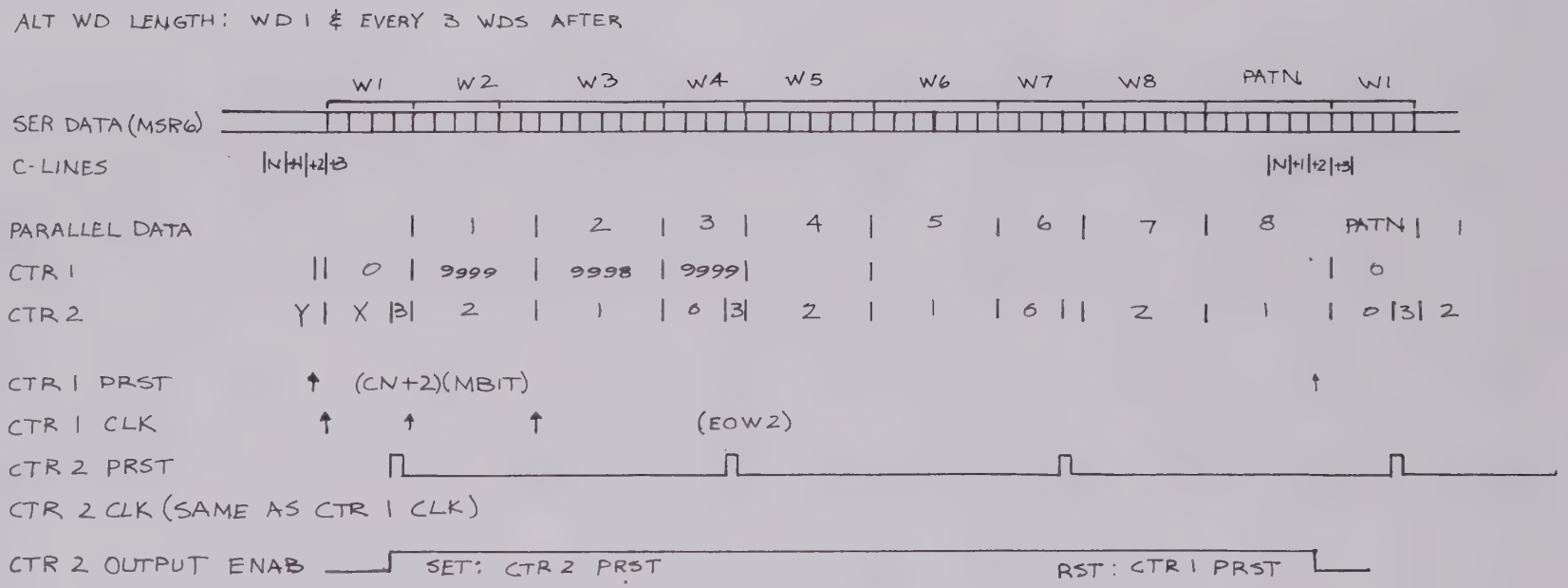
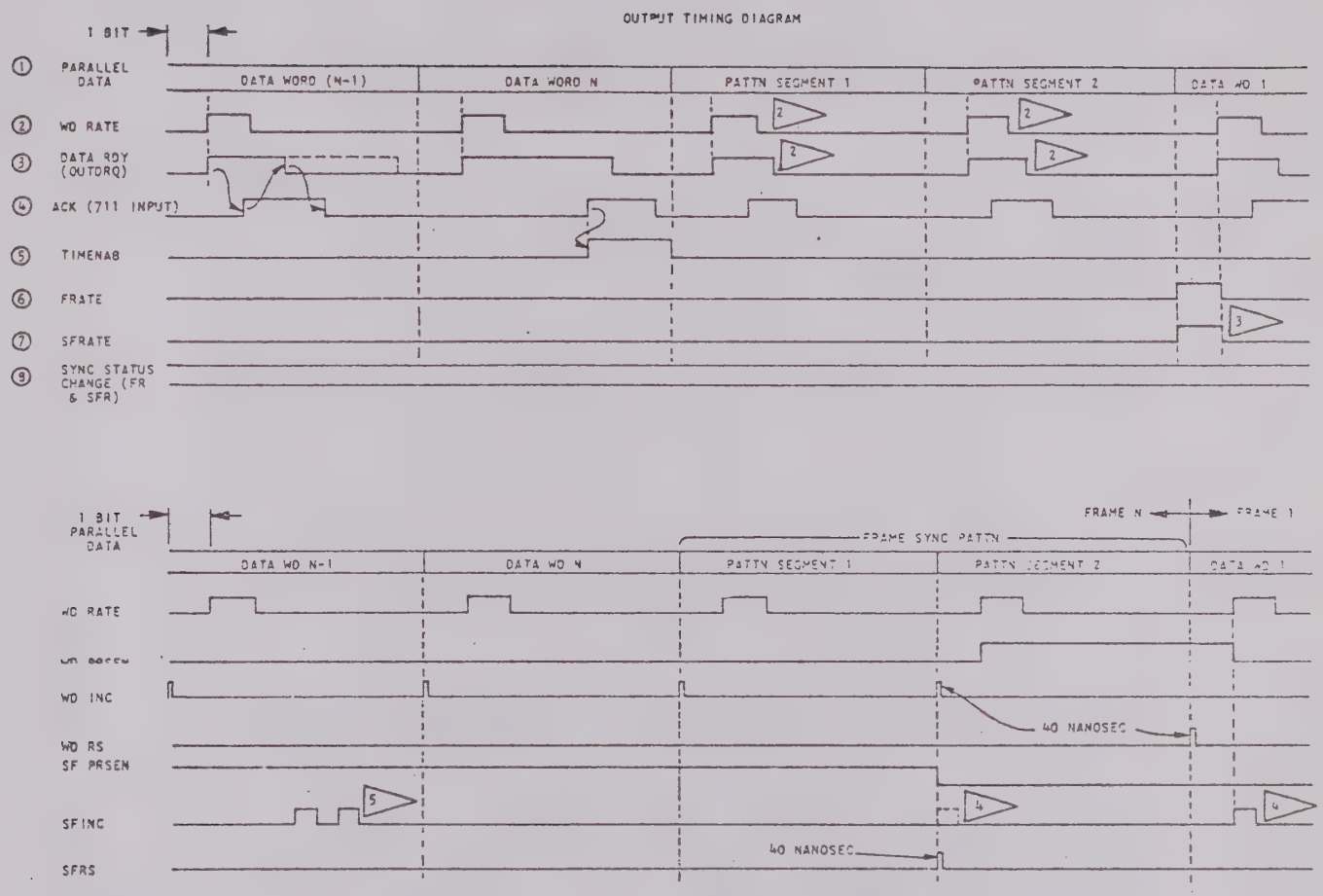


Figure 5-20. Word Selection and Display Timing.



NOTES:

5 IN ID MODE OCCURS AT BIT RATE DURING SYNC ACQUISITION. IN RECYCLE AND FCC SIGNALS 2 DO NOT OCCUR.

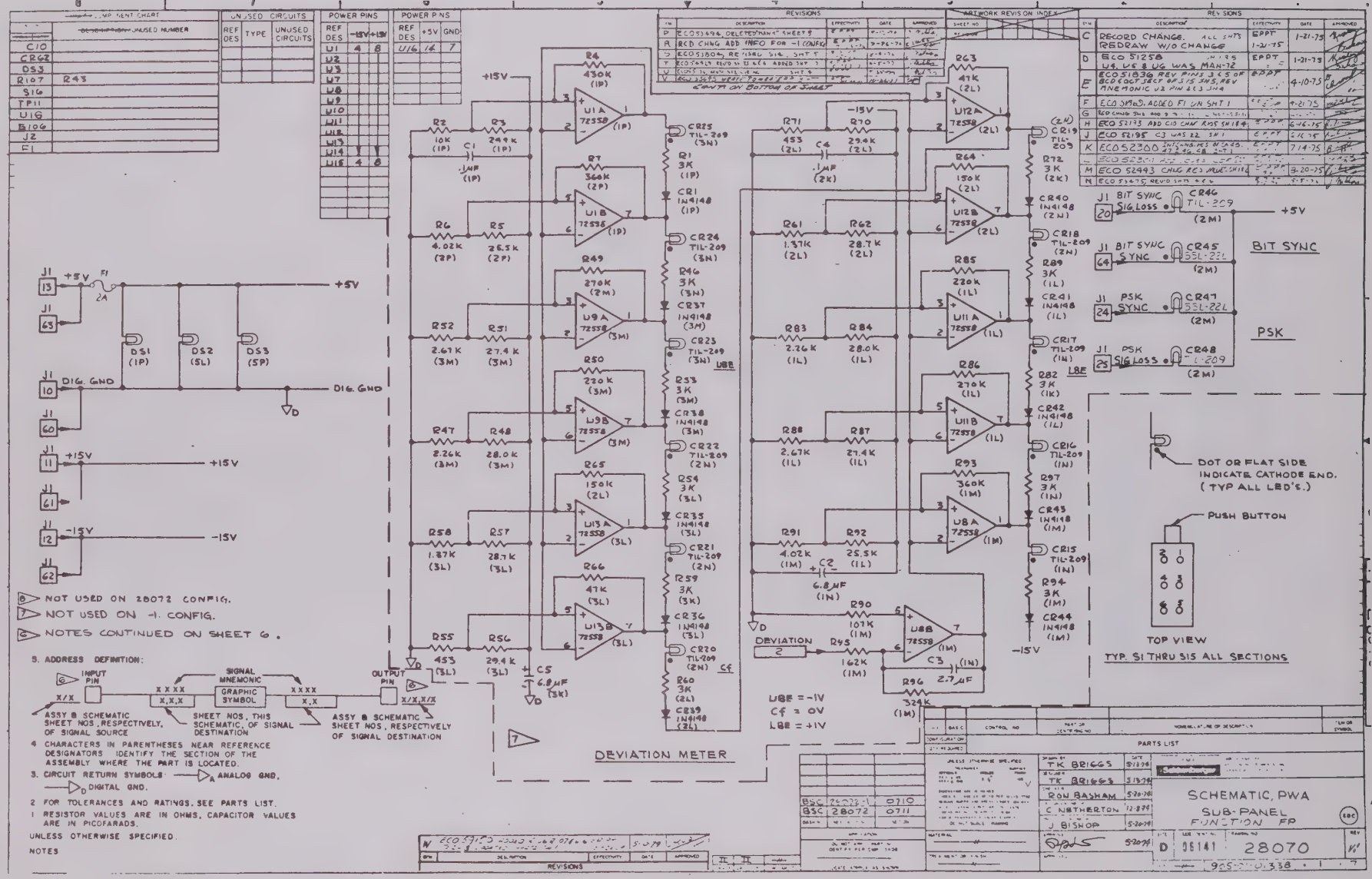
4 SFINC IS 1/2 BIT WIDE AND OCCURS ONCE PER FRAME (AFTER SF SYNC LEAVES SEARCH) COINCIDENT WITH FINAL FRAME SYNC PATN SEGMENT EXCEPT DURING THE FIRST FRAME WHEN SFINC OCCURS ONE BIT TIME AFTER DATA WD ONE IS PLACED ON THE OUTPUT LINES.

3 OCCURS DURING WORD 4 OF THE FIRST FRAME FOLLOWING THE SF PATTERN (ESSENTIALLY DEFINES "FRAME 1").

2 IF "DATA ONLY" MODE IS ACTIVE, SIGNALS ② & ③ ARE NOT ACTIVE FOR PATTN SEGMENTS. IF "STATUS" MODE IS ON, SIGS ② & ③ ARE NOT ACTIVE FOR PATTN SEGMENTS EXCEPT THE LAST ONE, AT WHICH TIME STATUS IS OUTPUT ON THE DATA LINES.

1 DATA RDY IS AUTOMATICALLY RESET 1/2 BIT TIME PRIOR TO DATA CHANGE IF ACK IS NOT RECEIVED.

Figure 5-22. Output Timing Diagram.


DEVIATION METER
SCHEMATIC, PWA
SUB-PANEL
FUNCTION FP
28070
BIT SYNC
PSK
+15V
-15V
DIG. GND
DEVIATION
TOP VIEW
TYP. SI THRU S15 ALL SECTIONS
DOT OR FLAT SIDE INDICATES CATHODE END. (TYP ALL LED'S.)
PUSH BUTTON
NOTES
UNLESS OTHERWISE SPECIFIED.
2 FOR TOLERANCES AND RATINGS, SEE PARTS LIST.
4 CHARACTERS IN PARENTHESES NEAR REFERENCE DESIGNATORS IDENTIFY THE SECTION OF THE ASSEMBLY WHERE THE PART IS LOCATED.
5. ADDRESS DEFINITION:
NOT USED ON 28072 CONFIG.
NOT USED ON -1. CONFIG.
NOTES CONTINUED ON SHEET 6.
UBE = -1V
Cf = 0V
LBE = +1V

2-9

SECTION 6

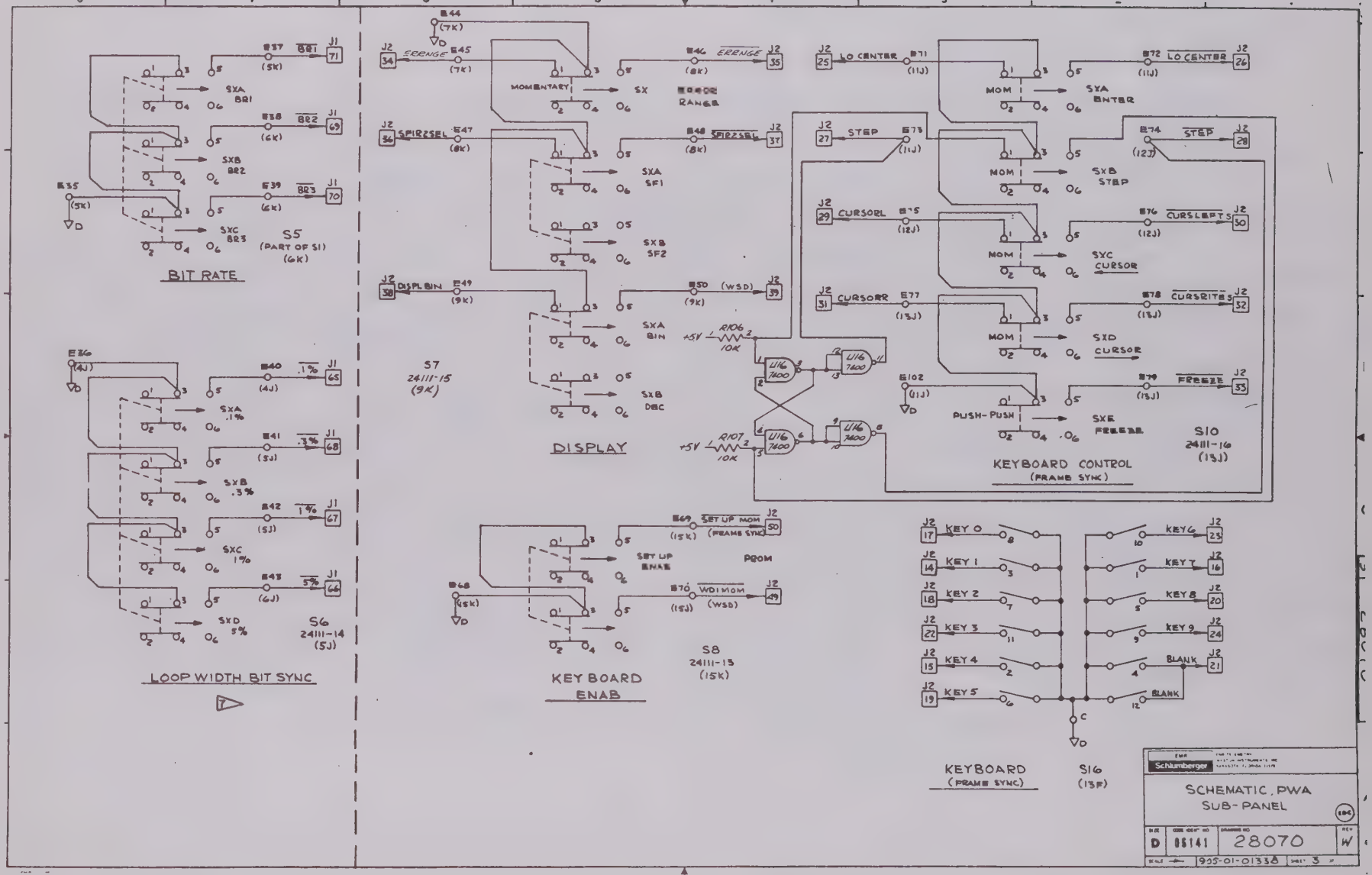
SCHEMATIC/LOGIC DIAGRAMS

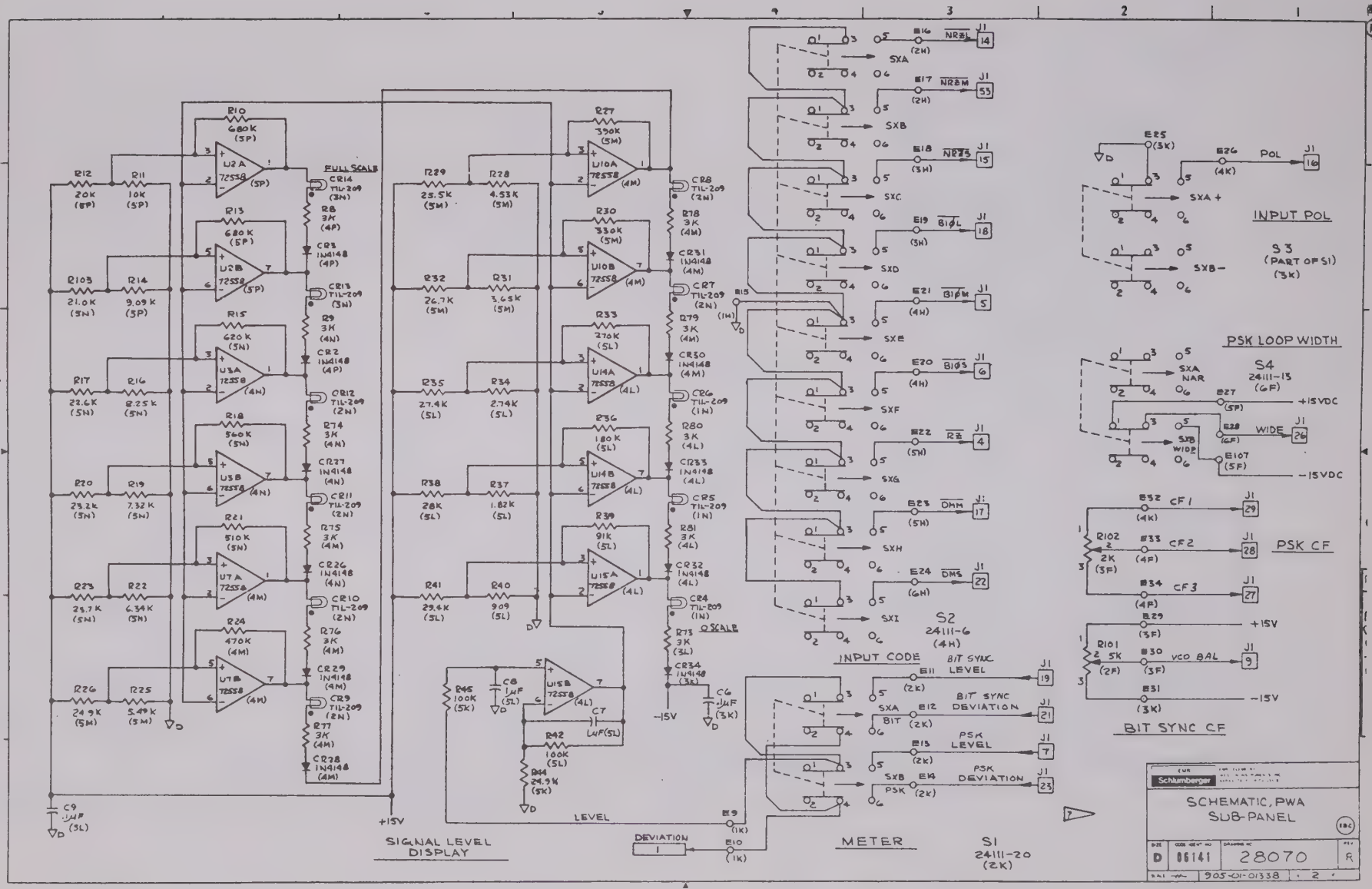
6.1 GENERAL

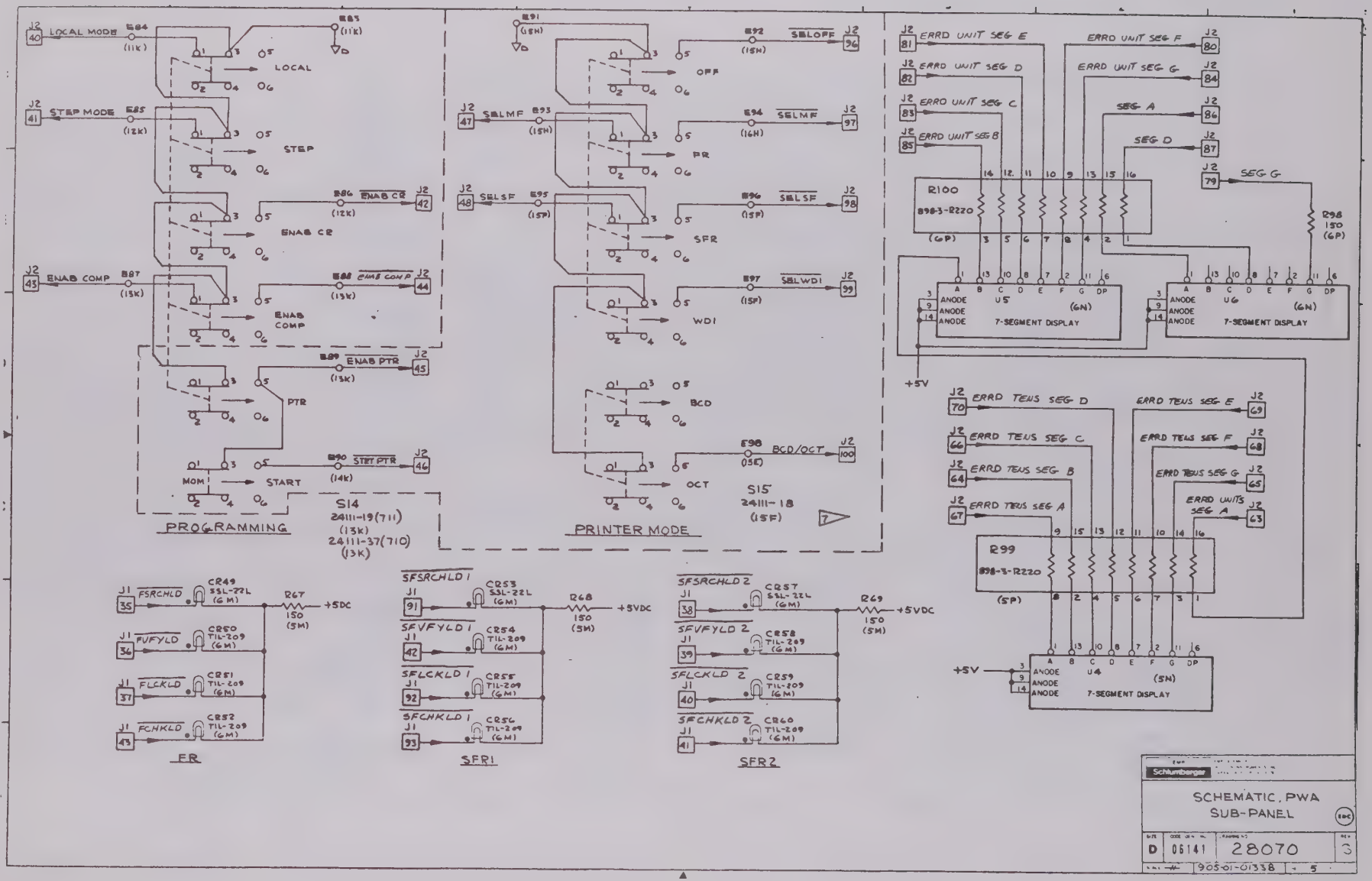
This section contains a complete set of schematic diagrams for the EMR Model 710 PCM Decommutator.

6.2 SCHEMATIC/LOGIC DIAGRAMS

DRAWING NO.	NAME
28070	Front Subpanel PWA Schematic (Function FP)
34595	Frame Sync PWASchematic (Function #4)
34597	Word Select & Display PWA Schematic (Function #8)
34309	Data Entry PWA Schematic (Function #10)
34599	Subframe Sync (2) PWA Sc-ematic (Function #5)
34590	Simulator Card 1 PWA Schematic (Function #6)
34593	Simulator Card 2 PWA Schematic (Function #7)
34307	Variable Word Length PWA Schematic Diagram
28704	Display Drivers Schematic (Basic Configuration)
28749	Display Drivers Schematic (-1 Configuration)


BIT RATE
S5
(PART OF S1)
(6K)
SXA BR1
SXB BR2
SXC BR3
LOOP WIDTH BIT SYNC
S6
24111-14
(5J)
SXA .1%
SXB .3%
SXC 1%
SXD 5%
DISPLAY
S7
24111-15
(9K)
SXA SF1
SXB SF2
SXA BIN
SXB DBC
KEY BOARD ENAB
S8
24111-15
(15K)
SET UP ENAB
KEYBOARD CONTROL
(FRAME SYNC)
S10
24111-16
(13J)
MOMENTARY
MOM
PUSH-PUSH
SX ERROR RANGE
SXA ENTER
SXB STEP
SXC CURSOR
SXD CURSOR
SXE FREEZE
KEYBOARD
(FRAME SYNC)
S16
(13F)
KEY 0
KEY 1
KEY 2
KEY 3
KEY 4
KEY 5
KEY 6
KEY 7
KEY 8
KEY 9
BLANK
Schlumberger
SCHEMATIC, PWA
SUB-PANEL
D
85141
28070
W
9205-01-01338


SIGNAL LEVEL DISPLAY
METER
S1
24111-20
(2K)
S2
24111-6
(4H)
S3
(PART OF S1)
(3K)
S4
24111-13
(6F)
INPUT POL
PSK LOOP WIDTH
PSK CF
BIT SYNC CF
INPUT CODE
FULL SCALE
0 SCALE
LEVEL
DEVIATION
+15V
-15V
SCHEMATIC, PWA
SUB-PANEL
Schlumberger
D
86141
28070
R
905-01-01338
2



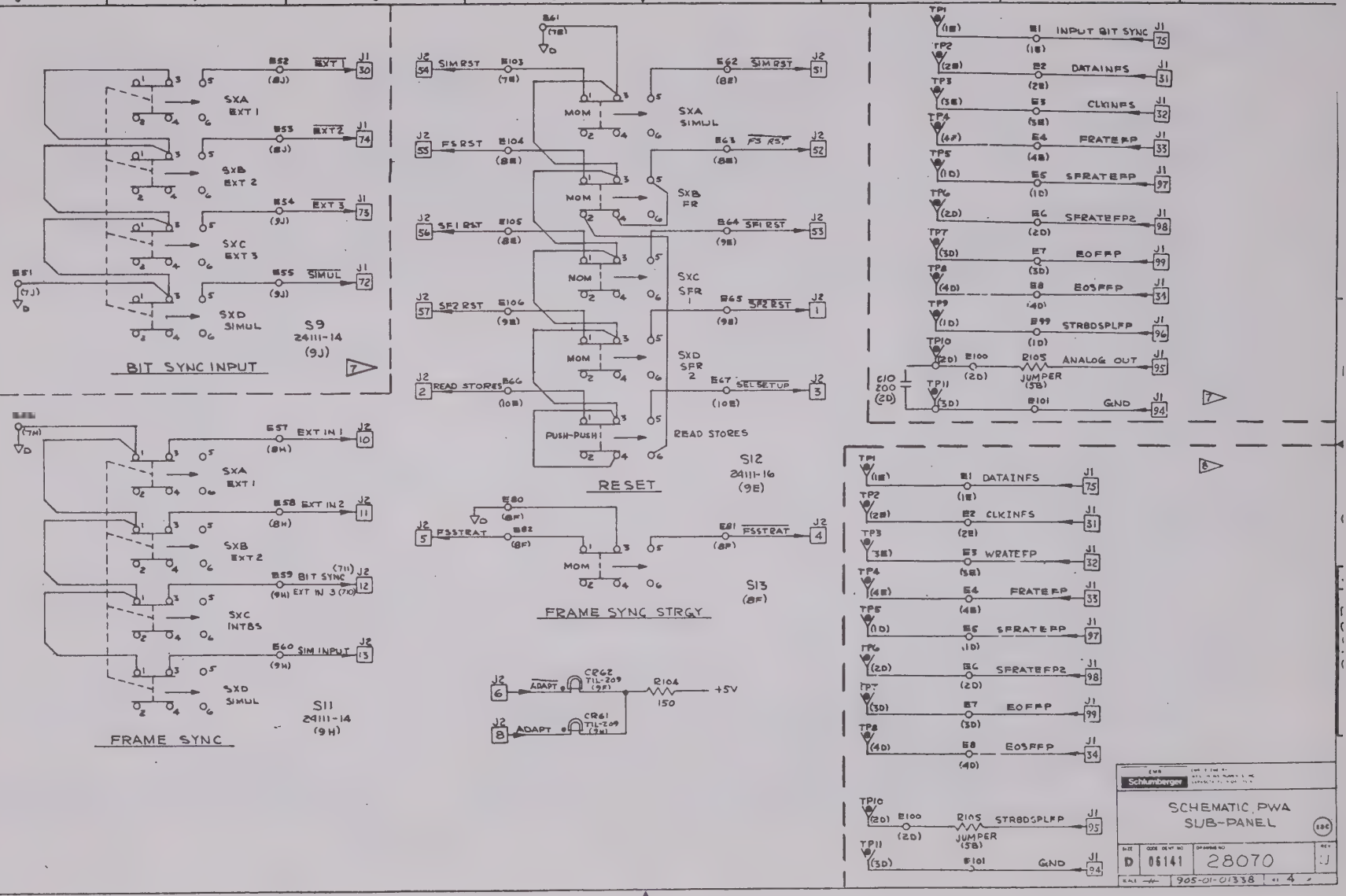
9-9

Schlumberger

SCHEMATIC, PWA
SUB-PANEL

D	05141	28070	3

905-01-01338 5


SXA EXT 1
SXB EXT 2
SXC EXT 3
SXD SIMUL
S9 24111-14 (9J)
BIT SYNC INPUT
SXA EXT 1
SXB EXT 2
SXC INTBS
SXD SIMUL
S11 24111-14 (9H)
FRAME SYNC
SXA SIMUL
SXB FR
SXC SFR 1
SXD SFR 2
PUSH-PUSH
READ STORES
S12 24111-16 (9E)
RESET
S13 (8F)
FRAME SYNC STRGY
INPUT BIT SYNC
DATAINFS
CLKINFS
FRATEFP
SFRATEFP
SFRATEFP2
EOFFP
EOSFFP
STRBDSPLFP
ANALOG OUT
JUMPER (5B)
GND
SCHEMATIC, PWA SUB-PANEL
Schlumberger
D
06141
28070
905-01-01338

J1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
1			
2			
3			
4	RZ	2	INT/3, 1/4, 3/6
5	IOM	2	INT/3, 1/4
6	IOS	2	INT/3, 1/4
7	PSK LEVEL	2	2-2/3, 2-1/1
8			
9	VCO BAL	2	INT/3, 1/1
10	DIG GND	1	⑥
11	+15V	1	⑥
12	-15V	1	⑥
13	+5V	1	⑥
14	NRZL	2	INT/3, 1/4
15	NRZS	2	INT/3, 1/4
16	POL	2	INT/3, 1/4
17	DMM	2	INT/3, 1/4
18	BIOL	2	INT/3, 1/4
19	BIT SYNC LEVEL	2	3/5
20	BIT SYNC SIG LOSS	1	3/5
21	BIT SYNC DEV	2	3/7
22	DMS	2	INT/3, 1/4
23	PSK DEVIATION	2	2-2/2, 2-1/3
24	PSK SYNC	1	2-1/3, 2-2/1
25	PSK SIG LOSS	1	2-1/1, 2-2/1
26	WIDE	2	INT/3, 2-1/3, 2-2/2
27	PSK CF 3	2	INT/3, 2-1/3, 2-2/2
28	PSK CF 2	2	INT/3, 2-1/3, 2-2/2
29	PSK CF 1	2	INT/3, 2-1/3, 2-2/2
30	EXT 1	4	INT/3, 3/1
31	CLK INFS	4	4/7
32	WRATEMP	4	5/20
33	FRATE FP	4	10/6 A2716 P37
34	E··· FFP	4	7/5
35	FSRCHLD	5	4/11
36	FVFYLD	5	4/11
37	FLCKLD	5	4/11
38	SF SRCH-DZ	5	5/21
39	SF VFYLDZ	5	5/21
40	SF LCKLDZ	5	5/21
41	SF CHKLDZ	5	5/21
42	SF JFYLD1	5	5/9
43	FCHKLD	5	4/11
44			
45			
46			
47			
48			
49			
50			

J1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
51			
52			
53	NR3M	2	INT/3, 1/4
54			
55			
56			
57			
58			
59			
60	DIG GND	1	⑥
61	+15V	1	⑥
62	-15V	1	⑥
63	+5V	1	⑥
64	BIT SYNC SYNC	1	3/6
65	.1%	3	INT/3, 3/7
66	5%	3	INT/3, 3/7
67	1%	3	INT/3, 3/7
68	.3%	3	INT/3, 3/7
69	BR2	3	INT/3, 3/2
70	BR3	3	INT/3, 3/2
71	BR1	3	INT/3, 3/2
72	SIMUL	4	INT/3, 3/1
73	EXT 3	4	INT/3, 3/1
74	EXT 2	4	INT/3, 3/1
75	DATA INFS	4	4/6
76			
77			
78			
79			
80			
81			
82			
83			
84			
85			
86			
87			
88			
89			
90			
91	SF SRCHLD1	5	5/9
92	SF LCKLD1	5	5/9
93	SF CHKLD1	5	5/9
94	DIG GND	4	INT/2
95	STRBDSPLFP	4	8/13
96			
97	SFRATE FP	4	5/11
98	SFRATE FP 2	4	5/23
99	EOFFP	4	7/6
100			

J2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
1	SF2 RST	4	INT/2, 5/21
2	READ STORES	4	INT/2, 10/5
3	SEL SET UP	4	INT/2, 10/5
4	FSSTRAT	4	INT/2, 4/11
5	FSSTRAT	4	INT/2, 4/11
6	ADAPT	4	4/11
7			
8	ADAPT	4	4/11
9			
10	EXT IN 1	4	INT/2, 4/7
11	EXT IN 2	4	INT/2, 4/7
12	BIT SYNC (711)	4	INT/2, 4/7 EXT IN 3 (710)
13	SIM INPUT	4	INT/2, 4/7
14	KEY 1	3	INT/2, 4/5
15	KEY 4	3	INT/2, 4/5
16	KEY 7	3	INT/2, 4/5
17	KEY 0	3	INT/2, 4/5
18	KEY 2	3	INT/2, 4/5
19	KEY 5	3	INT/2, 4/5
20	KEY 8	3	INT/2, 4/5
21	BLANK	3	INT/2, 4/5
22	KEY 3	3	INT/2, 4/5
23	KEY 6	3	INT/2, 4/5
24	KEY 9	3	INT/2, 4/5
25	LO CENTER	3	INT/2, 4/4
26	LO CENTER	3	INT/2, 4/4
27	STEP	3	INT/2, 4/4
28	STEP	3	INT/2, 4/4
29	CURSORL	3	INT/2, 4/4
30	CURSRITES	3	INT/2, 4/4
31	CURSORR	3	INT/2, 4/4
32	CURSLEFTS	3	INT/2, 4/4
33	FREQZE	3	INT/2, 4/4
34	ERRNGE	3	INT/2, 4/13
35	ERRNGE	3	INT/2, 4/13
36	SFIR2SEL	3	INT/2, 5/8
37	SFIR2SEL	3	INT/2, 5/8
38	DISPLBIN	3	INT/2, 8/17
39	(WSD)	3	INT/2
40	LOCAL MODE	5	INT/2, 4/4
41	STEP MODE	5	INT/2, 4/4
42	ENAB GR	5	INT/2, 4/4, 10/4
43	ENAB COMP	5	INT/2, 10/5
44	ENAB COMP	5	INT/2, 10/5, 4/4
45	ENAB PTR	5	INT/2, 4/4, 10/2
46	START PTR	5	INT/2, 10/4
47	SELMF	5	INT/2, 9/5
48	SELSF	5	INT/2, 9/6
49	WDIMOM	3	INT/2, 4/4, 8/10
50	SET UP MOM	3	INT/2, 4/4, 8/10

J2

PIN NO	MNEMONIC		PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51	SIMRST		4	INT/2, 7/10
52	FSRST		4	INT/2, 4/8
53	SFIRST		4	INT/2, 5/9
54	SIM RST		4	INT/2, 7/10
55	FSRST		4	INT/2, 4/8
56	SF1 RST		4	INT/2, 5/9
57	SF2 RST		4	INT/2, 5/21
58				
59				
60				
61				
62				
63	ERRD UNIT SEG A		5	4/14
64	TENS	B		
65		G		
66		C		
67		A		
68		F		
69		E		
70	ERRD TENS SEG D		5	4/14
71				
72				
73				
74				
75				
76				
77				
78				
79	SEG G		5	4/13
80	ERRD UNIT SEG F			4/14
81		E		
82		D		
83		C		
84		G		
85	ERRD UNIT SEG B			4/14
86	SEG A			4/13
87	SEG D		5	4/13
88				
89				
90				
91				
92				
93				
94				
95				
96	SELOFF		5	INT/2, 9/5
97	SELMF		5	INT/2, 9/5
98	SELSF		5	INT/2, 9/6
99	SELWDI		5	INT/2, 9/5
100	BCD/OCT		5	INT/2, 9/4

⑥ THIS SHEET USED ON 28072-1 ONLY

⑥ FOR ALL ELECTRICAL CROSS REF AS INDICATED IN NOTE 5 SEE ABOVE TABLE. ABBREVIATIONS USED FOR SOURCE AND DESTINATION DEFINITIONS ARE:
INT - INTERCONNECT SCHEMATIC 28073 (-4, 711 ONLY)
I/O - INPUT OUTPUT TABLE 30163 (711) OR 32939 (710)
FP - FRONT SUB-PANEL SCHEMATIC 28070 (711 & 710)
⑥ - WIRING DIAGRAM 28974 (711) OR 32945 (710)

Schlumberger

SCHEMATIC, PWA,
SUB PANEL
FUNCTION FP

SIZE	CAGE CODE NO.	DRAWING NO.	REV
D	06141	28070	V

SHEET 7 OF 7

8-9

J1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
1			
2			
3			
4	RZ	2	INT/3, 1/4, 3/6
5	RIDM	2	INT/3, 1/4
6	BDS	2	INT/3, 1/4
7	PSK LEVEL	2	2-1/3, 2-1/1
8			
9	VCO BAL	2	INT/3, 1/1
10	DIG GND	1	
11	+15V	1	
12	-15V	1	
13	+5V	1	
14	DRZL	2	INT/3, 1/4
15	DRZS	2	INT/3, 1/4
16	POL	2	INT/3, 1/4
17	DMM	2	INT/3, 1/4
18	BIBL	2	INT/3, 1/4
19	BIT SYNC LEVEL	2	3/5
20	BIT SYNC SIG LOW	1	3/5
21	BIT SYNC DET	2	3/7
22	DMS	2	INT/3, 1/4
23	PSK DEVIATION	2	2-1/3, 2-1/3
24	PSK SYNC	1	2-1/3, 2-2/1
25	PSK SIG LOSS	1	2-1/1, 2-2/1
26	WIDE	2	INT/3, 2-1/3, 2-2/3
27	PSK CF 3	2	INT/3, 2-1/3, 2-2/2
28	PSK CF 2	2	INT/3, 2-1/3, 2-2/2
29	PSK CF 1	2	INT/3, 2-1/3, 2-2/2
30	EAT 1	4	INT/3, 3/1
31	DATAINFS	4	4/6
32	CLKINFS	4	4/7
33	FPATEFP	4	8/20
34	EOFFP	4	7/9
35	FSRSHLD	5	4/11
36	FIFOLD	5	4/11
37	FCCLD	5	4/11
38	SF SCHLD2	5	5/21
39	SF IFLD2	5	5/21
40	SF CCLD2	5	5/21
41	SF CMKLD2	5	5/21
42	SF CFLD1	5	5/9
43	FCHKLD	5	4/11
44			
45			
46			
47			
48			
49			
50			

J1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51			
52			
53	NRZM	2	INT/3, 1/4
54			
55			
56			
57			
58			
59			
60	DIG GND	1	
61	+15V	1	
62	-15V	1	
63	+5V	1	
64	BIT SYNC SYNC	1	3/6
65	1.7₀	3	INT/3, 3/7
66	5.3₀	3	INT/3, 3/7
67	17₀	3	INT/3, 3/7
68	33₀	3	INT/3, 3/7
69	BRZ	3	INT/3, 3/2
70	BR3	3	INT/3, 3/2
71	BR1	3	INT/3, 3/2
72	SIMSL	4	INT/3, 3/1
73	EXT 3	4	INT/3, 3/1
74	EXT 2	4	INT/3, 3/1
75	INPUT BIT SYNC	4	3/2
76			
77			
78			
79			
80			
81			
82			
83			
84			
85			
86			
87			
88			
89			
90			
91	SF SCHLD1	5	5/9
92	SF CCKLDT	5	5/9
93	SF CMKLDT	5	5/9
94	DIG GND	4	INT/2
95	ANALOG OUTPUT	4	INT/2
96	STPBDSPLFP	4	8/3
97	SFRATE FP	4	5/11
98	SFRATE FP 2	4	5/23
99	EOFFP	4	7/6
100			

J2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
1	RESET	4	INT/2, 5/21
2	READ STORES	4	INT/2, 10/5
3	REL SET UP	4	INT/2, 10/5
4	FSSTRAT	4	INT/2, 4/11
5	FSSTRAT	4	INT/2, 4/11
6	ADAPT	4	4/11
7			
8	ADAPT	4	4/11
9			
10	EXT IN 1	4	INT/2, 9/7
11	EXT IN 2	4	INT/2, 9/7
12	BIT SYNC (711)	4	INT/2, 4/7 EXT IN 3 (710)
13	SIM INPUT	4	INT/2, 9/7
14	KEY 1	3	INT/2, 4/5
15	KEY 4	3	INT/2, 4/5
16	KEY 7	3	INT/2, 4/5
17	KEY 0	3	INT/2, 4/5
18	KEY 2	3	INT/2, 4/5
19	KEY 5	3	INT/2, 4/5
20	KEY 8	3	INT/2, 4/5
21	BLANK	3	INT/2, 4/5
22	KEY 3	3	INT/2, 4/5
23	KEY 6	3	INT/2, 4/5
24	KEY 9	3	INT/2, 4/5
25	LO CENTER	3	INT/2, 4/4
26	LO CENTER	3	INT/2, 4/4
27	STEP	3	INT/2, 9/4
28	STEP	3	INT/2, 9/4
29	CURSORL	3	INT/2, 4/4
30	CURSRITES	3	INT/2, 4/4
31	CURSRR	3	INT/2, 4/4
32	CURSLEFTS	3	INT/2, 9/4
33	FREEZE	3	INT/2, 9/4
34	EPRIGE	3	INT/2, 4/13
35	EPRISE	3	INT/2, 4/13
36	SFIRZSEL	3	INT/2, 5/8
37	SF CRZSEL	3	INT/2, 5/8
38	DISPLBIN	3	INT/2, 9/17
39	(N3D)	3	INT/2
40	LOCAL MODE	5	INT/2, 4/4
41	STEP MODE	5	INT/2, 4/4
42	ENAB GR	5	INT/2, 4/4, 10/4
43	ENABCOMP	5	INT/2, 10/5
44	ENAB COMP	5	INT/2, 10/5, 4/4
45	ENAB PTR	5	INT/2, 4/4, 10/2
46	START PTR	5	INT/2, 10/4
47	SELMF	5	INT/2, 3/5
48	SELSF	5	INT/2, 9/6
49	WDINADJA	3	INT/2, 4/4, 8/10
50	SET UP MSM	3	INT/2, 4/4, 8/10

J2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51	SIMRST	4	INT/2, 7/10
52	FSRST	4	INT/2, 4/9
53	SFIRST	4	INT/2, 5/9
54	SIMRST	4	INT/2, 7/10
55	FSRST	4	INT/2, 4/8
56	SF1RST	4	INT/2, 5/9
57	SF2RST	4	INT/2, 5/21
58			
59			
60			
61			
62			
63	ERRD UNIT SEG A	5	4/14
64	TENS B		
65	G		
66	C		
67	A		
68	F		
69	E		
70	ERRD TENS SEG D	5	4/14
71			
72			
73			
74			
75			
76			
77			
78			
79	SEG G	5	4/13
80	ERRD UNIT SEG F		4/14
81	E		
82	D		
83	C		
84	G		
85	ERRD UNIT SEG B		4/14
86	SEG A		4/13
87	SEG D	5	4/13
88			
89			
90			
91			
92			
93			
94			
95			
96	FCLOFF	5	INT/2, 9/5
97	SELMF	5	INT/2, 9/5
98	SELSF	5	INT/2, 9/6
99	SELADJ	5	INT/2, 9/5
100	BCD/OCT	5	INT/2, 9/4

6 FOR ALL ELECTRICAL CROSS REF AS INDICATED IN NOTE 5 SEE ABOVE TABLE. ABBREVIATIONS USED FOR SOURCE AND DESTINATION DEFINITIONS ARE:
INT - INTERCONNECT SCHEMATIC 28073 ([illegible] ONLY)
I/O - INPUT OUTPUT TABLE 30183 [illegible] 30233 (710)
FP - FRONT SUB-PANEL SCHEMATIC 28070 [illegible] 6/13)
7 - WIRING DIAGRAM 28974 (711), A [illegible] 2345 (713)

NOTES: CONTINUED

— THIS SHEET USED ON 28072 ONLY —

Schlumberger

SCHEMATIC, PWA,
SUB PANEL
FUNCTION FP

D	06141	28070	T

6-7

Schlumberger

SCHEMATIC PWA
FRAME SYNC

D | 06141 | 29312 | AD

9050101305

6-10

COMPONENT CHART	
	NUMBER
RA 24	RA1-15, 18-20, 22, 23
UA 23	UA4-8, 13, 14, 16, 17, 21
UB 29	UB4-7
UC 34	
UD 34	
UE 34	
UF 34	UF6, 7, 11, 12, 15
UG 32	UG5, 10, 11, 6, 7
UH 34	
UJ 34	
ZF6	ZF1-5
ZG15	ZG1-5, 8-13
F2	

UNUSED CIRCUITS		
REF DES	TYPE	UNUSED CIRCUITS
UB1	7404	D E F
UC17	74H183	B
UB3	7432	C,D
UB7	74S74	B
UB13	7404	F
UB14	7404	E,F
UB16	7404	E
UB17	7405	C,D,E,F
UC25		
UC29	74107	B
UC30	7437	ABC
UC32	7403	D
UC33	7420	B
UD31	7404	E,F
UD34		
UE10	7404	D,E
UE16	7420	B
UA15	7476	B
UH5	7404	B
UH10	74125	B,C,D
UH13	74H40	C,D
UH16	7413	B
UG8	74123	B
UH7	7474	A
UJ8	7404	E,F
UJ9	7404	E,F
UJ12	74S04	C,D,E,F
UJ34	7402	D

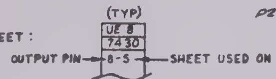
POWER PINS			POWER PINS			POWER PINS			POWER PINS			POWER PINS			POWER PINS			POWER PINS			POWER PINS		
REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND
UA1	16	8	UC5	14	7	UD8	14	7	UE11	14	7	UF17	16	8	UG28	16	8	UH32	14	7	UJ33	14	7
UA2	16	8	UC6	14	7	UD9	14	7	UE12	14	7	UF18	16	8	UG29	16	8	UH33	14	7	UJ34	14	7
UA3	16	8	UC7	14	7	UD10	14	7	UE13	14	7	UF19	16	8	UG30	16	8	UH34	14	7	UA9	5	12
UA15	5	13	UC8	14	7	UD11	14	7	UE14	14	7	UF20	16	8	UG31	16	8	UJ1	14	7	UA10	5	12
UA18	5	10	UC9	14	7	UD12	14	7	UE15	14	7	UF21	16	8	UG32	16	8	UJ2	14	7	UA11	5	12
UA19	5	12	UC10	14	7	UD13	14	7	UE16	14	7	UF22	16	8	UH1	14	7				UA12	5	12
UA20	5	12	UC11	14	7	UD14	14	7	UE17	14	7	UF23	16	8	UH2	14	7	UJ3	14	7	UG8	16	8
UA22	5	10	UC12	14	7	UD15	14	7	UE18	14	7	UF24	16	8	UH3	14	7				F34	16	8
UA23	5	10	UC13	14	7	UD16	14	7	UE19	14	7	UF25	16	8	UH4	14	7	UJ4	14	7	F33	14	7
UB1	14	7	UC14	14	7	UD17	14	7	UE20	14	7	UF26	16	8	UH5	14	7	UJ5	14	7	B2	14	7
UB7	14	7	UC15	14	7	UD18	14	7	UE21	14	7	UF27	16	8	UH6	14	7	UJ6	14	7	B3	14	7
UB8	14	7	UC16	14	7	UD19	14	7	UE22	14	7	UF28	16	8	UH7	14	7	UJ7	[illegible]	7			
UB9	14	7	UC17	14	7	UD20	14	7	UE23	14	7	UF29	16	8				UJ8	14	7			
UB10	14	7	UC18	14	7	UD21	14	7	UE24	14	7	UF30	16	8	UH8	14	7	UJ9	14	7			
UB11	14	7	UC19	14	7	UD22	14	7	UE25	14	7	UF31	16	8	UH9	14	7	UJ10	14	7			
UB12	14	7	UC20	14	7	UD23	14	7	UE26	14	7	UF32	16	8				UJ11	14	7			
UB13	14	7	UC21	14	7	UD24	14	7	UE27	14	7	UG1	16	8	UH11	14	7	UJ12	14	7			
UB14	14	7	UC22	14	7	UD25	14	7	UE28	14	7	UG2	16	8	UH12	14	7	UJ13	14	7			
UB15	14	7	UC23	14	7	UD26	14	7	UE29	14	7	UG3	16	8	UH13	14	7	UJ14	14	7			
UB16	14	7	UC24	14	7	UD27	14	7	UE30	14	7	UG4	16	8	UH14	14	7	UJ15	14	7			
UB17	14	7	UC25	14	7	UD28	14	7	UE31	14	7	UG9	16	8	UH15	14	7	UJ16	14	7			
UB18	16	8	UC26	14	7	UD29	14	7	UE32	14	7				UH16	14	7	UJ17	14	7			
UB19	16	8	UC27	14	7	UD30	14	7	UE33	14	7				UH17	14	7	UJ18	14	7			
UB20	16	8	UC28	14	7	UD31	14	7	UE34	14	7	UG12	16	8	UH18	14	7	UJ19	14	7			
UB21	16	8	UC29	14	7	UD32	14	7	UF1	16	8	UG13	16	8	UH19	14	7	UJ20	14	7			
UB22	16	8	UC30	14	7	UD33	14	7	UF2	16	8	UG16	16	8	UH20	14	7	UJ21	14	7			
UB23	16	8	UC31	14	7	UD34	14	7	UF3	16	8	UG17	16	8	UH21	14	7	UJ22	14	7			
UB24	16	8	UC32	14	7	UE1	14	7	UF4	16	8	UG18	16	8	UH22	14	7	UJ23	14	7			
UB25	16	8	UC33	14	7	UE2	14	7	UF5	16	8	UG19	16	8	UH23	14	7	UJ24	14	7			
UB26	16	8	UC34	14	7	UE3	14	7	UF8	16	8	UG20	16	8	UH24	14	7	UJ25	14	7			
UB27	16	8	UD1	14	7	UE4	14	7	UF9	16	8	UG21	16	8	UH25	14	7	UJ26	14	7			
UB28	16	8	UD2	14	7	UE5	14	7	UF10	16	8	UG22	16	8	UH26	14	7	UJ27	14	7			
UB29	16	8	UD3	14	7	UE6	14	7				UG23	16	8	UH27	14	7	UJ28	14	7			
UC1	14	7	UD4	14	7	UE7	14	7				UG24	16	8	UH28	14	7	UJ29	14	7			
UC2	14	7	UD5	14	7	UE8	14	7	UF13	16	8	UG25	16	8	UH29	14	7	UJ30	14	7			
UC3	14	7	UD6	14	7	UE9	14	7	UF14	16	8	UG26	16	8	UH30	14	7	UJ31	14	7			
UC4	14	7	UD7	14	7	UE10	14	7	UF16	16	8	UG27	16	8	UH31	14	7	UJ32	14	7			

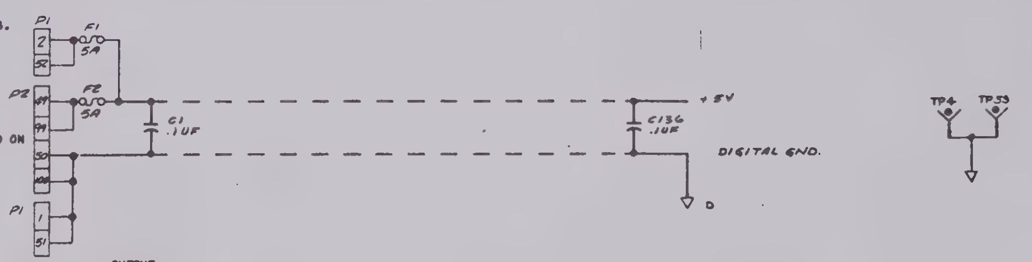
REVISIONS				
LTR	DESCRIPTION		DATE	APPROVED
A	REC. CHNG REDRAWN WITHOUT CHNG	[illegible]	1/9/74	[illegible]
B	ECO 51813 ADDED RA21J K RA24J,K AND CHNG UE33, 34 UC27, ADDED RA17H, SHT 1 & 2	[illegible]	4/10/75	[illegible]
C	ECO 51885 [illegible]	[illegible]	[illegible]	[illegible]
D	ECO 51867, ADDED F1 & F2		4/21/75	[illegible]
E	ECO 51953 [illegible]	[illegible]	6-24-75	[illegible]
F	ECO 51972 [illegible]	[illegible]	4 26 75	[illegible]
G	[illegible]	[illegible]	[illegible]	[illegible]
H	ECO 52141 [illegible]	[illegible]	6-4-75	[illegible]
J	ECO 52194 DELETE CONNECTION AT [illegible]	[illegible]	6-10-75	[illegible]
K	ECO 52301, ADDED NOTE 8 ELECTRICAL [illegible] REF ALL SHT	EPPT [illegible]	JULY 10, [illegible]	[illegible]
L	RCD CHNG REV NOTE 7 & ADD SH 3	EPPT 8-29-75	8-28-75	[illegible]
M	ECO 52494 ADD XADAPT [illegible] SHTS 11 & 23	[illegible]	9-9 75	[illegible]
N	ECO 53475, ADDED [illegible] SHTS 4, 7, 23	[illegible]	5-5-76	[illegible]
P	ECO 53749 CHGD SHTS 2, 5, 10, 12, 13 [illegible]	[illegible]	7/21/76	[illegible]
R	ECO 53820, ADDED UC25-B-D, UD34-A, UH34-A. SHTS [illegible]	EPPT 8-13-76	8-13-76	[illegible]
S	ECO 53868 CHNG SHEETS 1, 2, 3A, 4, 7, 12,	[illegible]	8-27-76	[illegible]
T	RCD CHNG, ADD [illegible] (—) TO MNEMONICS FROM UF33-PINS 1 & 2 SH 7 [illegible]	EPPT 9-20-76	9-20-76	[illegible]
U	ECO 54130 CIRCUIT CHANGE SHTS 3 & 5 [illegible]	[illegible]	10 [illegible] 76	[illegible]
V	ECO 54284, ADDED [illegible] SHT 3 & 4	[illegible]	11-17-76	[illegible]
W	ECO 54300, ADDED [illegible]	[illegible]	1-3-77	[illegible]
Y	[illegible] 55433 [illegible]	[illegible]	[illegible]	[illegible]
Z	ECO 55672 ADDED UB7 SHTS 1 2, 12	[illegible]	11-03-77	[illegible]
AA	ECO 55128 REVISED ZG14 SHT 2	[illegible]	11-21-77	[illegible]
AB	ECO [illegible] ADDED [illegible] SHT 1 & 2	[illegible]	[illegible]	[illegible]
AC	ECO 56711 DELETED UJ34 D SHT 1, 2, 13 & 23	[illegible]	7-5-78	[illegible]
AD	ECO 60506 REVISED 8BIT EMBIT SHT [illegible]	[illegible]	1-2-80	[illegible]

8 NOTES CONTINUED ON SHEET 23.

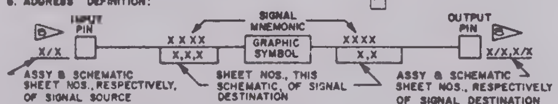
7 THIS DWG IS COMPLETE WITH SHEETS 1 THRU 23 & 3A, 3B & 3C.

6 ON SHEET:





5. ADDRESS DEFINITION:



4. CHARACTERS IN PARENTHESES NEAR REFERENCE DESIGNATORS IDENTIFY THE SECTION OF THE ASSEMBLY WHERE THE PART IS LOCATED.

3. CIRCUIT RETURN SYMBOLS: —▷A ANALOG GND, —▷D DIGITAL GND.

2. FOR TOLERANCES AND RATINGS, SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS.

UNLESS OTHERWISE SPECIFIED:

NOTES.

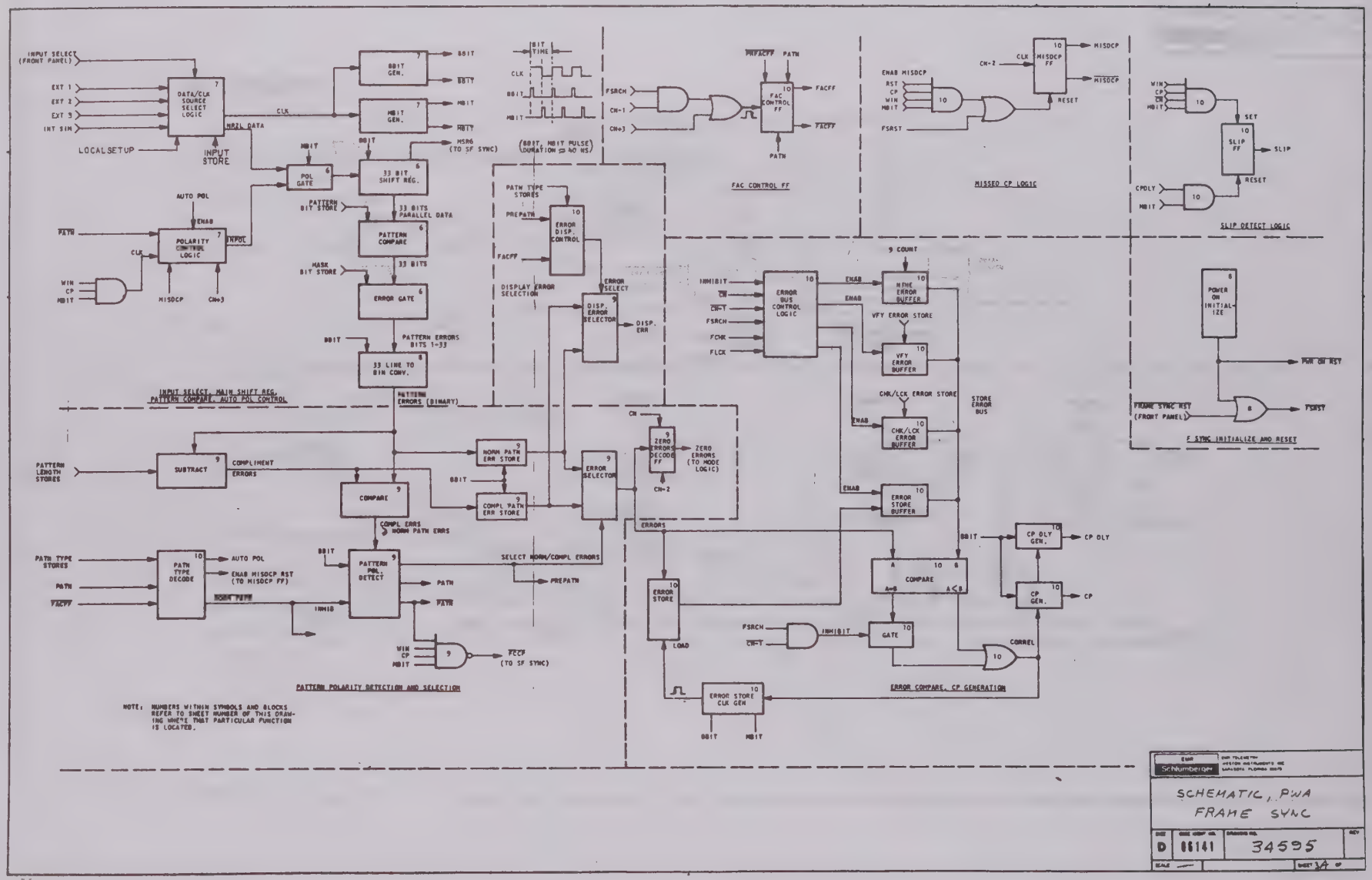
BSC	32956	710
BSC	28052	711

PARTS LIST

E. AHLEFELD 9/24/74
E. AHLEFELD 9/24/74
J. BISHOP 6/24/74
J. BISHOP 6/26/74

SCHEMATIC PWA
FRAME SYNC
(FUNCTION #4)

D 06141 29312



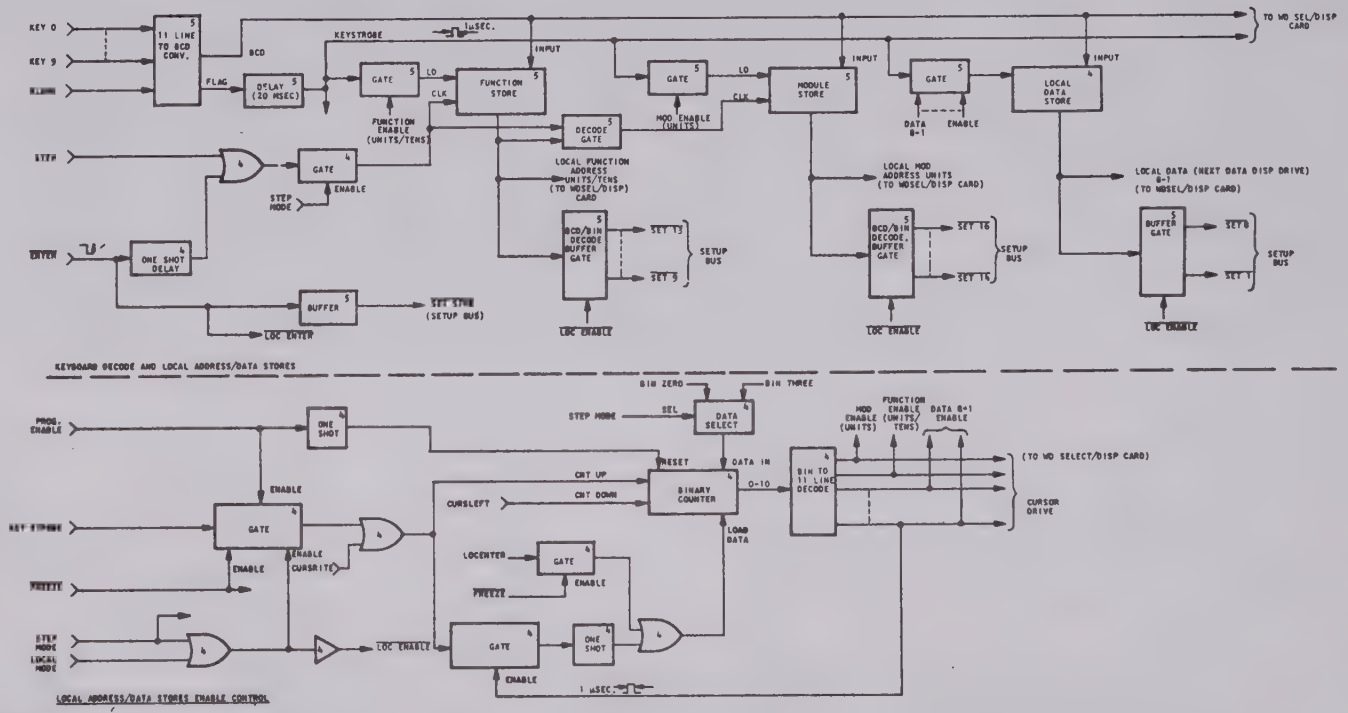
6-12

Schlumberger

SCHEMATIC, PWA
FRAME SYNC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	86141	34595	

SCALE — SHEET 3A OF



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

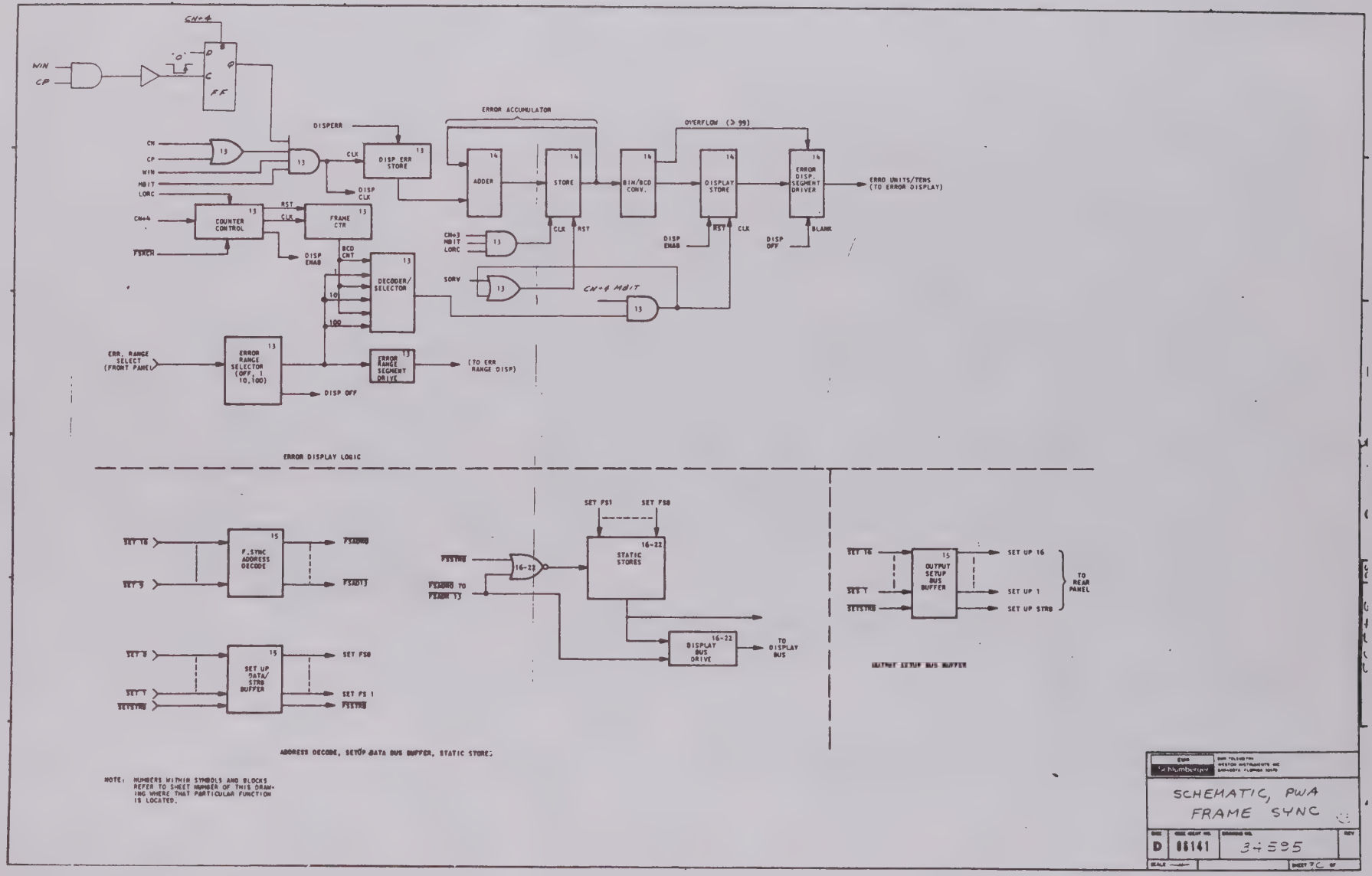
SCHEMATIC, PWA
FRAME SYNC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	88141	34595	

SCALE — SHEET 3 OF

6-11

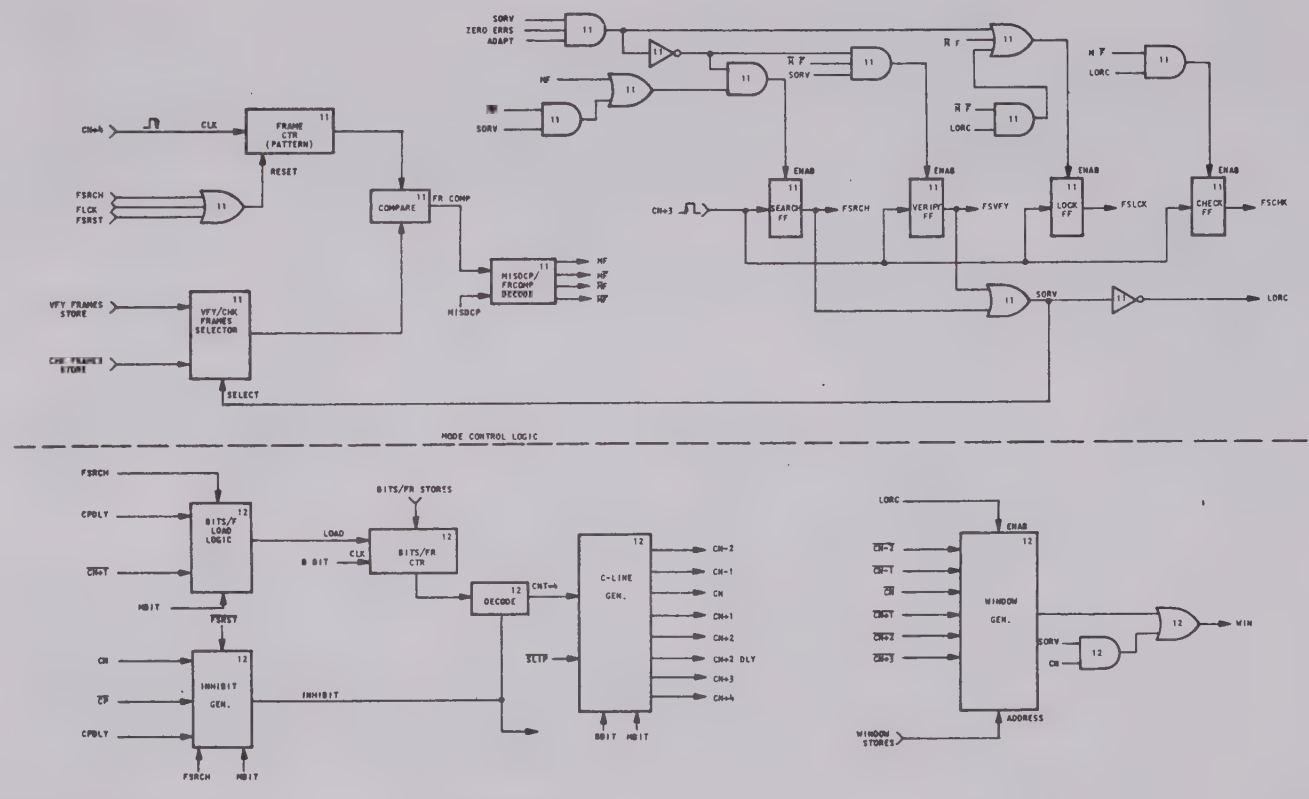
131 34595



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

SCHEMATIC, PWA
FRAME SYNC

D 86141 34595



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

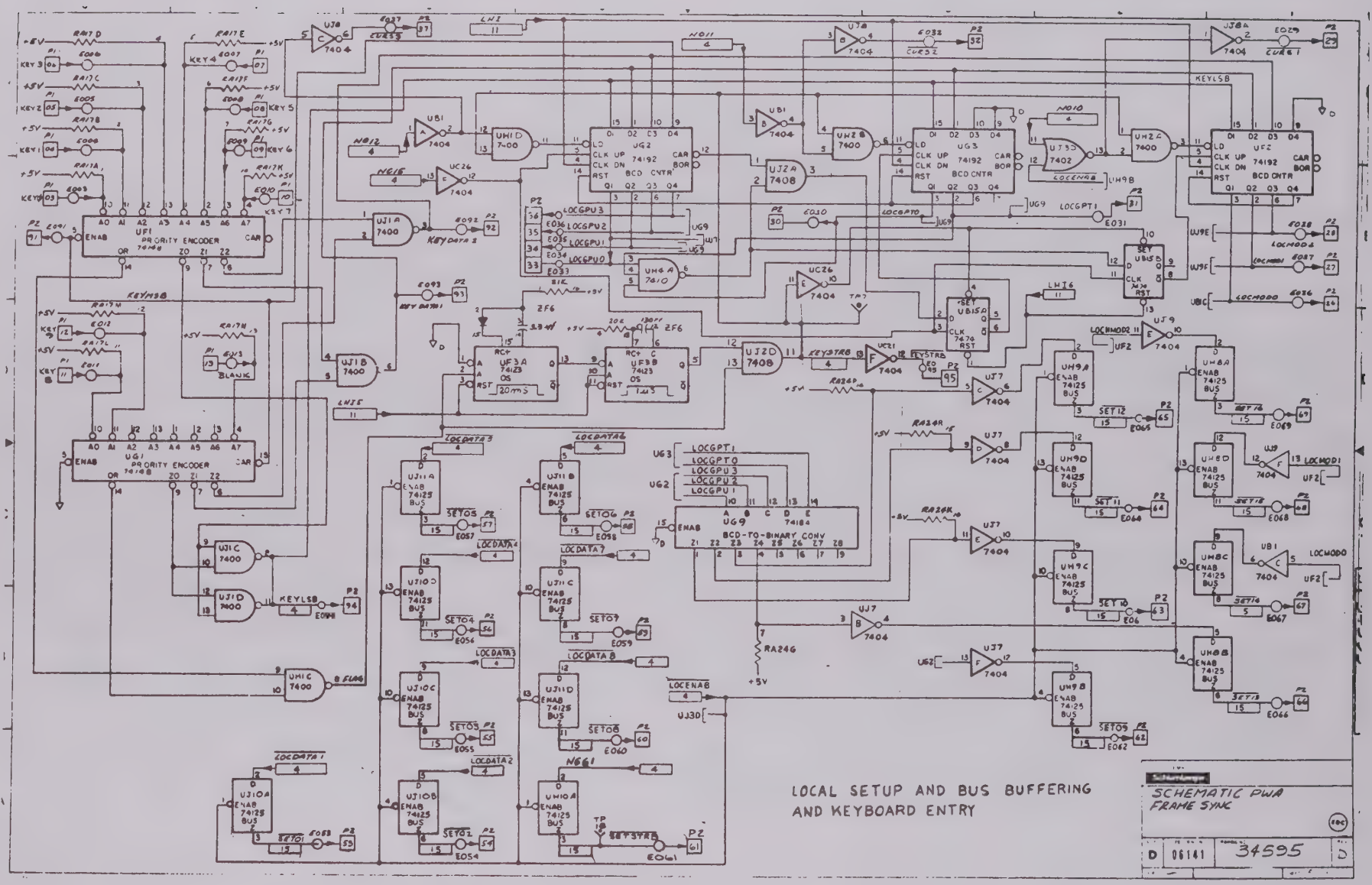
C-LINE AND WINDOW GENERATION

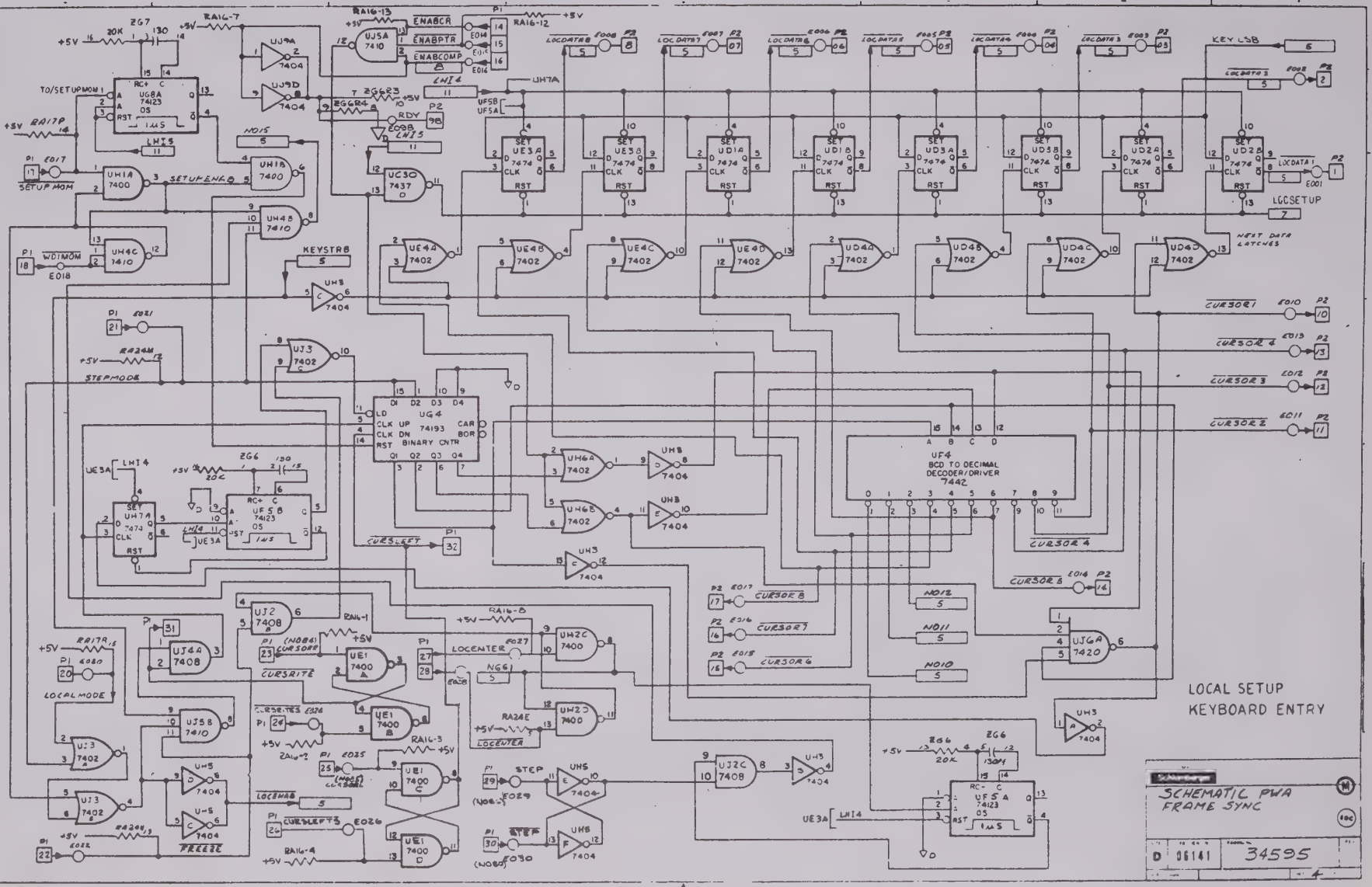
Schlumberger

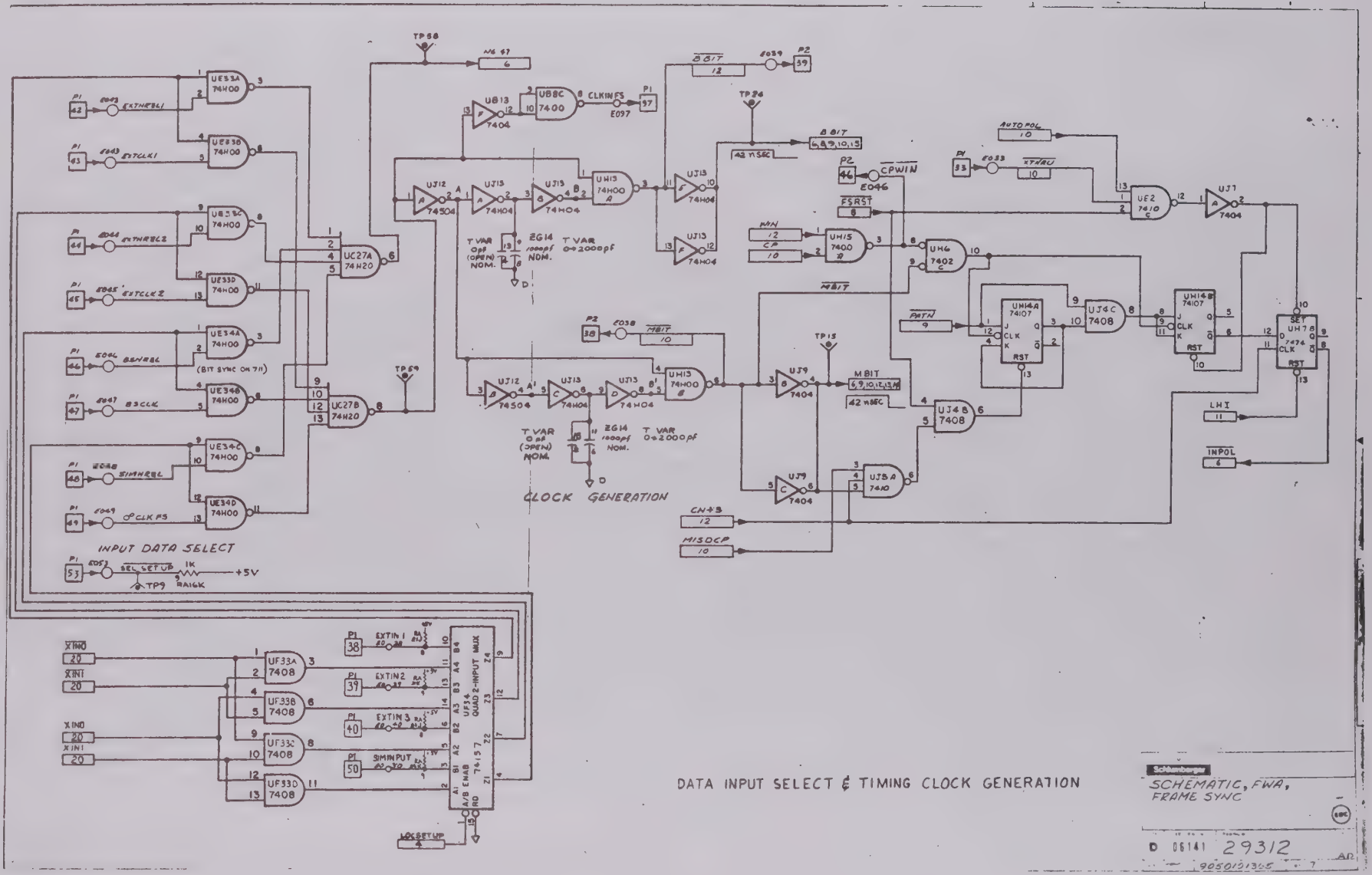
SCHEMATIC, PWA (M)
FRAME SYNC

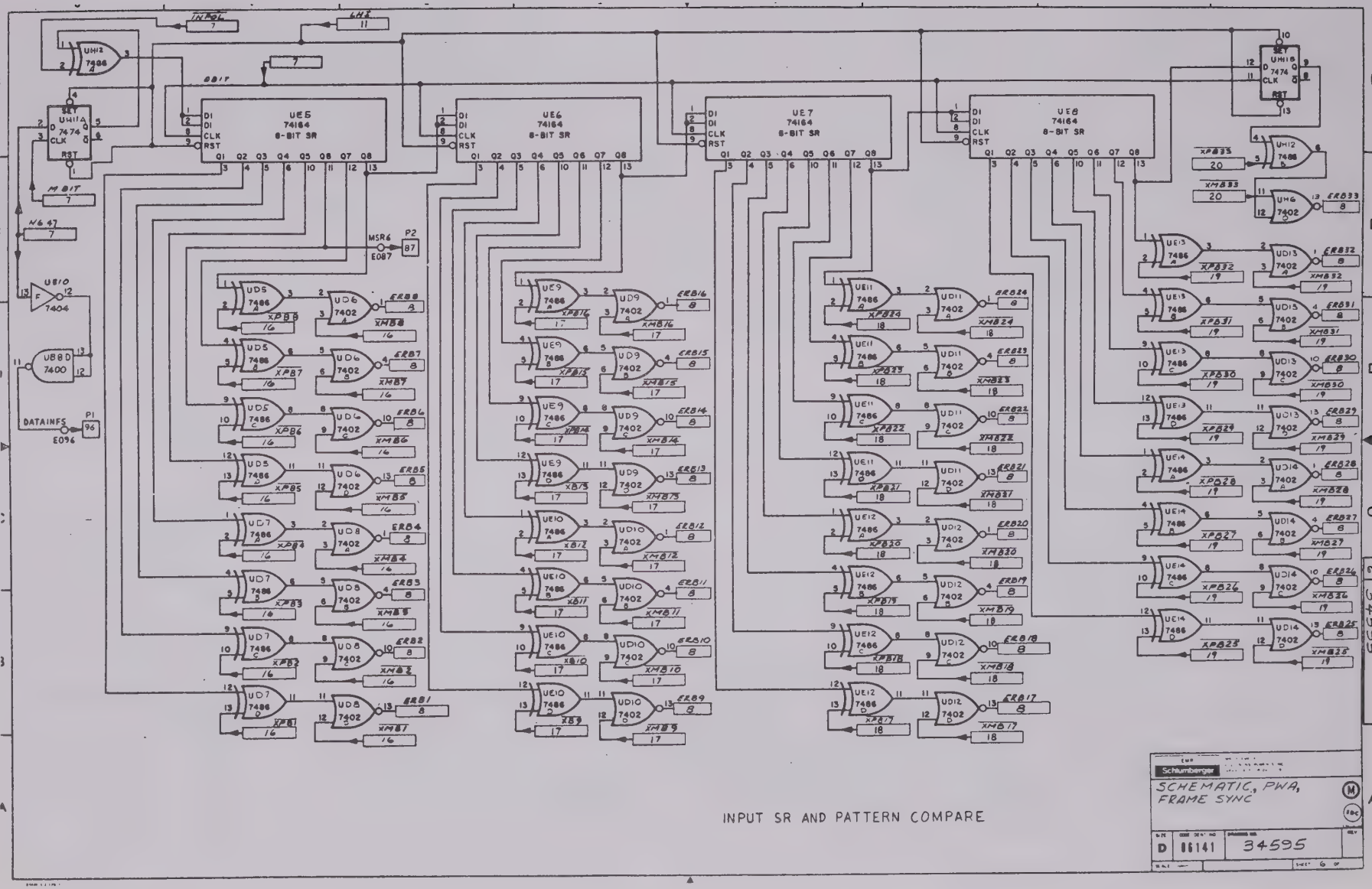
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	86141	34595	

SCALE — SHEET 38 OF

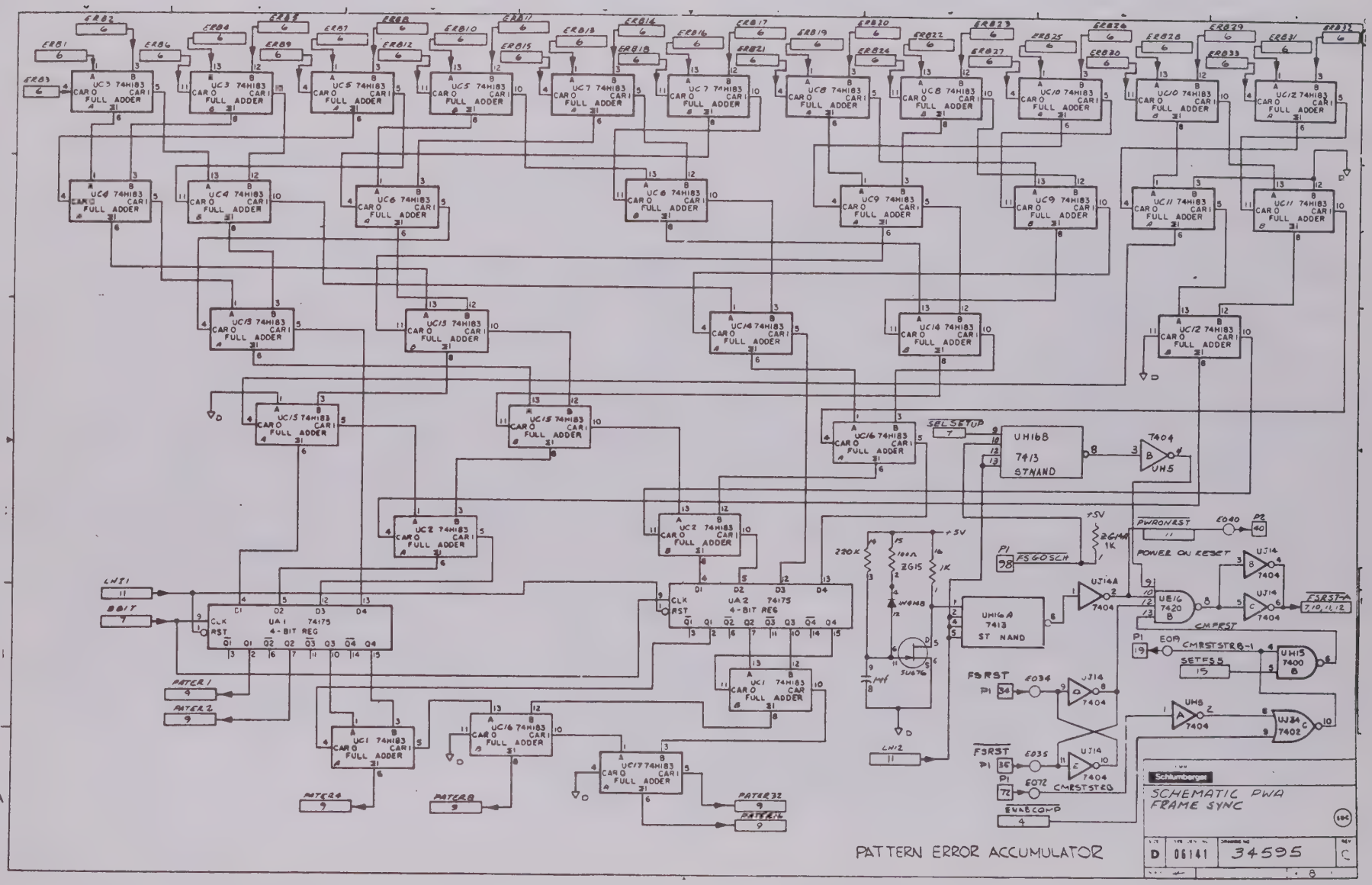

LOCAL SETUP AND BUS BUFFERING
AND KEYBOARD ENTRY
SCHEMATIC PWA
FRAME SYNC
D 06141 34595

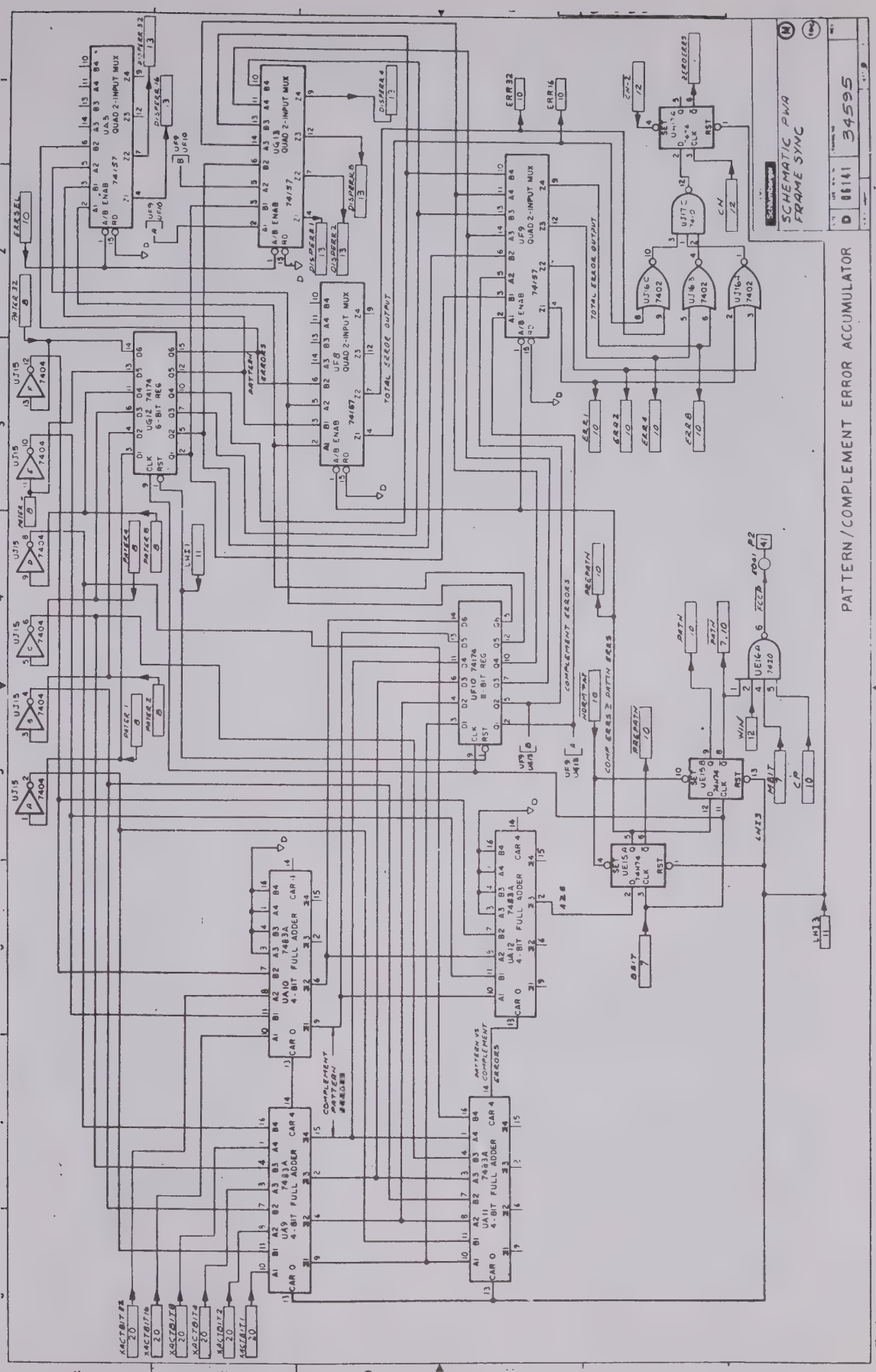

LOCAL SETUP
KEYBOARD ENTRY
SCHEMATIC PWA
FRAME SYNC
D 06141
34595

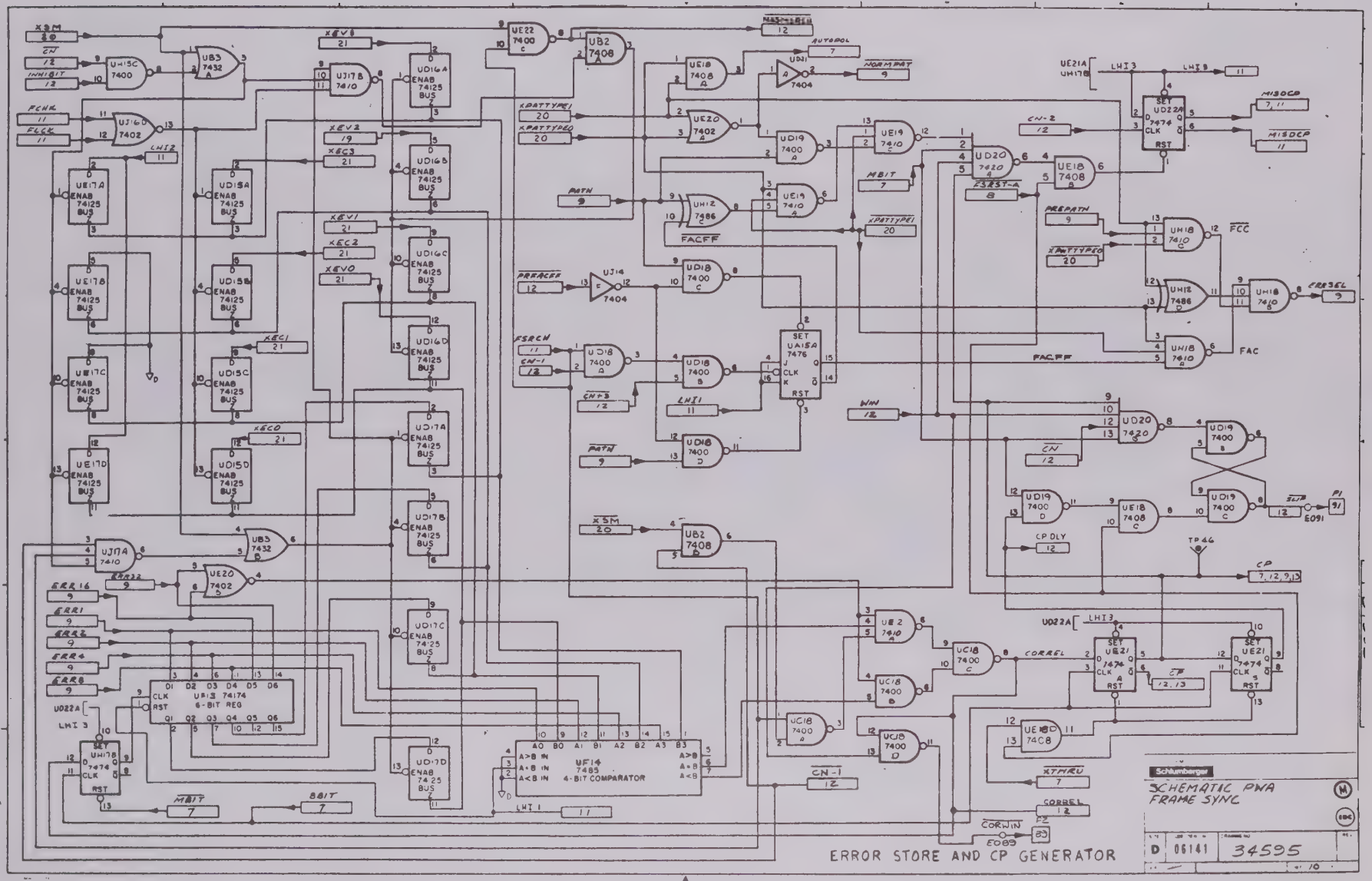

INPUT DATA SELECT
CLOCK GENERATION
DATA INPUT SELECT & TIMING CLOCK GENERATION
SCHEMATIC, FWA, FRAME SYNC
D 06141 29312

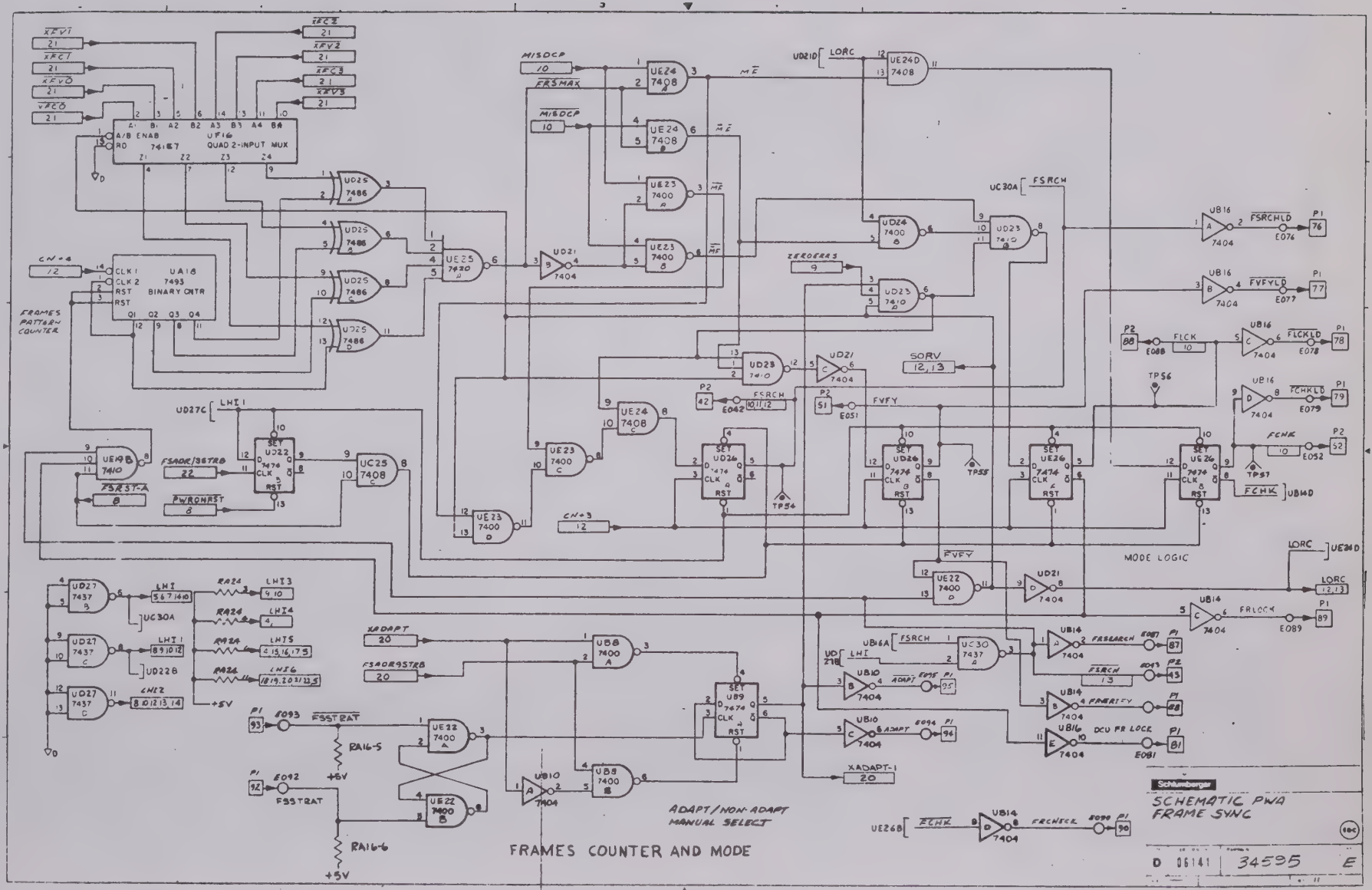


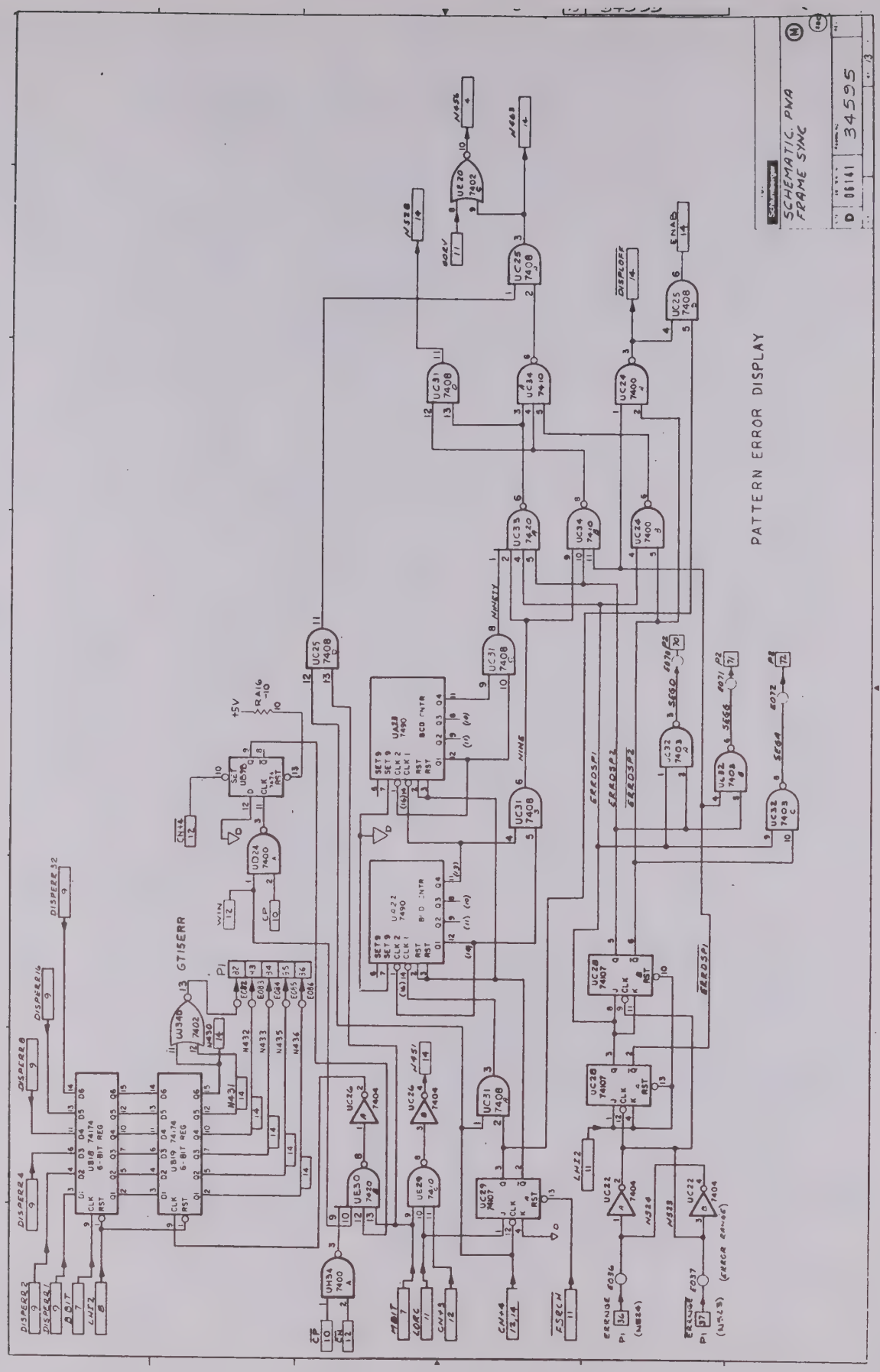
INPUT SR AND PATTERN COMPARE

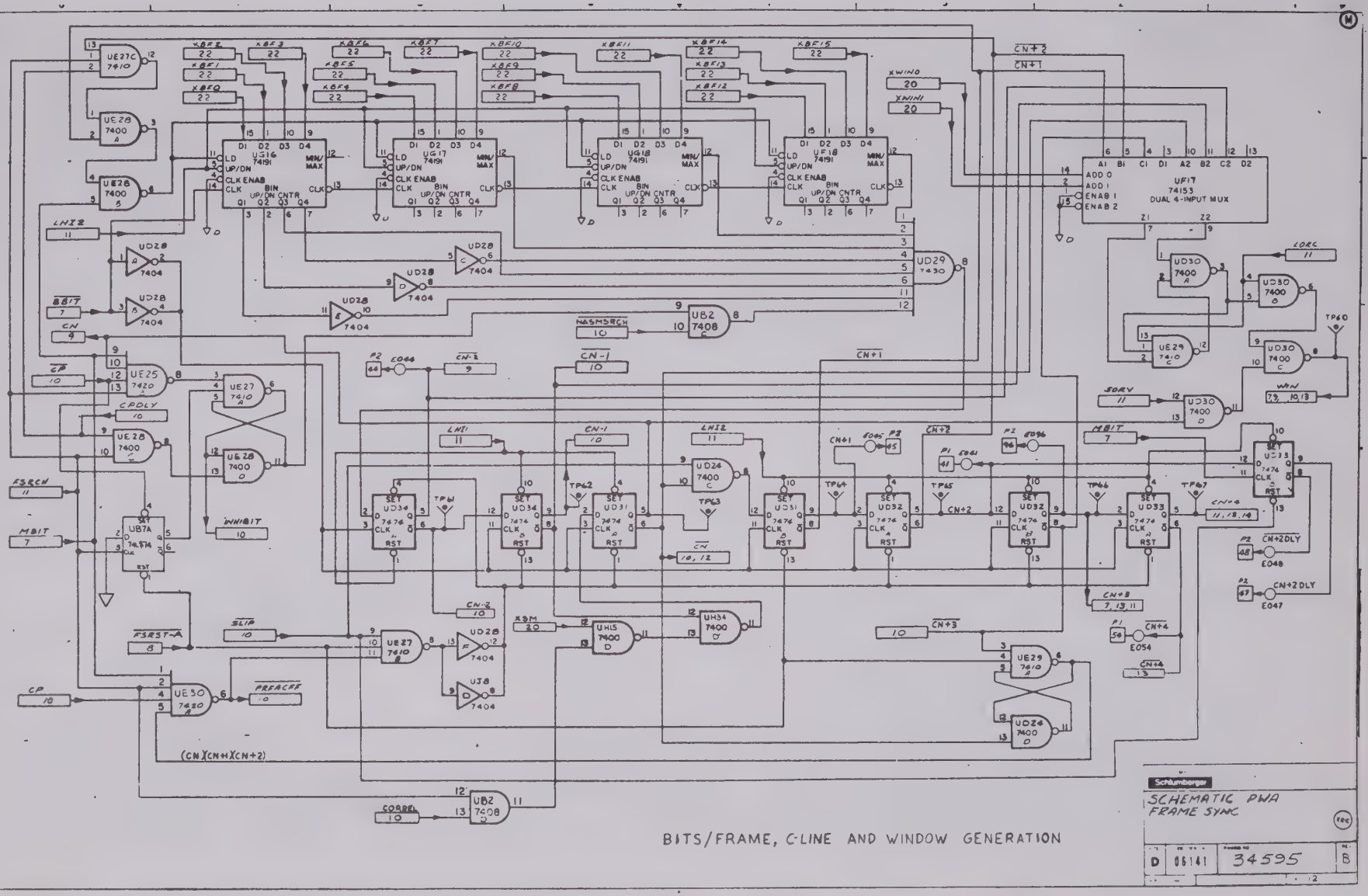

PATTERN ERROR ACCUMULATOR
SCHEMATIC PWA
FRAME SYNC
Schlumberger
D
06141
34595
UC3 74H183 FULL ADDER
UC5 74H183 FULL ADDER
UC7 74H183 FULL ADDER
UC8 74H183 FULL ADDER
UC10 74H183 FULL ADDER
UC12 74H183 FULL ADDER
UC4 74H183 FULL ADDER
UC6 74H183 FULL ADDER
UC9 74H183 FULL ADDER
UC11 74H183 FULL ADDER
UC13 74H183 FULL ADDER
UC14 74H183 FULL ADDER
UC15 74H183 FULL ADDER
UC16 74H183 FULL ADDER
UC2 74H183 FULL ADDER
UC1 74H183 FULL ADDER
UC17 74H183 FULL ADDER
UA1 74175 4-BIT REG
UA2 74175 4-BIT REG
UH16B 7413 ST NAND
UH16A 7413 ST NAND
UJ14 7404
UE16 7420
UH15 7400
UJ34 7402
SU676
SEL SETUP
PWRONRST
POWER ON RESET
FSGOSCH
FSRST
CMFRST
CMESTSTRB-1
CMESTSTEQ
EVAECOMP
LWI1
LWI2
BBIT
PATTER1
PATTER2
PATTER4
PATTER8
PATTER32
PATTER16
220K
2G15
1K
2GMΩ
1K
+5V
1mf

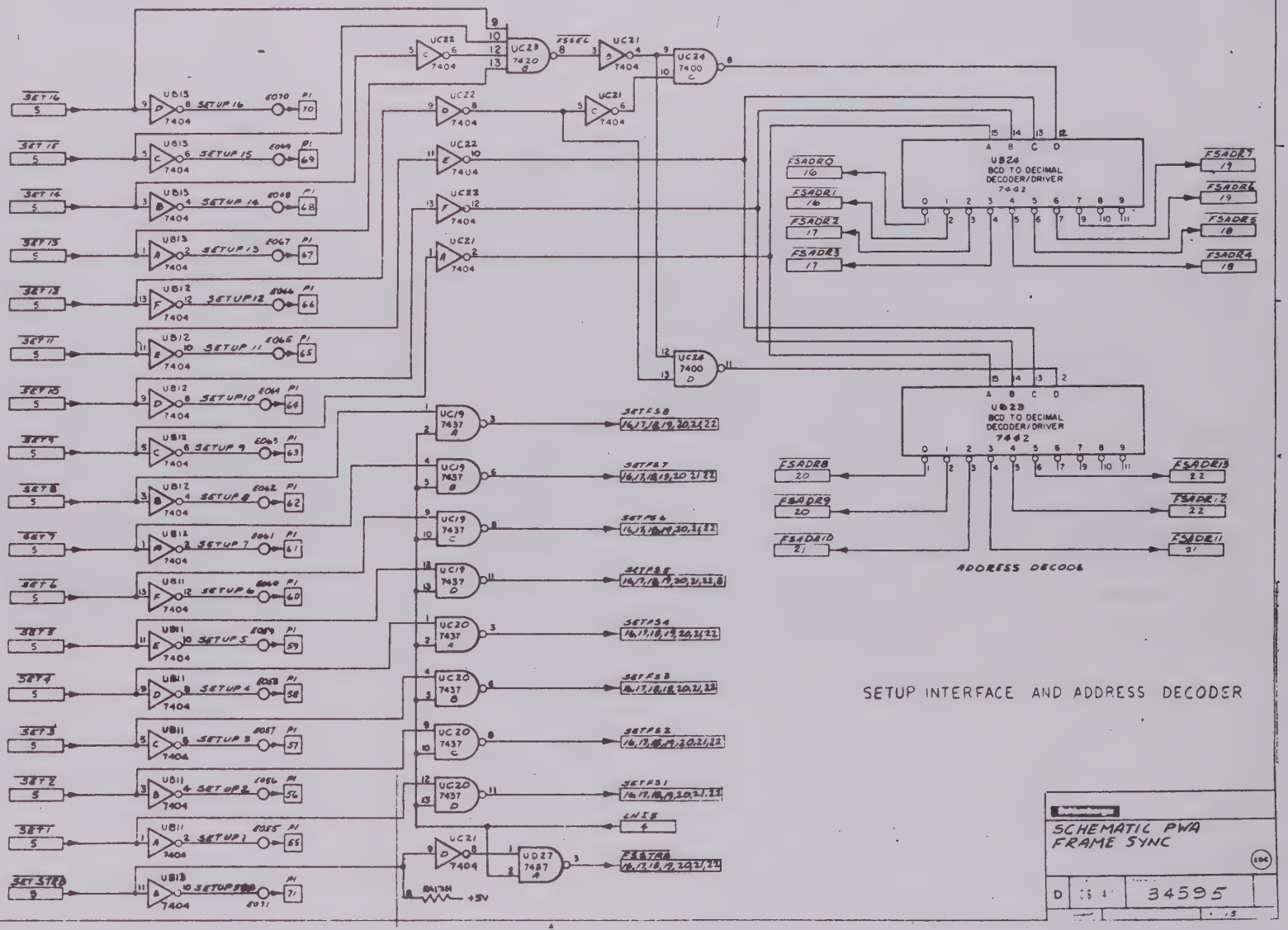

SCHEMATIC PWA
FRAME SYNC
D 06141 34595
PATTERN/COMPLEMENT ERROR ACCUMULATOR

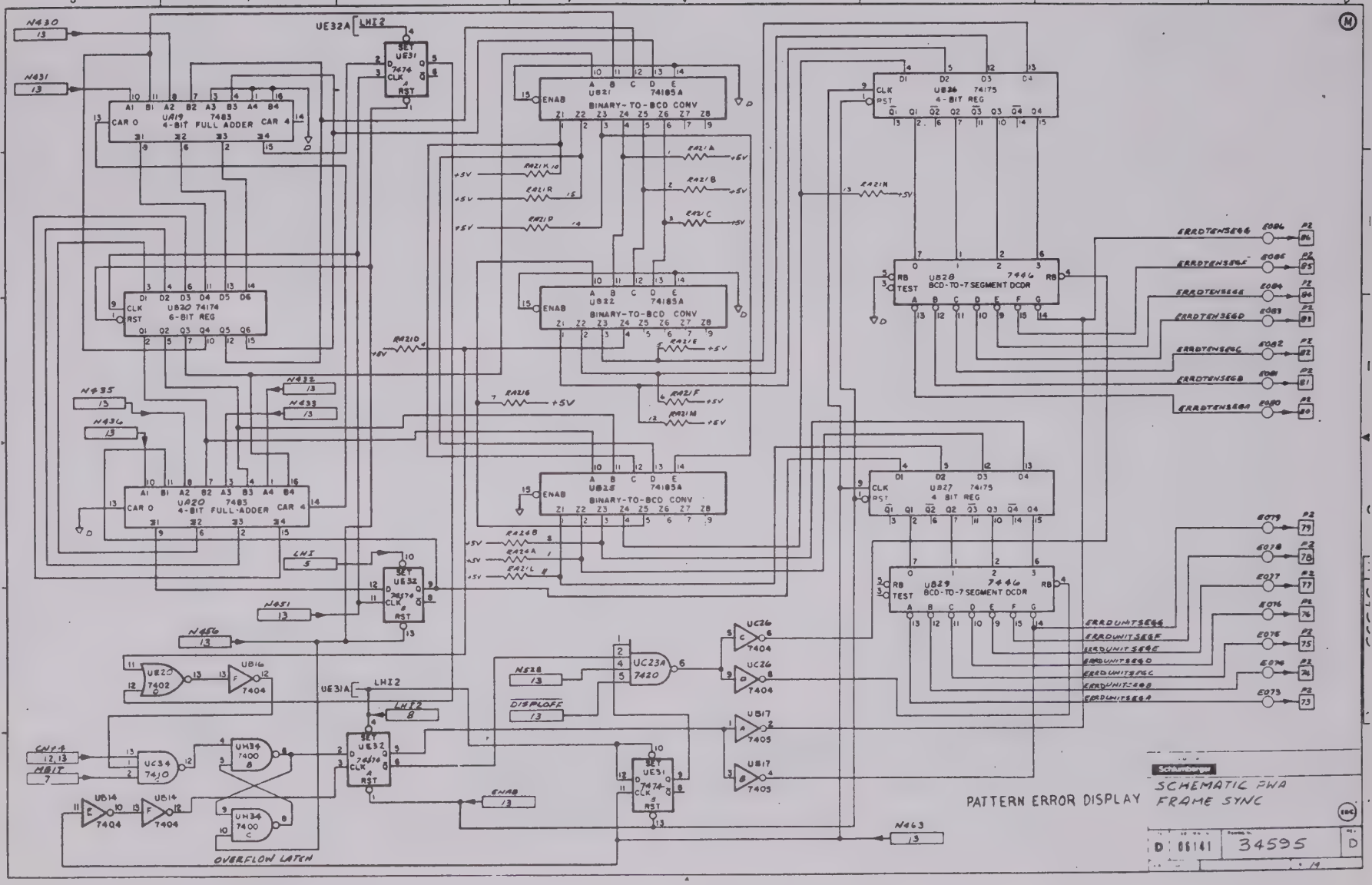

ERROR STORE AND CP GENERATOR
SCHEMATIC PWA
FRAME SYNC
Schlumberger
D 06141 34595

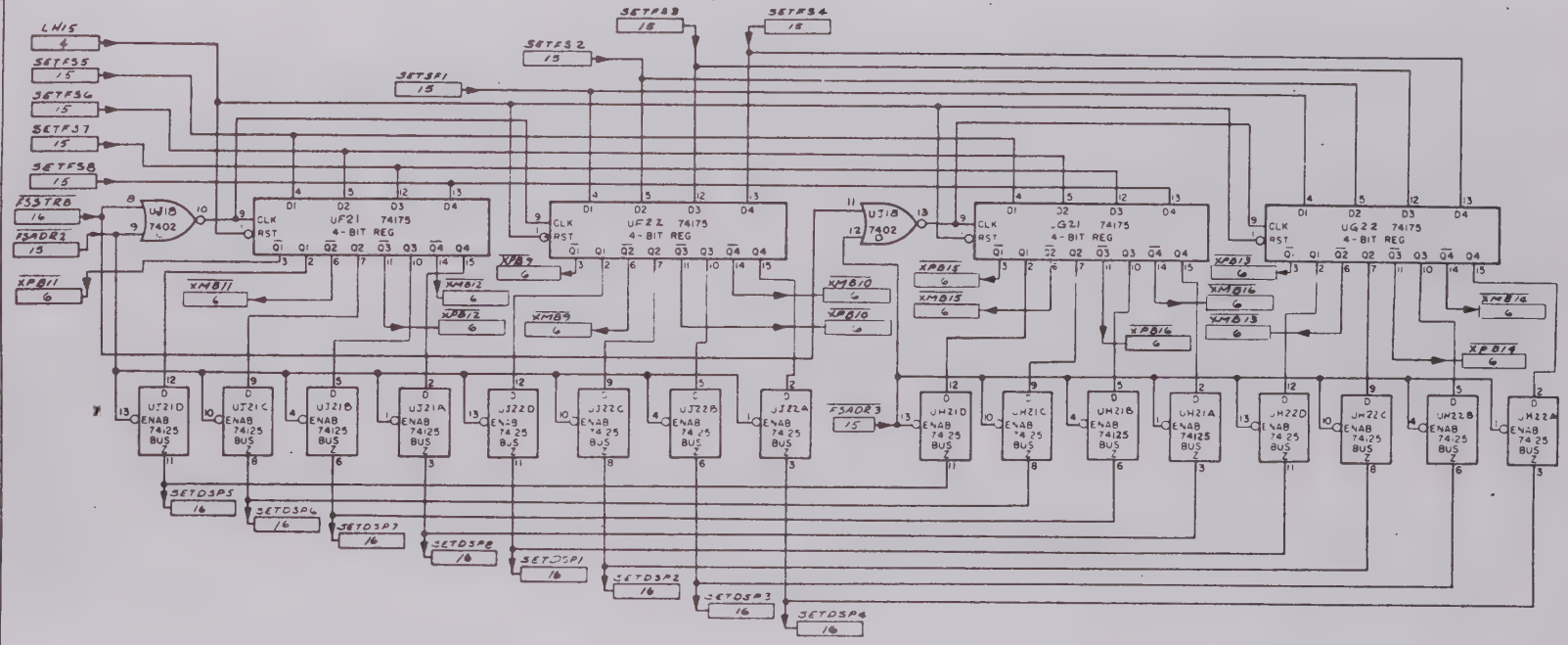

FRAMES COUNTER AND MODE
ADAPT/NON-ADAPT MANUAL SELECT
MODE LOGIC
SCHEMATIC PWA FRAME SYNC
D 06141 34595 E


PATTERN ERROR DISPLAY
SCHEMATIC PWA
FRAME SYNC
34595
GT15ERR


XBF2
XBF1
XBF0
XBF3
XBF6
XBF5
XBF4
XBF7
XBF10
XBF9
XBF8
XBF11
XBF14
XBF13
XBF12
XBF15
XWIN0
XWIN1
CN+2
CN+1
UE27C 7410
UE28 7400
UG16 74191
UG17 74191
UG18 74191
UF18 74191
UF17 74153 DUAL 4-INPUT MUX
UD28 7404
UD29 7430
UB2 7408
UE25 7420
UE27 7410
UE30 7430
UB7A 74S74
UD34 7474
UD31 7474
UD32 7474
UD33 7474
UJ3 7474
UD30 7400
UE29 7410
UD24 7400
UH15 7400
UH34 7400
UJ8 7404
LNI2
BBIT
CN
CP
CPDLY
FSRCH
MBIT
WNIBIT
FSRST-A
SLIP
PREACFF
CORREL
NASMSRCH
LNI1
CN-1
CN-2
CN
SORV
WIN
TP60
TP62
TP63
TP64
TP65
TP66
TP67
TPW
CN+3
CN+4
CN+2DLY
E044
E045
E046
E047
E048
E054
(CN)(CN+1)(CN+2)
BITS/FRAME, C-LINE AND WINDOW GENERATION
Schlumberger
SCHEMATIC PWA
FRAME SYNC
D
86141
34595
B


UB13 SETUP 16 E070 P1 70
UB13 SETUP 15 E069 P1 69
UB13 SETUP 14 E068 P1 68
UB13 SETUP 13 E067 P1 67
UB12 SETUP 12 E066 P1 66
UB12 SETUP 11 E065 P1 65
UB12 SETUP 10 E064 P1 64
UB12 SETUP 9 E063 P1 63
UB12 SETUP 8 E062 P1 62
UB12 SETUP 7 E061 P1 61
UB11 SETUP 6 E060 P1 60
UB11 SETUP 5 E059 P1 59
UB11 SETUP 4 E058 P1 58
UB11 SETUP 3 E057 P1 57
UB11 SETUP 2 E056 P1 56
UB11 SETUP 1 E055 P1 55
UB13 SETUP STRB E071 P1 71
UC22 UC23 UC21 UC24 UC26 UC25
FSSTL
UC19 UC20 UD27
SETFS8 SETFS7 SETFS6 SETFS5 SETFS4 SETFS3 SETFS2 SETFS1
4 WIRE
FSSTRB
PULL UP +5V
UB24 BCD TO DECIMAL DECODER/DRIVER 7442
UB23 BCD TO DECIMAL DECODER/DRIVER 7442
FSADR0 FSADR1 FSADR2 FSADR3
FSADR4 FSADR5 FSADR6 FSADR7
FSADR8 FSADR9 FSADR10
FSADR11 FSADR12 FSADR13
ADDRESS DECODE
SETUP INTERFACE AND ADDRESS DECODER
SCHEMATIC PWA
FRAME SYNC
34595

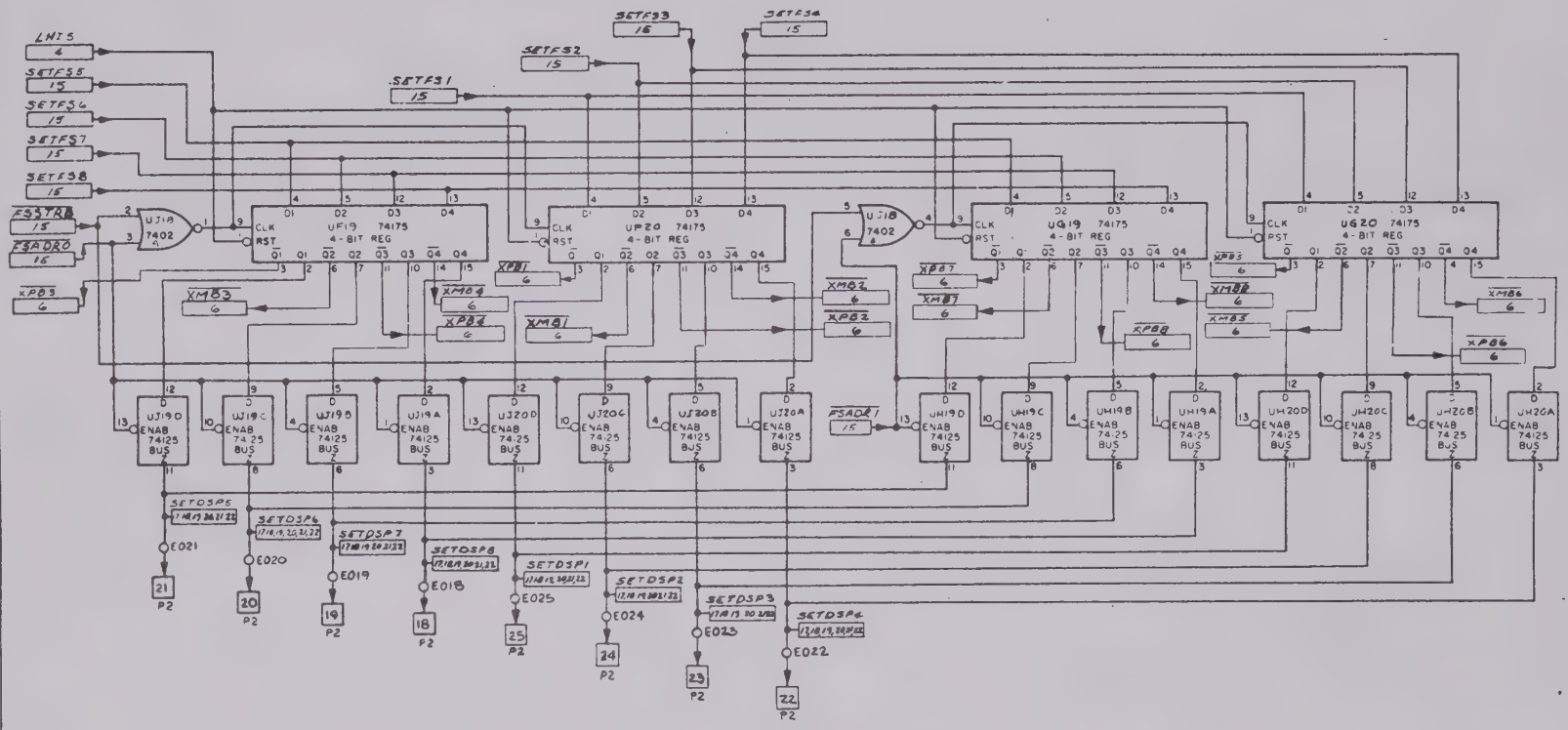

PATTERN ERROR DISPLAY
SCHEMATIC PWA
FRAME SYNC
D 06141
34595
OVERFLOW LATCH



SETUP STORES INSTRUCTIONS 1-2 THRU 1-3

SCHEMATIC, PWA, FRAME SYNC

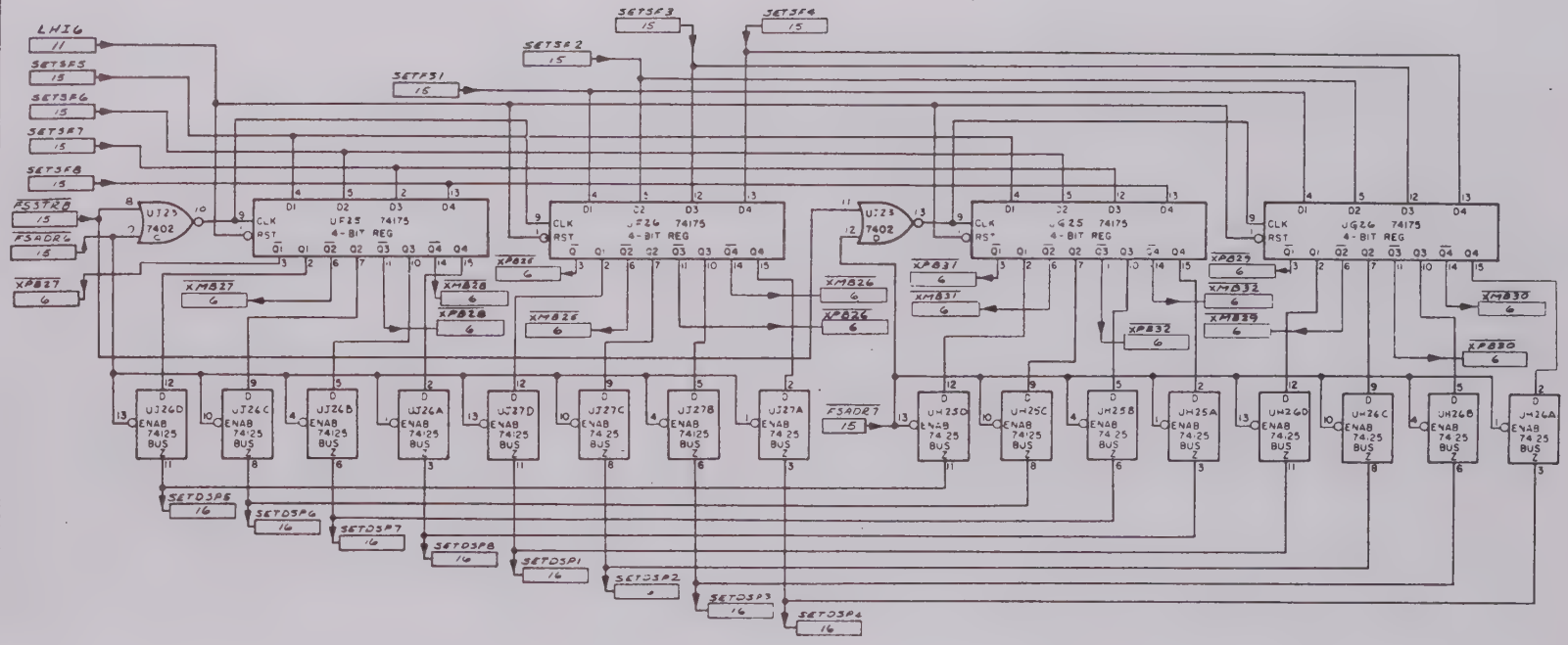
34595



SETUP STORES INSTRUCTIONS I-0 THRU I-1

SCHEMATIC PWA
FRAME SYNC

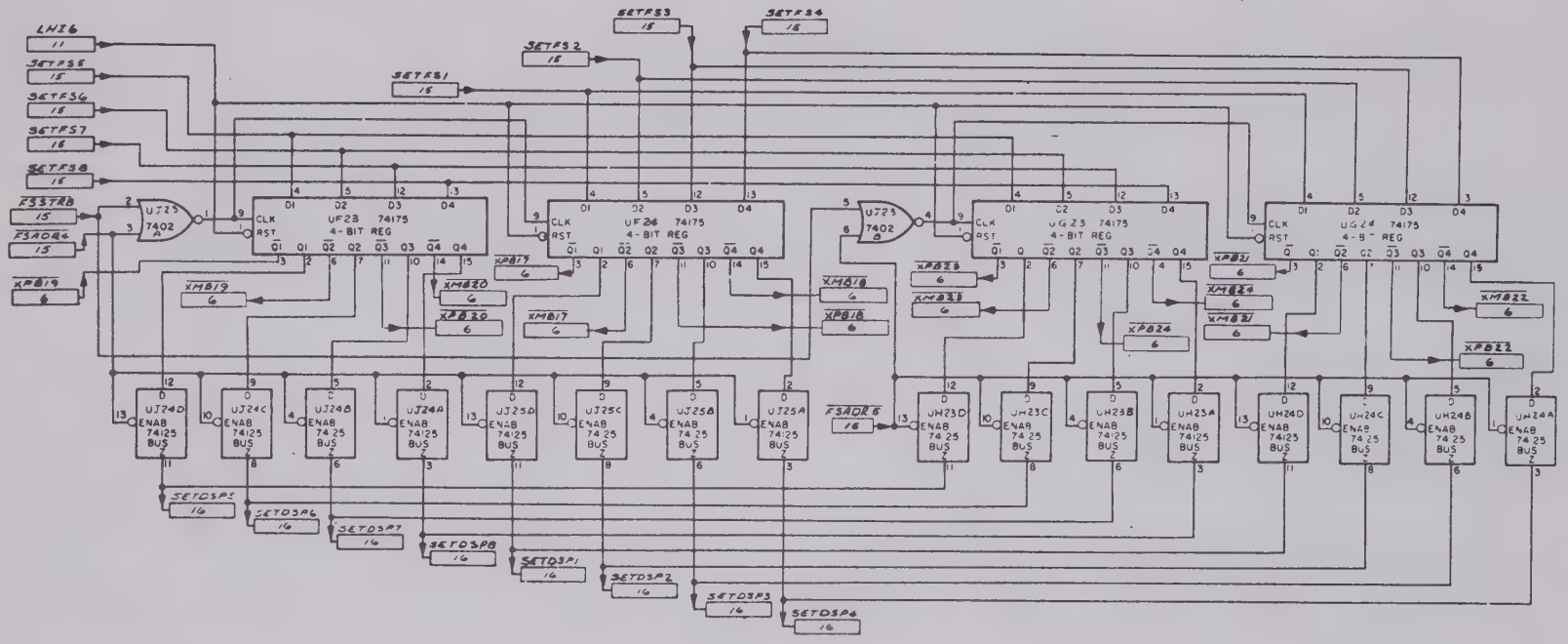
D | 34595



SETUP STORES INSTRUCTIONS 1-6 THRU 1-7

SCHEMATIC, PWA, FRAME SYNC

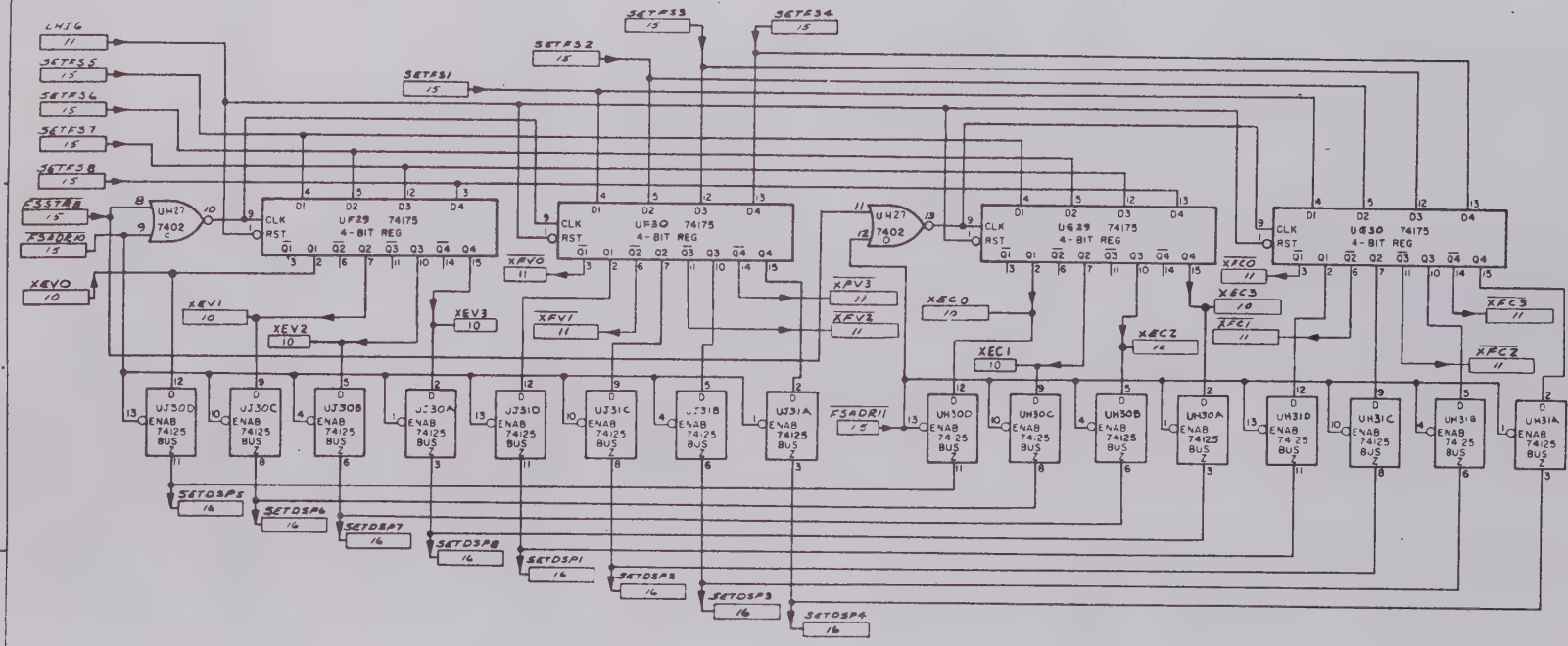
D 34595



SETUP STORES INSTRUCTIONS 1-4 THRU 1-5

SCHEMATIC PWA
FRAME SYNC

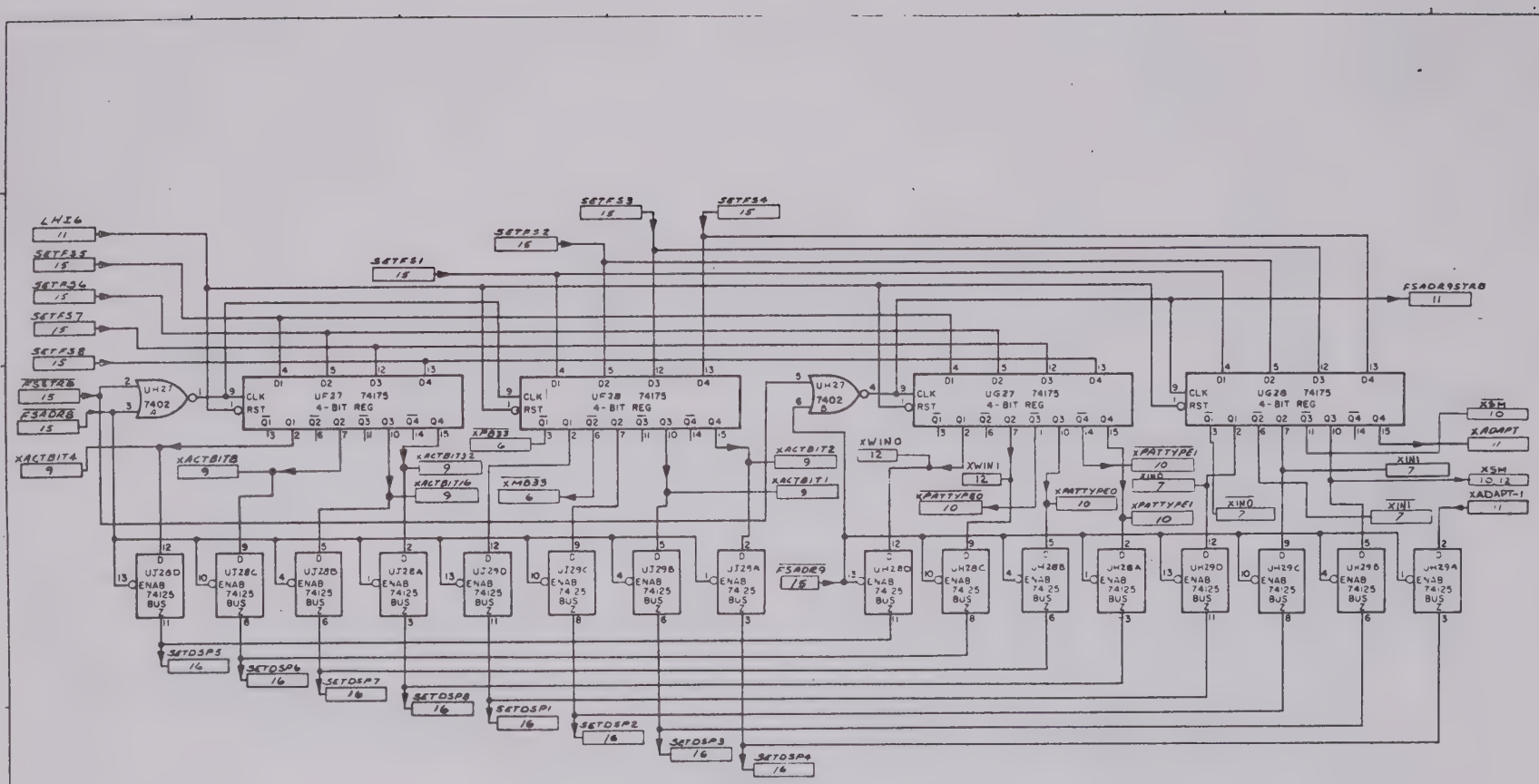
34595



SETUP STORES INSTRUCTIONS 1-10 THRU 1-11

SCHEMATIC, PWA, FRAME SYNC

D | 06 41 | 34595



SETUP STORES INSTRUCTIONS 1-8 THRU 1-9

P1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
1	D GND	1	B
2	+5V	1	B
3	KEY 0	5	FP/3
4	KEY 1	5	FP/3
5	KEY 2	5	FP/3
6	KEY 3	5	FP/3
7	KEY 4	5	FP/3
8	KEY 5	5	FP/3
9	KEY 6	5	FP/3
10	KEY 7	5	FP/3
11	KEY 8	5	FP/3
12	KEY 9	5	FP/3
13	BLANK	5	FP/3
14	ENABCR	4	FP/5
15	ENABPTR	4	FP/5
16	ENABCOMP	4	FP/5
17	SETUPMOM	4	FP/3
18	WDIMOM	4	FP/3
19	CMRSTSTRB-1	8	7/10
20	LOCAL MODE	4	FP/5
21	STEPMODE	4	FP/5
22	FREEEE	4	FP/3
23	CURSORR	4	FP/3
24	CURSRITE5	4	FP/3
25	CURSORL	4	FP/3
26	CURSLEFT5	4	FP/3
27	LOCENTER	4	FP/3
28	LOCENTER	4	FP/3
29	STEP	4	FP/3
30	STEP	4	FP/3
31	CURSRITE	4	8/10
32	CURSLEFT	4	8/10
33	XTHRU	7	8/24
34	FSRST	8	FP/4
35	FSRST	8	FP/4
36	ERRNGE	13	FP/3
37	ERRNGE	13	FP/3
38	EXTIN 1	7	FP/4
39	EXTIN 2	7	FP/4
40	EXTIN 3	7	FP/4
41	CN+2	12	5/4, 5/16, 8/8
42	EXTNRZL1	7	RP/J22
43	EXTCLK 1	7	RP/J23
44	EXTNRZL 2	7	RP/J24
45	EXTCLK 2	7	RP/J25
46	EXTNRZL3	7	RP/J26
47	EXTCLK3	7	RP/J27
48	SIMNRZL	7	6/7
49	0° CLK	7	6/5
50	SIMINPUT	7	FP/4

P1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51	D GND	1	B
52	+5V	1	B
53	SEL SET UP	7	10/5, 5/9, 5/21
54	CN+4	12	5/8, 5/20
55	SET UP 1	15	RP/J32PA2
56	SET UP 2	15	RP/J32PA4
57	SET UP 3	15	RP/J32PA6
58	SET UP 4	15	RP/J32PA8
59	SET UP 5	15	RP/J32PA10
60	SET UP 6	15	RP/J32PA12
61	SET UP 7	15	RP/J32PD13
62	SET UP 8	15	RP/J32PC2
63	SET UP 9	15	RP/J32PC4
64	SET UP 10	15	RP/J32PC6
65	SET UP 11	15	RP/J32PC8
66	SET UP 12	15	RP/J32PC10
67	SET UP 13	15	RP/J32PC12
68	SET UP 14	15	RP/J32PE2
69	SET UP 15	15	RP/J32PE4
70	SET UP 16	15	RP/J32PE6
71	SET UP STRB	15	RP/J32PE8
72	CMRSTSTRB	8	10/5
73	/TIMENAB	7	8/19
74	TIMENAB	7	RP/J31PN13
75	/WDINC	7	8/9
76	FSRCHLD	11	FP/5
77	FVFYLD	11	FP/5
78	FLCKLD	11	FP/5
79	FCHKLD	11	FP/5
80	WDINC	7	RP/J34PE8
81	DCU FR LOCK	11	RP/J38PE12
82	GTISERR	13	8/20
83	N432	13	8/20
84	N433	13	8/20
85	N435	13	8/20
86	N436	13	8/20
87	FRSEARCH	11	RP/J33PE8
88	FRVERIFY	11	RP/J33PE10
89	FRLOCK	11	RP/J33PE12
90	FRCHECK	11	RP/J33PH13
91	SLIP	10	8/20
92	FSSTRAT	11	FP/4
93	FSSTRAT	11	FP/4
94	ADAPT	11	FP/4
95	ADAPT	11	FP/4
96	DATAINFS	6	FP/4
97	CLK INFS	7	FP/4
98	/FS GO SCH	8	2/2
99	/WDRS	7	8/9
100	WDRS	11	RP/J34PE10

P2

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
1	LOCDATA 1	4	8/16
2	LOCDATA 2	4	8/16
3	LOCDATA 3	4	8/16
4	LOCDATA 4	4	8/16
5	LOCDATA 5	4	8/16
6	LOCDATA 6	4	8/18
7	LOCDATA 7	4	8/18
8	LOCDATA 8	4	8/18
9	/PAR-ERR	7	8/9
10	CURSOR 1	4	8/16
11	CURSOR 2	4	8/16
12	CURSOR 3	4	8/16
13	CURSOR 4	4	8/16
14	CURSOR 5	4	8/16
15	CURSOR 6	4	8/18
16	CURSOR 7	4	8/18
17	CURSOR 8	4	8/18
18	SETDSP 8	16	5/6, 5/18, 7/7, 8/22, 10/6
19	SETDSP 7	16	
20	SETDSP 6	16	
21	SETDSP 5	16	
22	SETDSP 4	16	
23	SETDSP 3	16	
24	SETDSP 2	16	
25	SETDSP 1	16	5/6, 5/18, 7/7, 8/22, 10/6
26	LOCMOD 0	5	8/27
27	LOCMOD 1	5	8/27
28	LOCMOD 2	5	8/27
29	CURS 1	5	8/27
30	LOCGPT 0	5	8/27
31	LOCGPT 1	5	8/27
32	CURS 2	5	8/25
33	LOCGPU 0	5	8/25
34	LOCGPU 1	5	8/25
35	LOCGPU 2	5	8/25
36	LOCGPU 3	5	8/25
37	CURS 3	5	8/25
38	MOTF	7	5/4, 5/16, 8/7, 2/3
39	BDIT	7	5/4, 5/16, 8/7, 2/3
40	DUCONREST	9	5/2, 5/21, 10/2, 2/2, 8/24
41	FCCB	9	5/8, 5/20
42	FSRCH	11	9/5
43	FSRCH	11	5/8, 5/20, 8/7, 2/3
44	CN-2	12	5/8, 5/20, 8/20
45	CN+1	12	8/7, 2/2
46	CRWIN	7	8/7
47	CN+2DLY	12	5/11, 5/23
48	CN+2DLY	12	8/4
49	+5V	1	B
50	D GND	1	B

P2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51	FVFY	11	8/20
52	FCHK	11	8/20
53	SET01	5	5/4, 5/14, 7/13, 8/20, 10/4, 2/3
54	SET02	5	
55	SET03	5	
56	SET04	5	
57	SET05	5	
58	SET06	5	
59	SET07	5	
60	SET08	5	5/12, 5/24, 7/13, 8/20, 10/4
61	SETSTRB	5	5/12, 5/24, 7/13, 8/20, 10/4
62	SET09	5	
63	SET 10	5	
64	SET 11	5	
65	SET 12	5	
66	SET 13	5	
67	SET 14	5	
68	SET 15	5	
69	SET 16	5	5/12, 5/24, 7/13, 8/20, 10/4, 2/3
70	SEGD	13	FP/5
71	SEGG	13	
72	SEGA	13	
73	ERRDUNITSEGA	14	
74	ERRDUNITSEGB	14	
75	ERRDUNITSEGC	14	
76	ERRDUNITSEGD	14	
77	ERRDUNITSEGE	14	
78	ERRDUNITSEGF	14	
79	ERRDUNITSEGG	14	
80	ERRDTENSEGA	14	
81	ERRDTENSEGB	14	
82	ERRDTENSEGC	4	
83	ERRDTENSEGD	14	
84	ERRDTENSEGE	14	
85	ERRDTENSEGF	14	
86	ERRDTENSEGG	14	FP/5
87	MSR 6	6	5/7, 5/19, 8/4
88	FLCK	11	8/20, 9/6
89	CRWIN	10	8/7
90	PAR DATA 1	7	RP/J31PG2
91	KEYMSB	5	8/10
92	KEY DATA 2	5	8/10
93	KEY DATA 1	5	8/10
94	KEY LSB	5	8/10
95	KEYSTRB	5	8/10
96	CN-3	12	5/8, 5/20, 8/15
97	PAR DATA 2	7	RP/J33PG2
98	EOJ	4	RP/J33PG6
99	-5V	1	B
100	D GND	1	B

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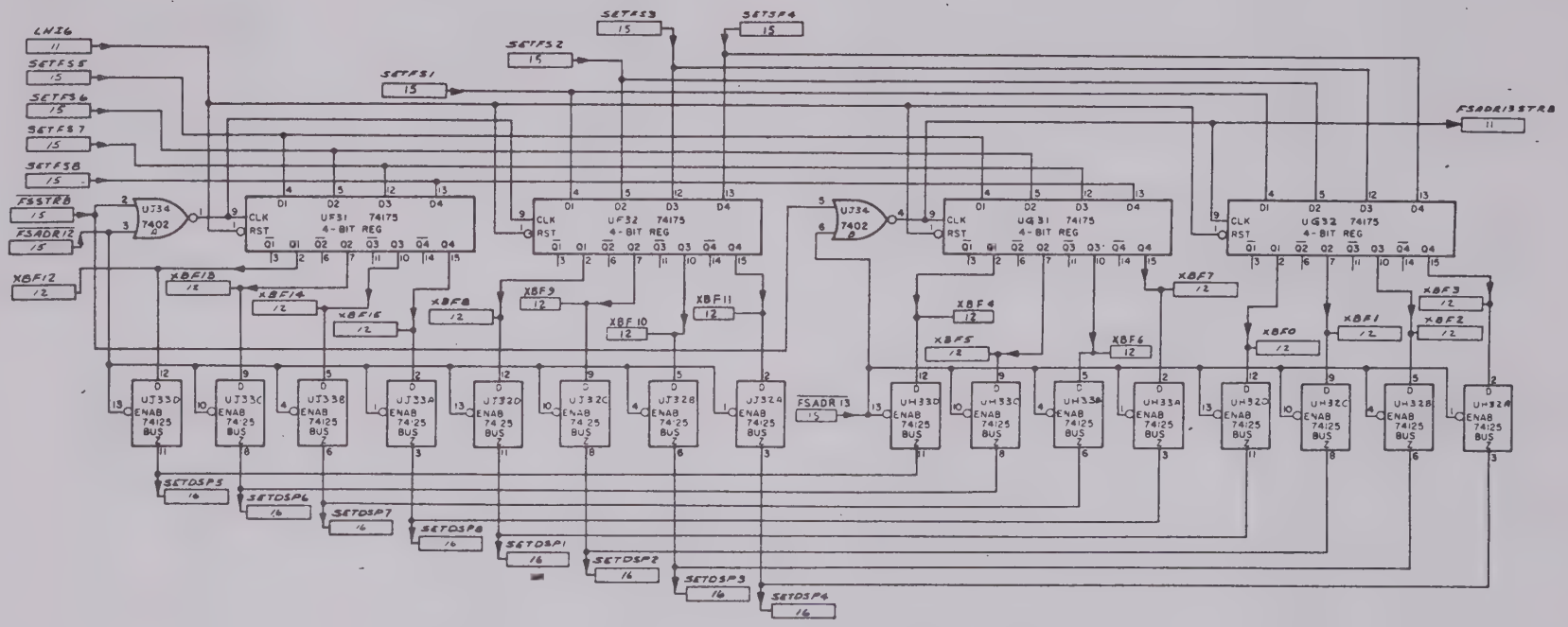
SCHEMATIC, PWA,
FRAME SYNC
FUNCTION #4

SIZE	CODE IDENT NO	DRAWING NO	REV
D	06141	34595	E

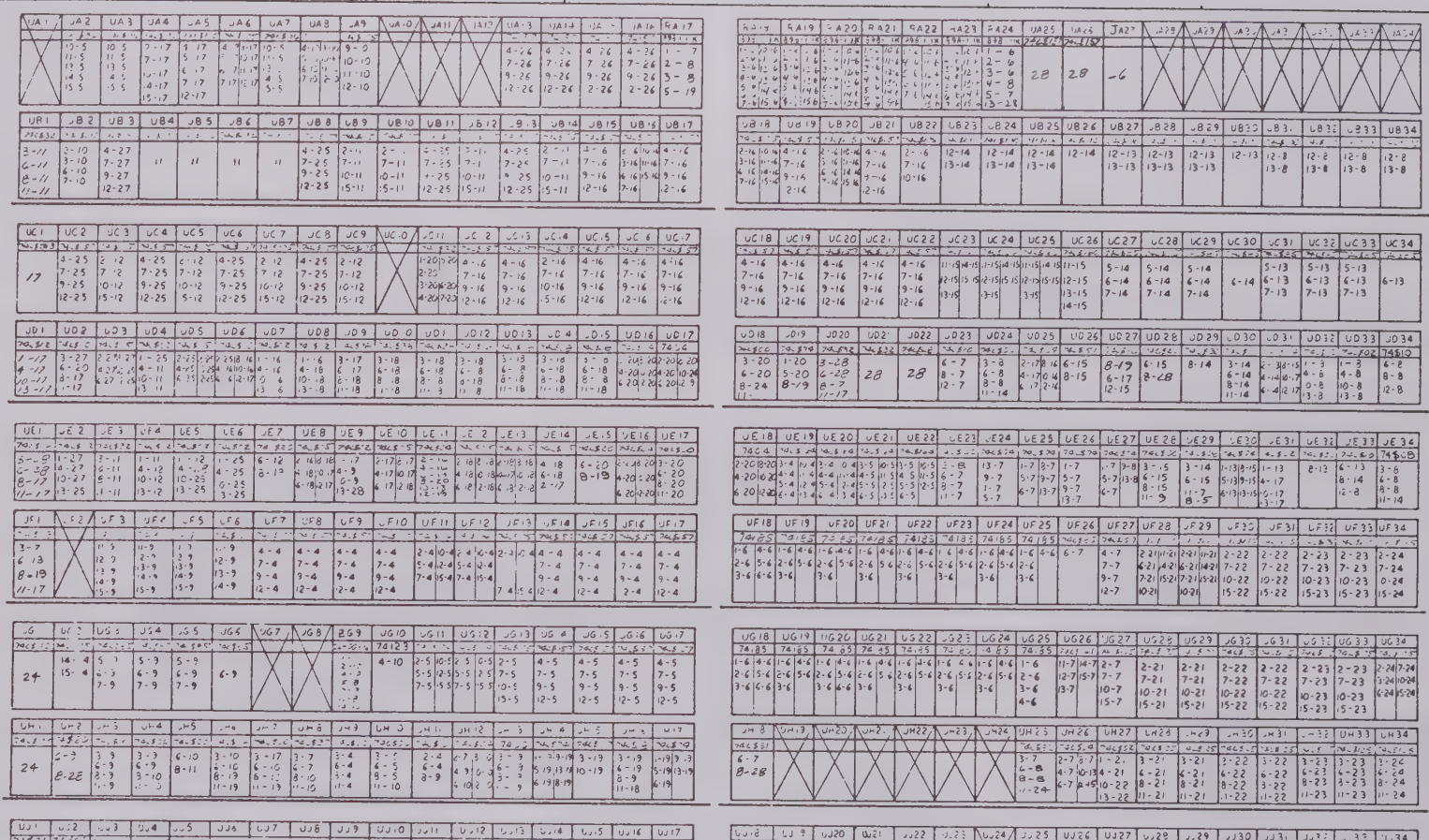
SHEET 23



SETUP STORES INSTRUCTIONS 1-12 & 1-13

SCHEMATIC, PWA, FRAME SYNC

D | 34595



SCHEM, PWA,
WORD SELECT & DISPLAY

D 34597 L

6-36

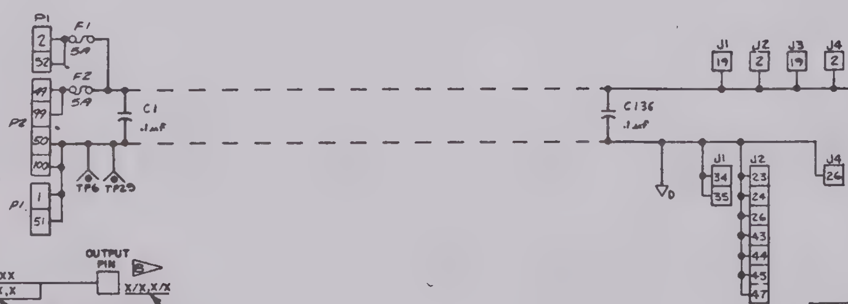
COMPONENT CHART	
	UNUSED NUMBER
UA26	UA1,10,11,12,17-25 28-34
UB34	
UC34	UC19
UD34	
UE34	
UF34	UF2
UG34	UG7
UH34	UH19-24
UJ34	UJ24
TP32	TP1-8, 11, 15, 7&8
C136	
F2	
J4	
P4	

UNUSED CIRCUITS		
REF DES	TYPE	UNUSED CIRCUITS
UD18	7400	D
RA17	898-1-R	D,E,F,G H,J,K,L,M,N,P,R
RA18	898-1-R	H,J,L
RA19	898-1-R	H,J
RA20	898-1-R	H,J
RA21	898-1-R	H,J
RA22	898-1-R	H,J
RA23	898-1-R	H,J
RA24	898-1-R	F,G,H,J K,L,M, P,R

POWER PINS			POWER PINS			POWER PINS			POWER PINS		
REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND
UA2	5	12	UB27	16	8	UC32	16	8	UE6	14	7
UA3	5	12	UB28	16	8	UC33	16	8	UE7	14	7
UA4	16	8	UB29	16	8	UC34	16	8	UE8	14	7
UA5	16	8	UB30	16	8	UD2	14	7	UE9	14	7
UA6	16	8	UB31	16	8	UD3	14	7	UE10	14	7
UA7	5	12	UB32	16	8	UD4	14	7	UE11	14	7
UA8	16	8	UB33	16	8	UD5	14	7	UE12	14	7
UA9	16	8	UB34	16	8	UD6	14	7	UE13	14	7
UA13	16	8	UC2	16	8	UD7	14	7	UE14	14	7
UA14	16	8	UC3	16	8	UD8	14	7	UE15	14	7
UA15	16	8	UC4	16	8	UD9	14	7	UE16	14	7
UA16	16	8	UC5	16	8	UD10	14	7	UE17	14	7
UB2	16	8	UC6	16	8	UD11	14	7	UE18	14	7
UB3	16	8	UC7	16	8	UD12	14	7	UE19	14	7
UB4	16	8	UC8	16	8	UD13	14	7	UE20	14	7
UB5	16	8	UC9	16	8	UD14	14	7	UE21	14	7
UB6	16	8	UC11	16	8	UD15	14	7	UE22	14	7
UB7	16	8	UC12	16	8	UD16	14	7	UE23	14	7
UB8	16	8	UC13	16	8	UD17	14	7	UE24	14	7
UB9	16	8	UC14	16	8	UD18	14	7	UE25	14	7
UB10	16	8	UC15	16	8	UD19	14	7	UE26	14	7
UB11	16	8	UC16	16	8	UD23	14	7	UE27	14	7
UB12	16	8	UC17	16	8	UD24	14	7	UE28	14	7
UB13	16	8	UC18	16	8	UD25	14	7	UE29	14	7
UB14	16	8	UC19	16	8	UD26	14	7	UE30	14	7
UB15	16	8	UC20	16	8	UD27	14	7	UE31	14	7
UB16	16	8	UC21	16	8	UD28	14	7	UE32	14	7
UB17	16	8	UC22	16	8	UD29	14	7	UE33	14	7
UB18	16	8	UC23	16	8	UD30	14	7	UE34	14	7
UB19	16	8	UC24	16	8	UD31	14	7	UF3	16	8
UB20	16	8	UC25	16	8	UD32	14	7	UF4	16	8
UB21	16	8	UC26	16	8	UD33	14	7	UF5	16	8
UB22	16	8	UC27	16	8	UD34	14	7	UF6	16	8
UB23	16	8	UC28	16	8	UE2	14	7	UF7	16	8
UB24	16	8	UC29	16	8	UE3	14	7	UF8	16	8
UB25	16	8	UC30	16	8	UE4	14	7	UF9	16	8
UB26	16	8	UC31	16	8	UE5	14	7	UF10	16	8

POWER PINS			POWER PINS			POWER PINS			POWER PINS		
REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND
UF11	16	8	UG21	16	8	UH32	14	7	UA25	16	8
UF12	16	8	UG22	16	8	UH33	14	7	UA26	16	8
UF13	16	8	UG23	16	8	UH34	14	7	UB1	14	7
UF14	16	8	UG24	16	8	UJ4	14	7	UC1	16	8
UF16	16	8	UG25	16	8	UJ5	14	7	UD1	14	7
UF17	16	8	UG26	16	8	UJ6	14	7	UD20	14	7
UF18	16	8	UG27	16	8	UJ7	14	7	UD21	14	7
UF19	16	8	UG28	16	8	UJ8	14	7	UD22	14	7
UF20	16	8	UG29	16	8	UJ9	14	7	UE1	14	7
UF21	16	8	UG30	16	8	UJ10	14	7	UF1	14	7
UF22	16	8	UG31	16	8	UJ11	14	7	UG1	16	8
UF23	16	8	UG32	16	8	UJ12	14	7	UH1	14	7
UF24	16	8	UG33	16	8	UJ13	14	7	UH2	14	7
UF25	16	8	UG34	16	8	UJ14	14	7	UJ1	14	7
UF26	16	8	UH3	14	7	UJ15	14	7	UJ2	14	7
UF27	16	8	UH4	14	7	UJ16	14	7	UJ21	14	7
UF28	16	8	UH5	14	7	UJ17	14	7	UJ22	14	7
UF29	16	8	UH6	14	7	UJ18	14	7	UJ23	14	7
UF30	16	8	UH7	14	7	UJ19	14	7			
UF31	16	8	UH8	14	7	UJ25	14	7			
UF32	16	8	UH9	14	7	UJ26	14	7			
UF33	16	8	UH10	14	7	UJ27	14	7			
UF34	16	8	UH11	14	7	UJ28	14	7			
UG3	16	8	UH12	14	7	UJ29	14	7			
UG4	16	8	UH13	14	7	UJ30	14	7			
UG5	16	8	UH14	14	7	UJ31	14	7			
UG6	16	8	UH15	14	7	UJ32	14	7			
UG11	16	8	UH16	14	7	UJ33	14	7			
UG12	16	3	UH17	14	7	UJ34	14	7			
UG13	16	8	UH18	14	7						
UG14	16	8	UH25	14	7	UG2	16	8			
UG15	16	8	UH26	14	7						
UG16	16	8	UH27	14	7						
UG17	16	8	UH28	14	7	UF15	16	8			
UG18	16	8	UH29	14	7	UJ3	14	7			
UG19	16	8	UH30	14	7	UJ20	14	7			
UG20	16	8	UH31	14	7						

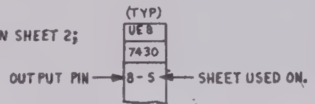
REVISIONS			
A	UPDATE FOR Ø3 SN2,5,13,15,17,19,20 [illegible]	[illegible]	9-30-77
B	ECO [illegible]	E P PT SN131	[illegible]-26-77
C	ECO55700 RN UD34 & UE34 SHT2 [illegible]	[illegible]	[illegible]-77
D	ECO55719 ADDED UG[illegible]	[illegible]	11-19-77
E	ECO 55739 ADD C3 [illegible]	[illegible]	[illegible]-77
F	ECO 55756 ADD 267 SHT 2 [illegible]	[illegible]	[illegible]
G	ECO 55801, [illegible] ADDED [illegible]	[illegible]	[illegible]
H	ECO 55777 DELETED [illegible] SHT 1 & 2	[illegible]	[illegible]
J	ECO56030 REV UD18 UNUS ADD UGE [illegible]	[illegible]	2-24-78
K	ECO [illegible] DELETED UF1 FROM UNUSED CIR. [illegible] ADDED [illegible] TO UF1 TABLE SHT 2 ADDED UF1 TO SCHEM SHT 17	E P PT	6-15-78
L	ECO 56[illegible]	[illegible]	7-19-78
M	ECO 57670 ADD P2P30 & 31, SHT 7, [illegible]	[illegible]	[illegible]-12-78



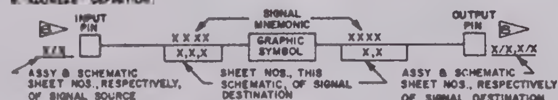
8 SEE SHT. 29

7 THIS DWG IS COMPLETE WITH SHEETS 1 THRU 29 & 34 & 38.

6 ON SHEET 2;



5. ADDRESS DEFINITION:



4. CHARACTERS IN PARENTHESES NEAR REFERENCE DESIGNATORS IDENTIFY THE SECTION OF THE ASSEMBLY WHERE THE PART IS LOCATED.

3. CIRCUIT RETURN SYMBOLS: —▷A ANALOG GND, —▷D DIGITAL GND.

2. FOR TOLERANCES AND RATINGS. SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS.

UNLESS OTHERWISE SPECIFIED:

NOTES:

10 SEE SHT 29

9. J1 THRU J4 ARE WIRED PIN TO PIN (VIA CABLES TO FRONT PANEL DISPLAY PWA'S. J1 TO J2 & J2 TO J1 ON TOP DISPLAY, SCHEMATIC NO. 28704 & J3 TO J2 & J4 TO J1 ON BOTTOM DISPLAY, SCHEMATIC NO. 28749.

FUNCTION #8

BSC	34595	710-02

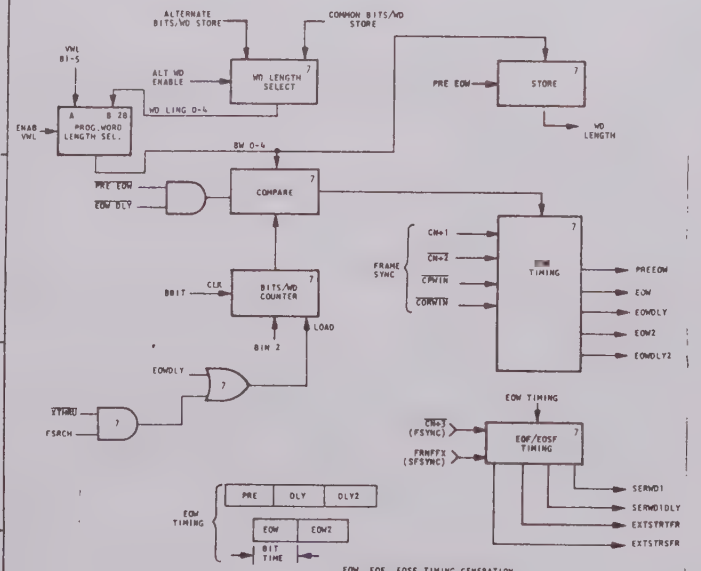
PARTS LIST

C. FASO 6-23-77

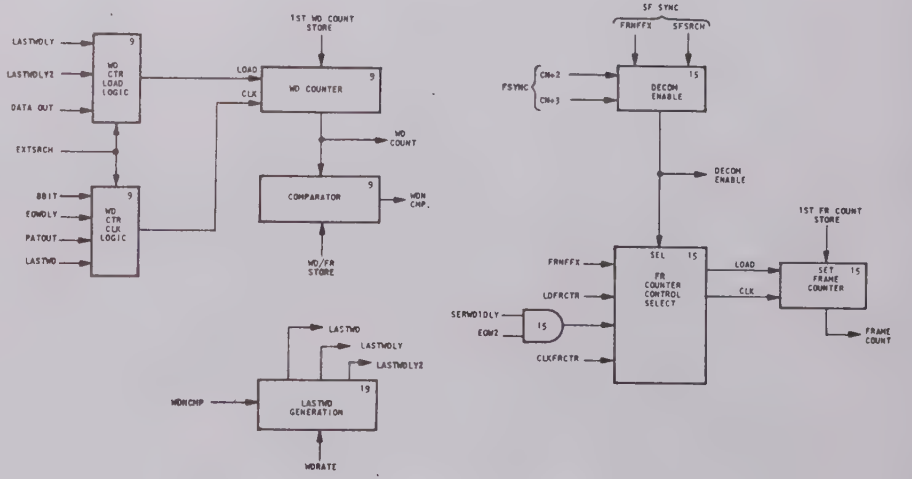
Schlumberger

SCHEM, PWA, WORD SELECT & DISPLAY

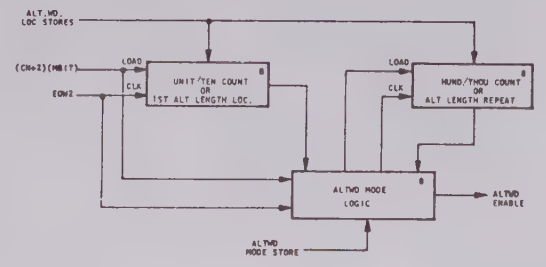
D 06141 34597



EOW, EOF, EOSF TIMING GENERATION

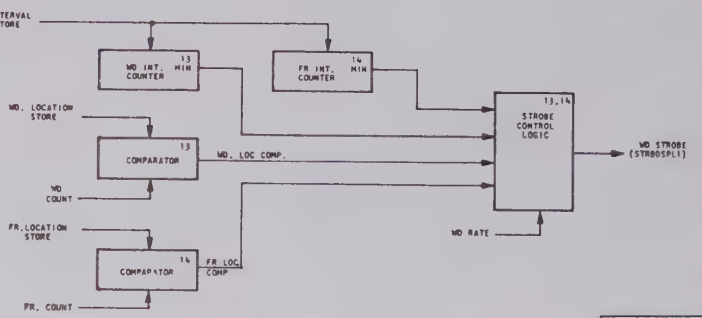


WD/FRAME AND FRAME/SFRAME COUNTERS



ALTERNATE WD LENGTH CONTROL

NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.



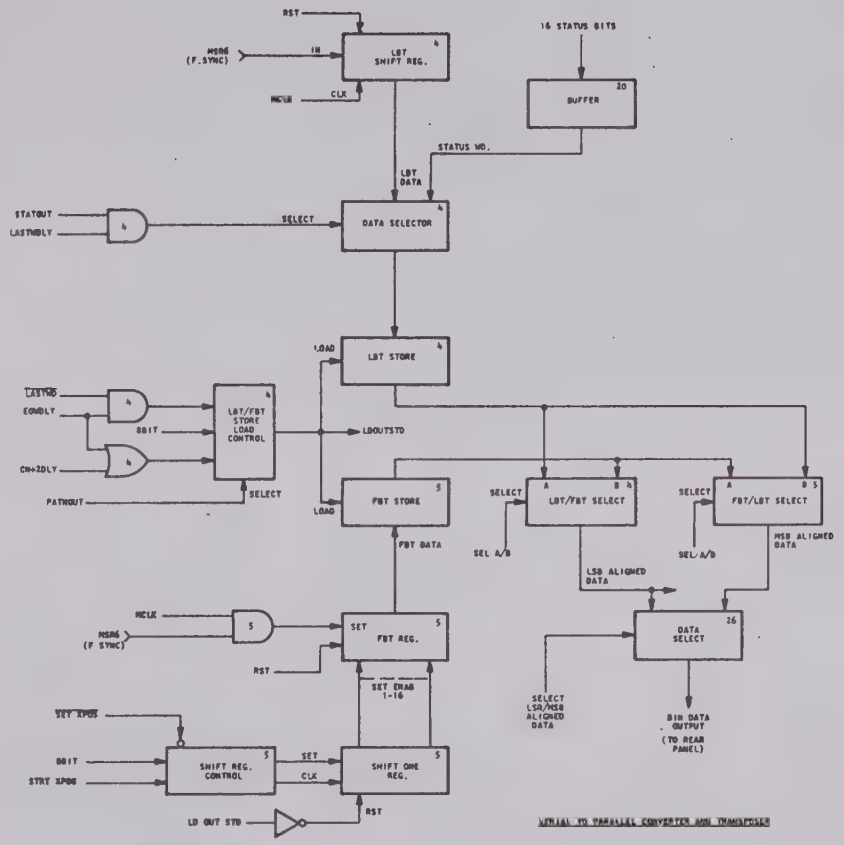
DISPLAY STROBE GENERATION

Schlumberger

SCHEMATIC, PU1A
WORD SELECT & DISPLAY

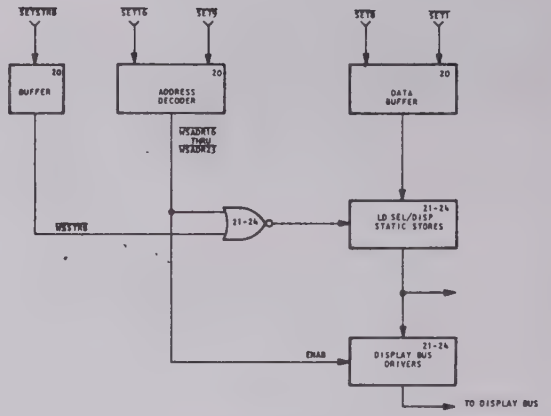
SIZE	CODE IDENT NO	DRAWING NO	REV
D	06141	34597	

SCALE — SHEET 7 OF



SERIAL TO PARALLEL CONVERTER AND TRANSMITTER

NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.



ADDRESS DECODE AND STATIC STORES

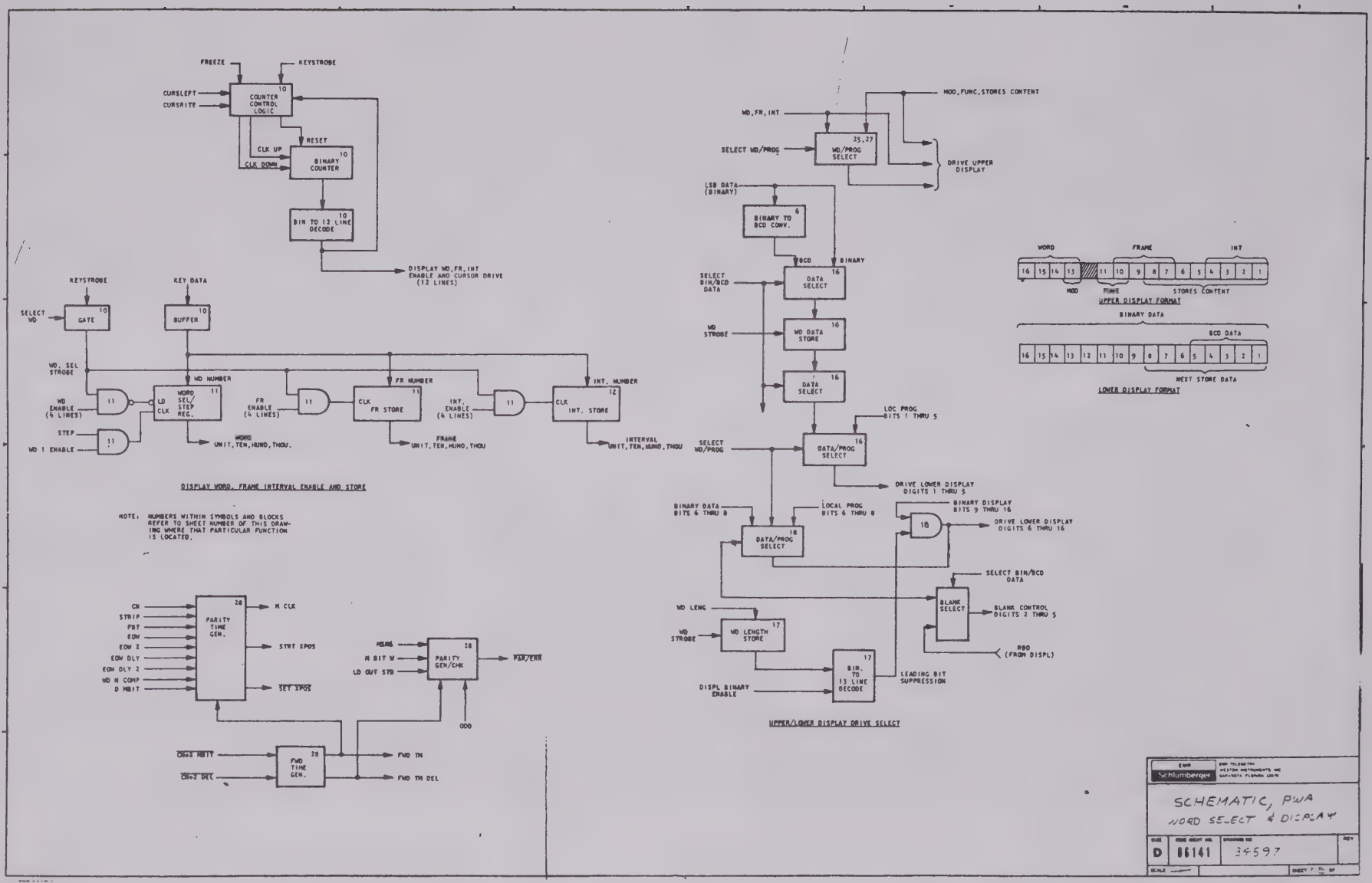
Schlumberger

SCHEMATIC, PWA
WORD SELECT & DISPLAY

SIZE	WEC ASSY NO.	DRAWING NO.	REV
D	88141	34597	

SCALE — SHEET 3 OF

SCHEM, PWA,
WORD SELECT & DISPLAY
SERIAL TO PARALLEL CONVERTER & LSB ALIGNED OUTPUT MUX

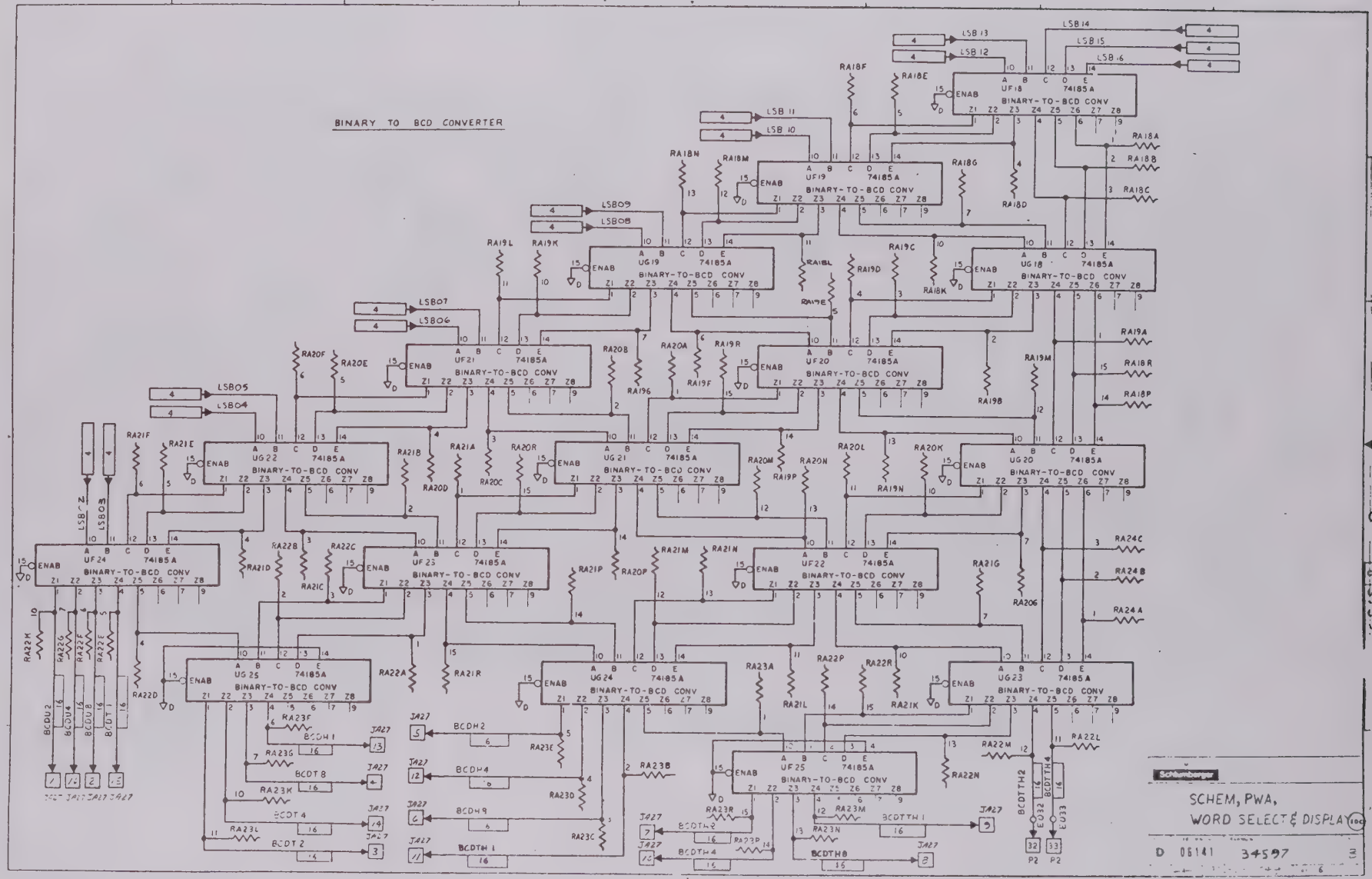


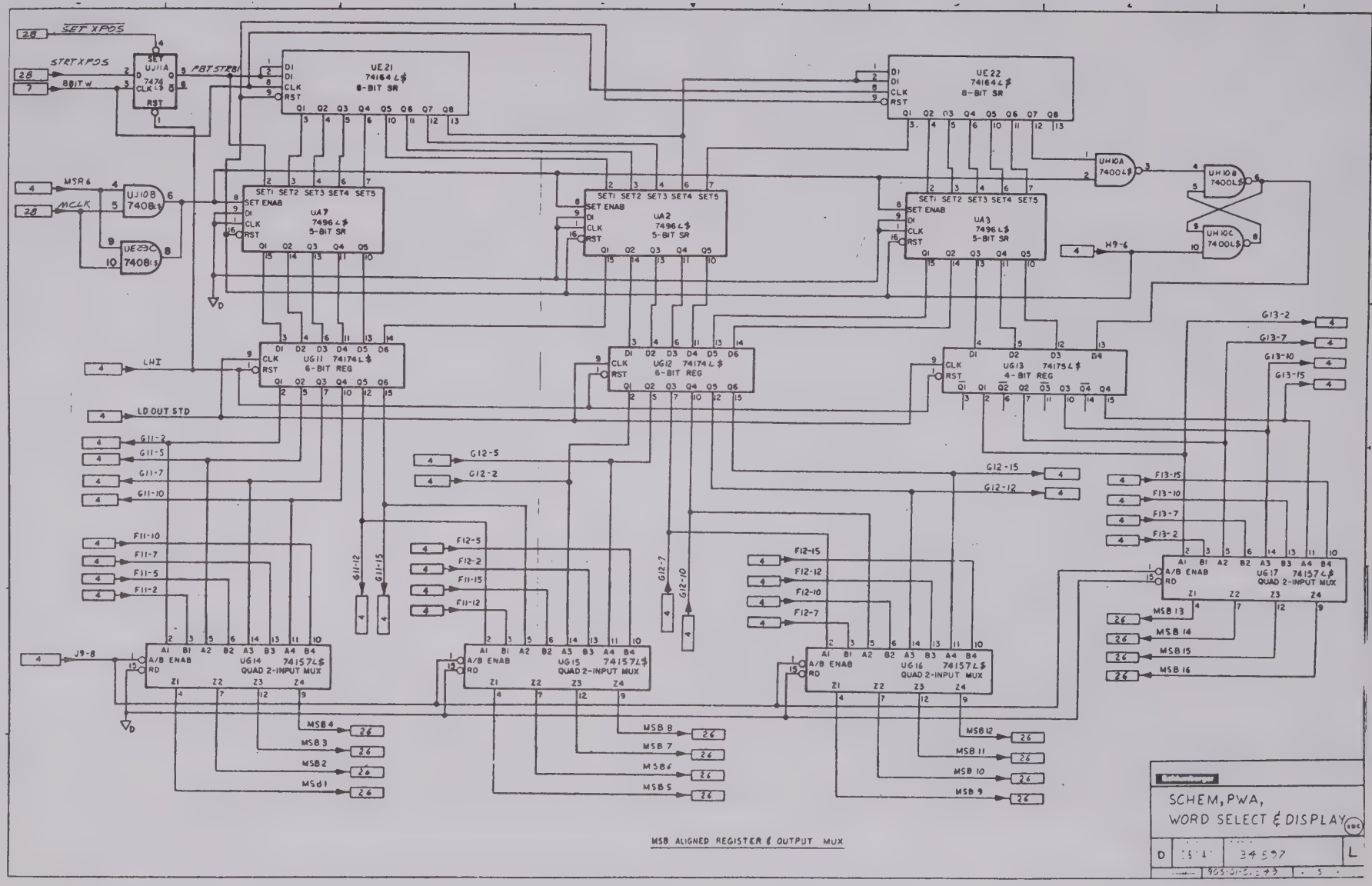
Schlumberger

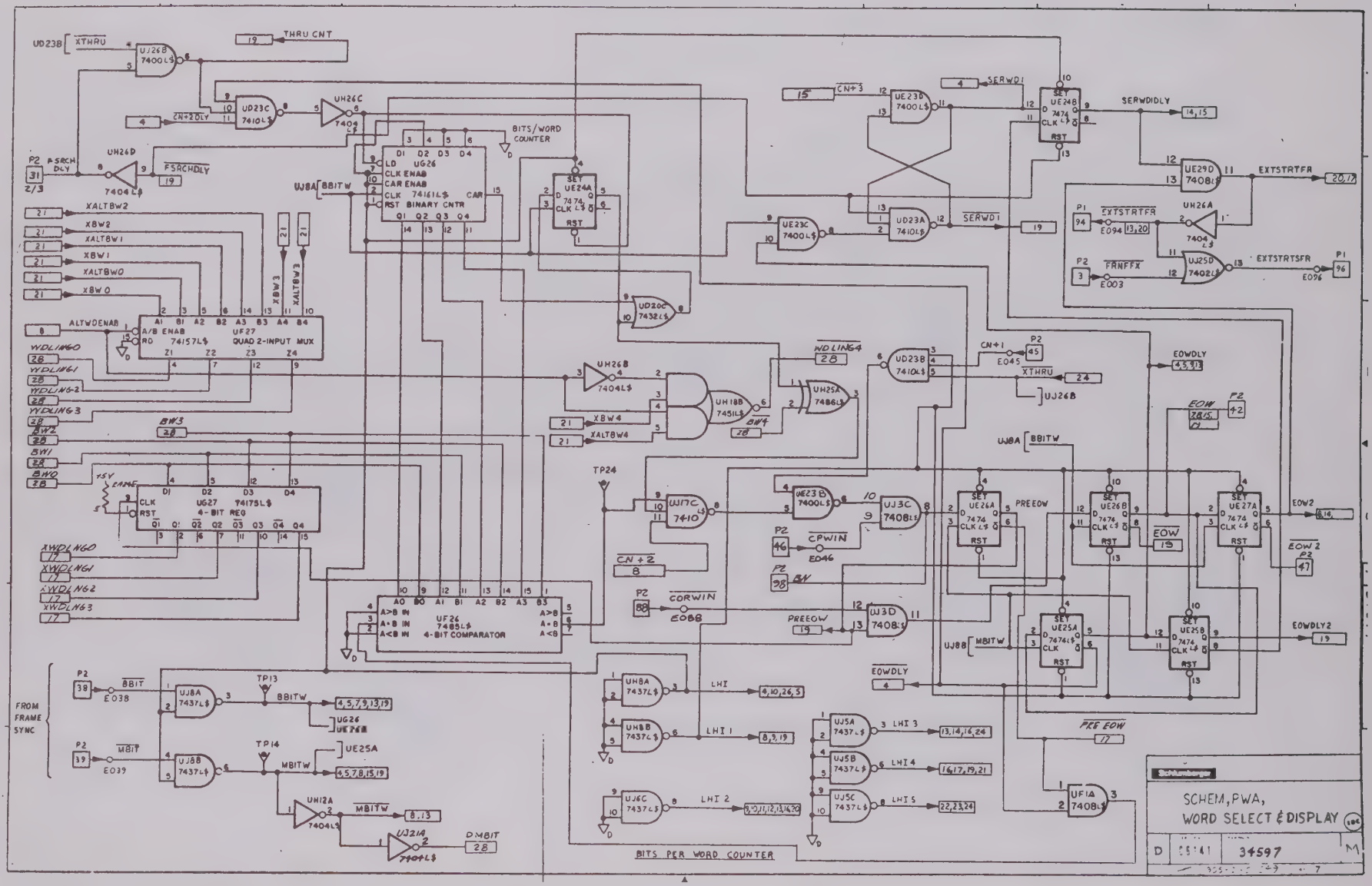
SCHEMATIC, PWA
WORD SELECT & DISPLAY

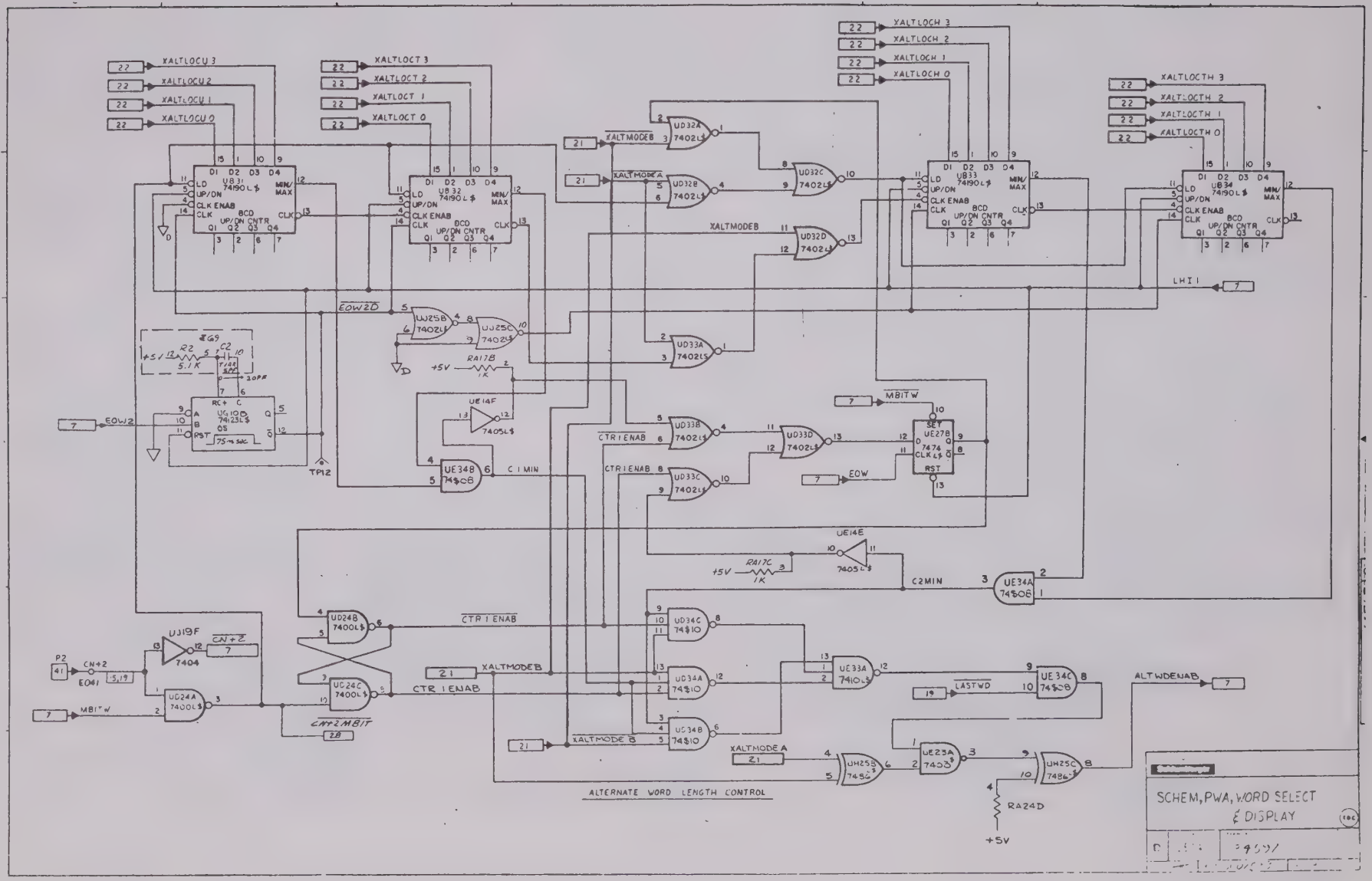
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	86141	34597	

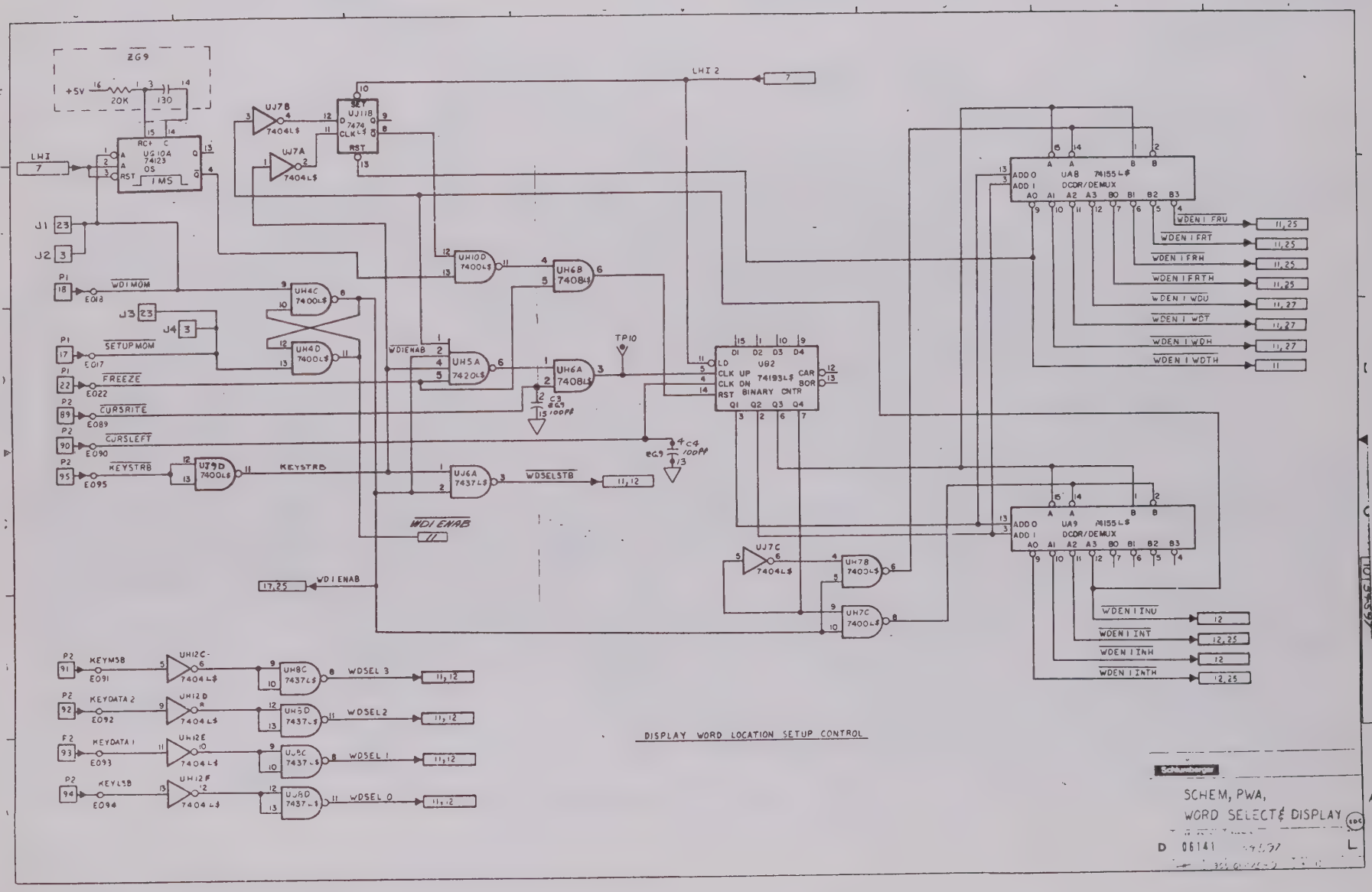
SCALE — SHEET 7 OF


BINARY TO BCD CONVERTER
LSB 16
LSB 15
LSB 14
LSB 13
LSB 12
LSB 11
LSB 10
LSB 09
LSB 08
LSB 07
LSB 06
LSB 05
LSB 04
LSB 03
LSB 02
UF18 74185A BINARY-TO-BCD CONV
UF19 74185A BINARY-TO-BCD CONV
UG18 74185A BINARY-TO-BCD CONV
UG19 74185A BINARY-TO-BCD CONV
UF20 74185A BINARY-TO-BCD CONV
UG20 74185A BINARY-TO-BCD CONV
UF21 74185A BINARY-TO-BCD CONV
UG21 74185A BINARY-TO-BCD CONV
UF22 74185A BINARY-TO-BCD CONV
UG22 74185A BINARY-TO-BCD CONV
UF23 74185A BINARY-TO-BCD CONV
UG23 74185A BINARY-TO-BCD CONV
UF24 74185A BINARY-TO-BCD CONV
UG24 74185A BINARY-TO-BCD CONV
UF25 74185A BINARY-TO-BCD CONV
UG25 74185A BINARY-TO-BCD CONV
ENAB
BCDU2
BCDU4
BCDU8
BCDT1
BCDH2
BCDH4
BCDH8
BCDH1
BCDT8
BCDT4
BCDT2
BCDTH2
BCDTH4
BCDTH8
BCDTH1
SCHEM, PWA,
WORD SELECT & DISPLAY
D 06141 34597


SET XPOS
STRT XPOS
BBIT W
MBT STRB
UE21 74164 L$ 8-BIT SR
UE22 74164 L$ 8-BIT SR
UA7 7496 L$ 5-BIT SR
UA2 7496 L$ 5-BIT SR
UA3 7496 L$ 5-BIT SR
MSR 6
MCLK
LHI
LD OUT STD
UG11 74174 L$ 6-BIT REG
UG12 74174 L$ 6-BIT REG
UG13 74175 L$ 4-BIT REG
G11-2
G11-5
G11-7
G11-10
G12-5
G12-2
G12-15
G12-12
G13-2
G13-7
G13-10
G13-15
F13-15
F13-10
F13-7
F13-2
F11-10
F11-7
F11-5
F11-2
F12-5
F12-2
F11-15
F11-12
F12-15
F12-12
F12-10
F12-7
J9-8
UG14 74157L$ QUAD 2-INPUT MUX
UG15 74157L$ QUAD 2-INPUT MUX
UG16 74157L$ QUAD 2-INPUT MUX
UG17 74157L$ QUAD 2-INPUT MUX
MSB 4
MSB 3
MSB 2
MSB 1
MSB 8
MSB 7
MSB 6
MSB 5
MSB 12
MSB 11
MSB 10
MSB 9
MSB 13
MSB 14
MSB 15
MSB 16
MSB ALIGNED REGISTER & OUTPUT MUX
SCHEM, PWA, WORD SELECT & DISPLAY
D
34597
L


SCHEM, PWA,
WORD SELECT & DISPLAY
34597
BITS PER WORD COUNTER
BITS/WORD COUNTER
THRU CNT
UF26 7485L$ 4-BIT COMPARATOR
UG27 74175L$ 4-BIT REG
UF27 QUAD 2-INPUT MUX
UG26 74161L$ CAR BINARY CNTR
UF1A 7408L$
UE24A 7474 CLK L$ RST
UE24B 7474 CLK L$ RST
UE25A 7474L$ CLK RST
UE25B 7474L$ CLK RST
UE26A 7474 CLK L$ RST
UE26B 7474 CLK L$ RST
UE27A 7474 CLK L$ RST
UE29D 7408L$
UJ25D 7402L$
UH26A 7404 L$
UJ21A 7404L$
UH12A 7404L$
UJ8A 7437L$
UJ8B 7437L$
UJ5A 7437L$
UJ5B 7437L$
UJ5C 7437L$
UH8A 7437L$
UH8B 7437L$
UJ6C 7437L$
UJ3C 7408L$
UJ3D 7408L$
UH18B 7451L$
UH25A 7486L$
UD20C 7432L$
UJ7C 7410
UD23A 7410L$
UD23B 7410L$
UD23C 7410L$
UE23B 7400L$
UE23C 7400L$
UE23D 7400L$
UJ26B 7400L$
UD23B 7400L$
UH26B 7404L$
UH26C 7404 L$
UH26D 7404 L$
UJ8A 7437L$
UJ8B 7437L$
UJ5A 7437L$
UJ5B 7437L$
UJ5C 7437L$
UH8A 7437L$
UH8B 7437L$
UJ6C 7437L$
UJ3C 7408L$
UJ3D 7408L$
UH18B 7451L$
UH25A 7486L$
UD20C 7432L$
UJ7C 7410
UD23A 7410L$
UD23B 7410L$
UD23C 7410L$
UE23B 7400L$
UE23C 7400L$
UE23D 7400L$
UJ26B 7400L$
UD23B 7400L$
UH26B 7404L$
UH26C 7404 L$
UH26D 7404 L$
XTHRU
SERWD1
SERWDLY
EXTSTRTFR
FANFFX
FSRCHDLY
ALTWDENAB
XALTBW2
XBW2
XALTBW1
XBW1
XALTBW0
XBW0
XBW4
XALTBW4
WDLING0
WDLING1
WDLING-2
WDLING-3
WDLING4
BW3
BW2
BW1
BW0
BW4
XWDLNG0
XWDLNG1
XWDLNG2
XWDLNG3
CNAME
TSV
CN+2DLY
CN+3
CN+1
CN+2
BBITW
MBITW
DMBIT
CPWIN
CORWIN
PREEOW
EOW
EOW2
EOWDLY
EOWDLY2
PRE EOW
LHI
LHI 1
LHI 2
LHI 3
LHI 4
LHI 5
TP13
TP14
TP24
FROM FRAME SYNC
EO38
EO39
EO45
EO46
EO88
EO94
EO96
EO03
UJ26B
UJ8A
UJ8B
UE25A
UG26
PREEOW
EOW
EOW2
EOWDLY
EOWDLY2
PRE EOW
SCHEM, PWA, WORD SELECT & DISPLAY
D
34597


XALTLOCU 3
XALTLOCU 2
XALTLOCU 1
XALTLOCU 0
XALTLOCT 3
XALTLOCT 2
XALTLOCT 1
XALTLOCT 0
XALTLOCH 3
XALTLOCH 2
XALTLOCH 1
XALTLOCH 0
XALTLOCTH 3
XALTLOCTH 2
XALTLOCTH 1
XALTLOCTH 0
XALTMODEB
XALTMODEA
XALTMODEB
LHI 1
EOW2D
EOW2
TP12
C1MIN
CTR1ENAB
MBITW
EOW
C2MIN
LASTWD
ALTWDENAB
CNT2MBIT
+5V
ALTERNATE WORD LENGTH CONTROL
SCHEM, PWA, WORD SELECT & DISPLAY



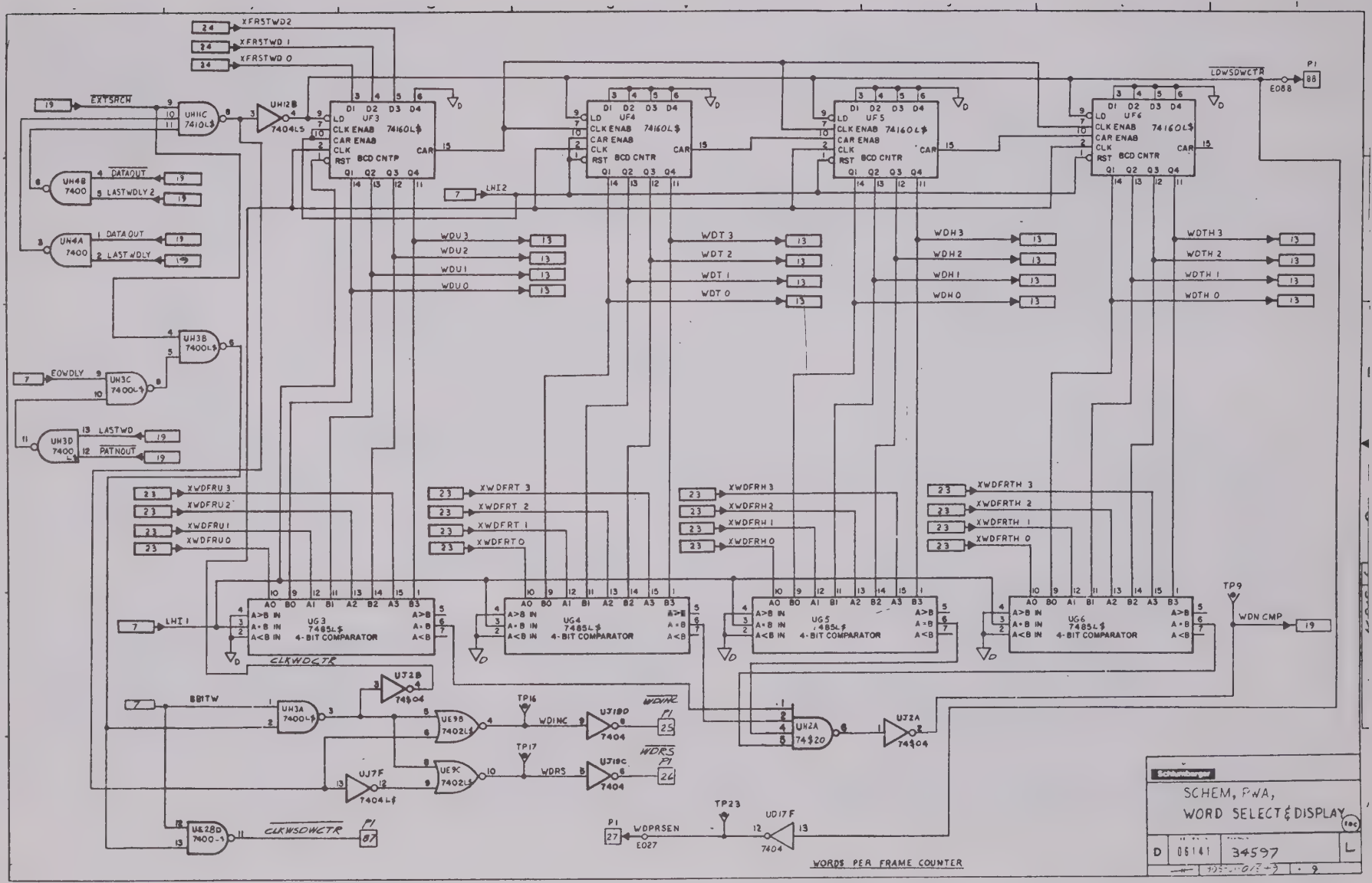
DISPLAY WORD LOCATION SETUP CONTROL

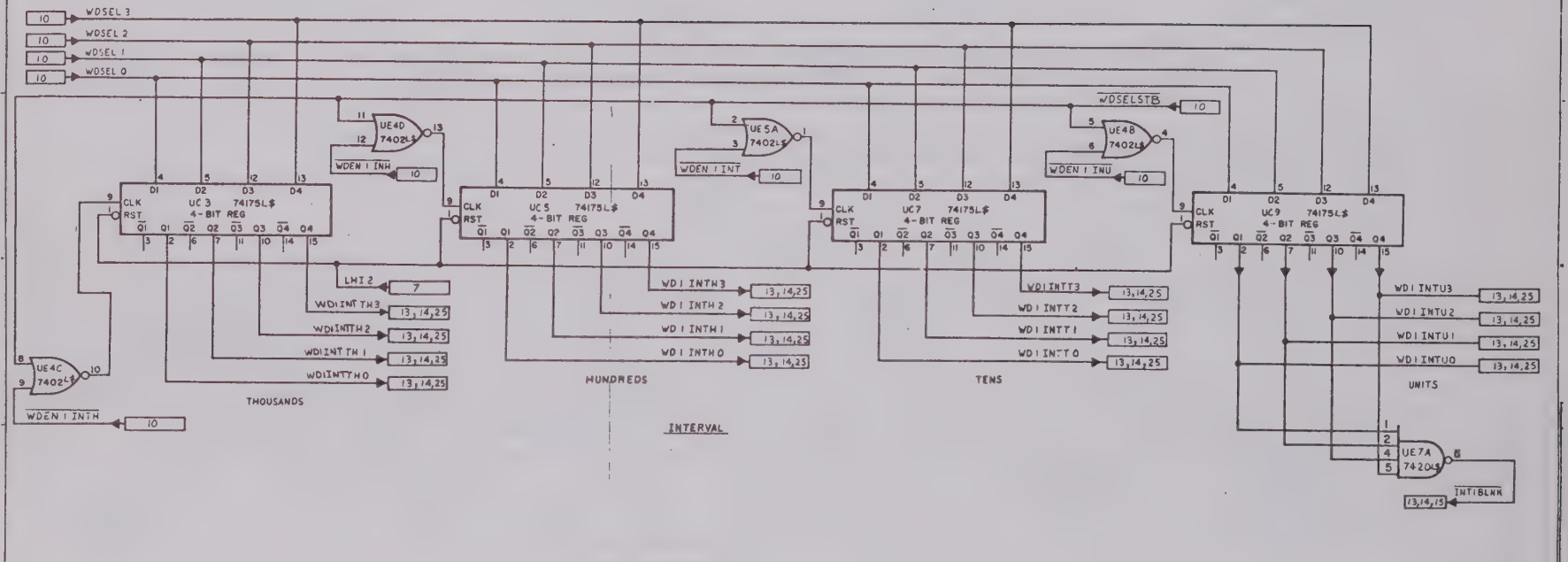
Schlumberger

SCHEM, PWA,
WORD SELECT & DISPLAY

D 06141 L

4-49

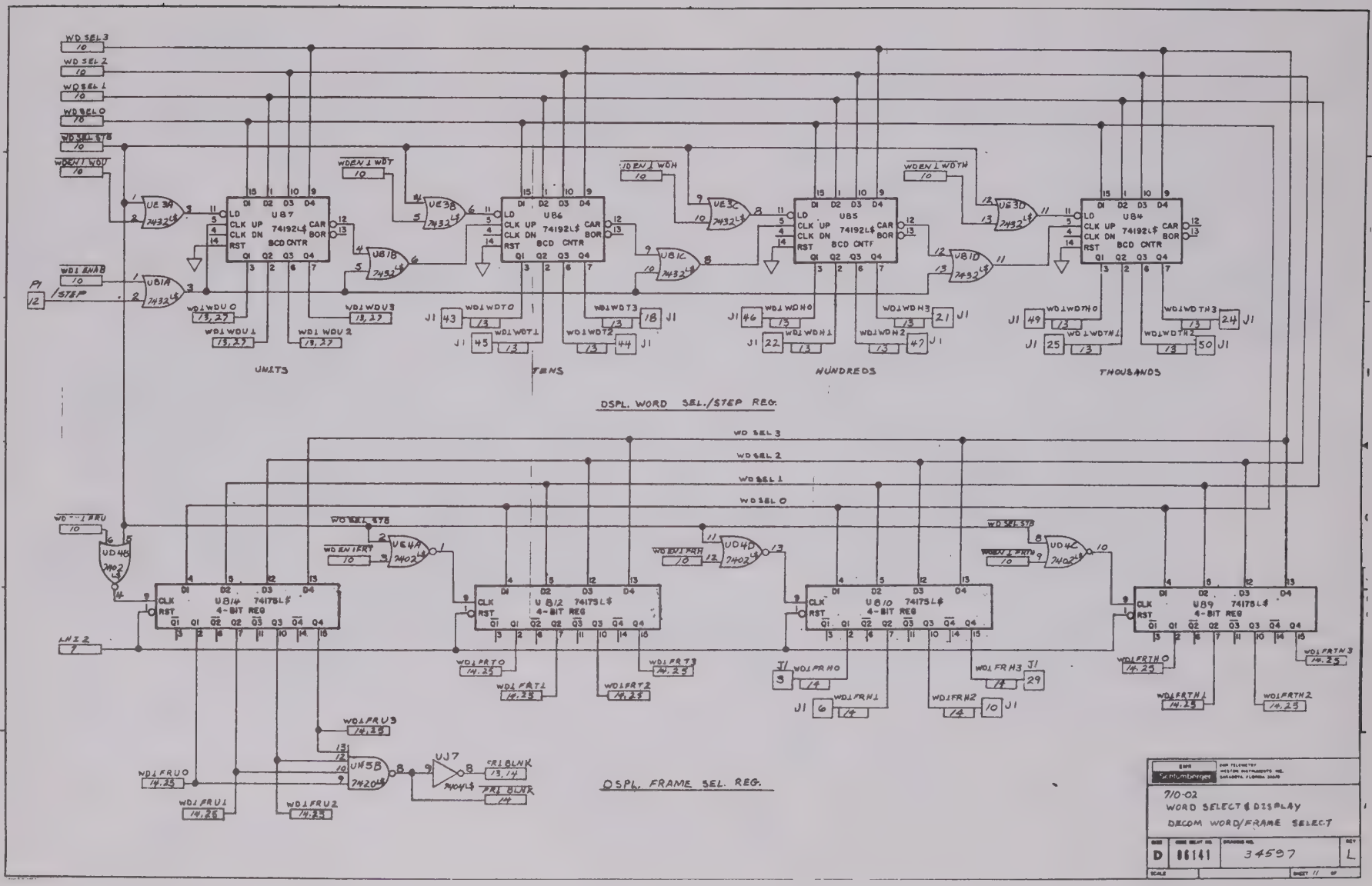

XFRSTWD2
XFRSTWD 1
XFRSTWD 0
LDWSDWCTR
P1
E088
EXTSRCH
UH11C 7410L$
UH12B 7404L$
UF3
UF4
UF5
UF6
74160L$
CLK ENAB
CAR ENAB
CLK
RST
BCD CNTR
CAR
Q1 Q2 Q3 Q4
LHI2
UH4B 7400
DATAOUT
LASTWDLY 2
UH4A 7400
DATA OUT
LAST WDLY
WDU3
WDU2
WDU1
WDU0
WDT 3
WDT 2
WDT 1
WDT 0
WDH3
WDH2
WDH1
WDH0
WDTH3
WDTH2
WDTH1
WDTH0
UH3B 7400L$
EOWDLY
UH3C 7400L$
UH3D 7400L$
LASTWD
PATNOUT
XWDFRU3
XWDFRU2
XWDFRU1
XWDFRU0
XWDFRT 3
XWDFRT 2
XWDFRT 1
XWDFRTO
XWDFRH3
XWDFRH2
XWDFRH1
XWDFRH0
XWDFRTH 3
XWDFRTH 2
XWDFRTH 1
XWDFRTH 0
TP9
WDN CMP
LHI 1
UG3 7485L$ 4-BIT COMPARATOR
UG4 7485L$ 4-BIT COMPARATOR
UG5 7485L$ 4-BIT COMPARATOR
UG6 7485L$ 4-BIT COMPARATOR
A>B IN
A=B IN
A<B IN
A>B
A=B
A<B
CLKWDCTR
UJ2B 74$04
BBITW
UH3A 7400-S
UE9B 7402L$
UE9C 7402L$
UJ7F 7404L$
TP16
TP17
WDINC
WDRS
UJ10D 7404
UJ10C 7404
UH2A 74$20
UJ2A 74$04
UE28D 7400-S
CLKWSDWCTR
TP23
UD17F 7404
WDPRSEN
E027
WORDS PER FRAME COUNTER
SCHEM, PWA,
WORD SELECT & DISPLAY
D
06141
34597
L

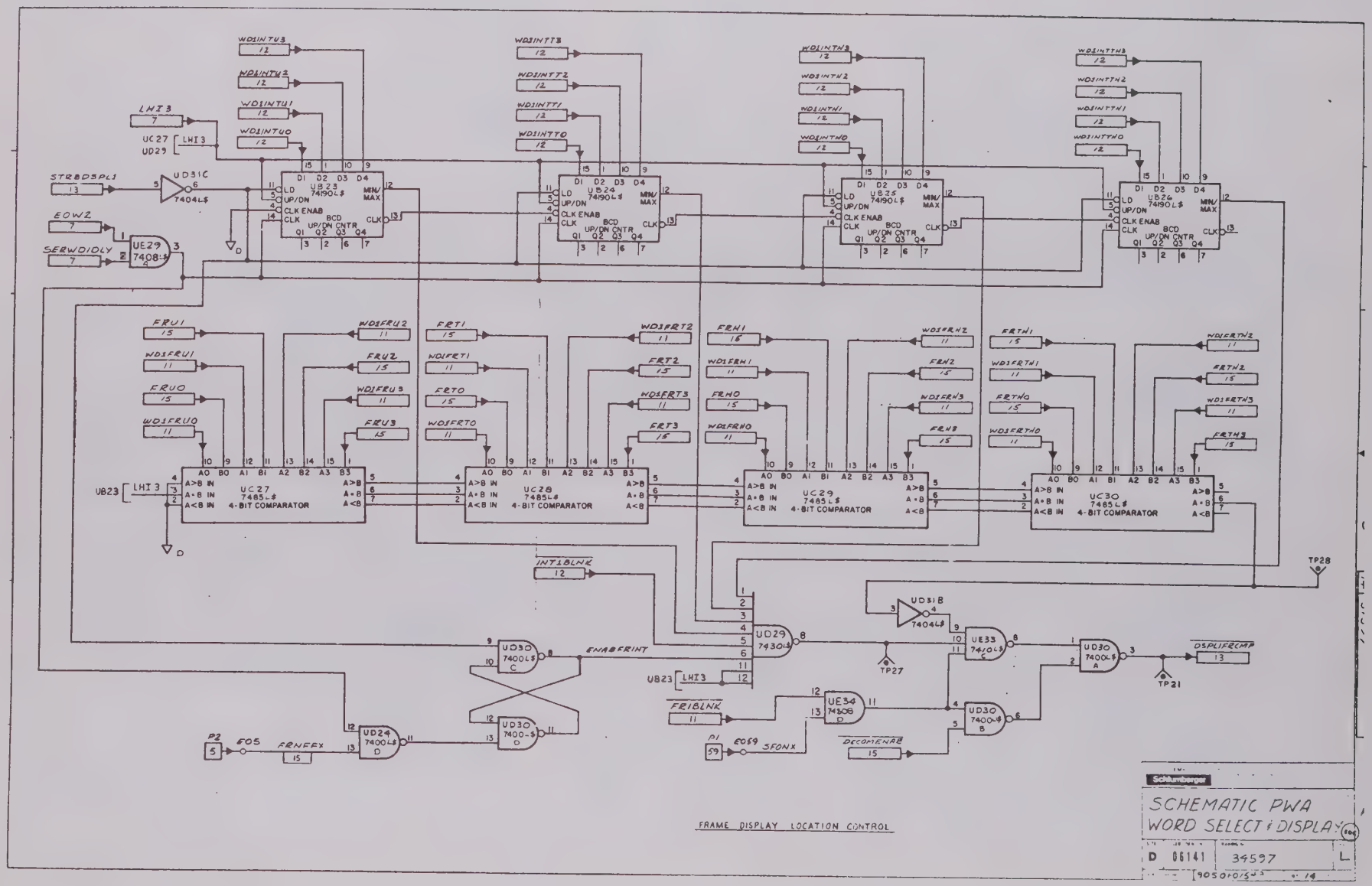


Schlumberger

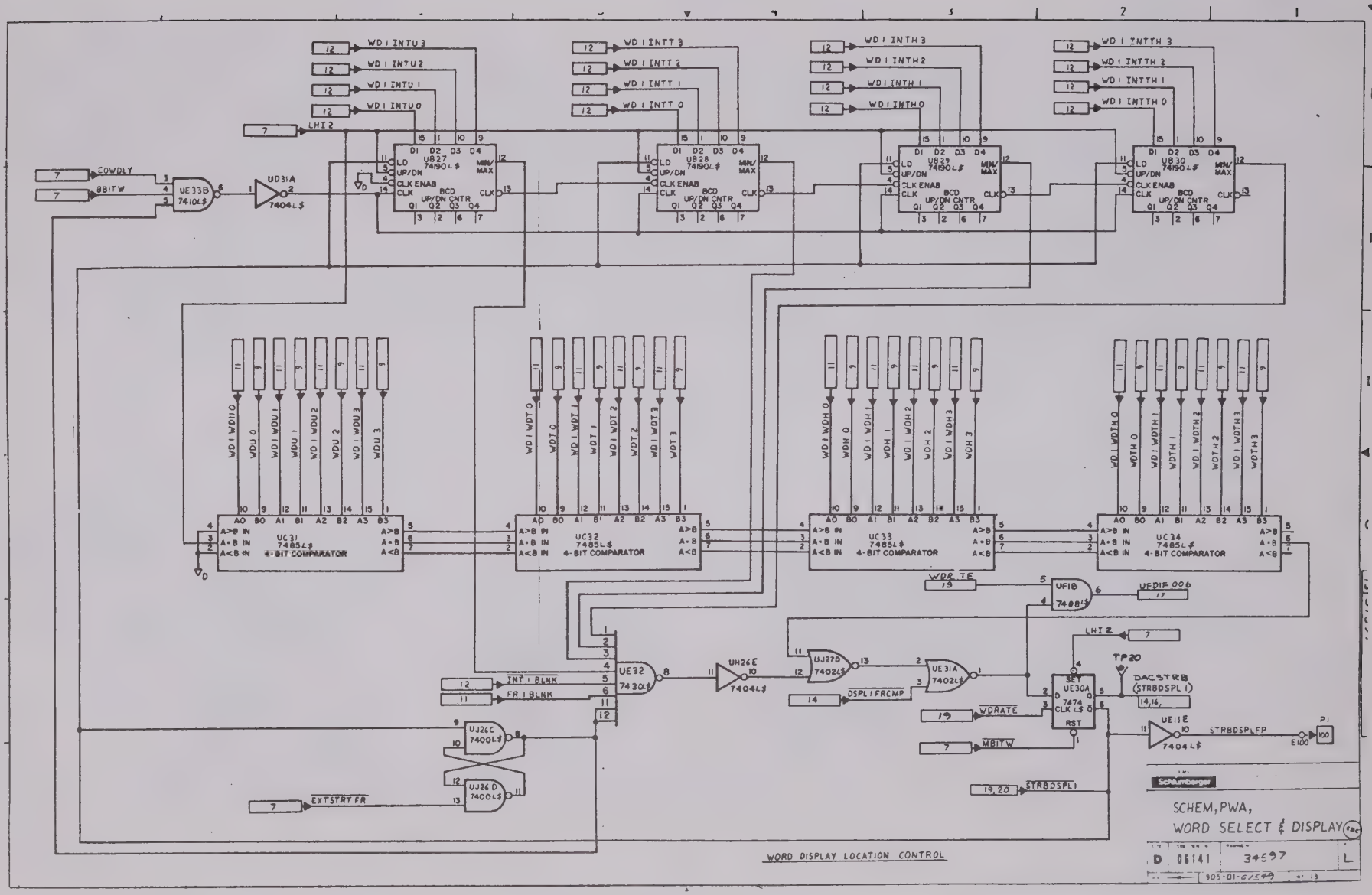
SCHEM, PWA,
WORD SELECT & DISPLAY

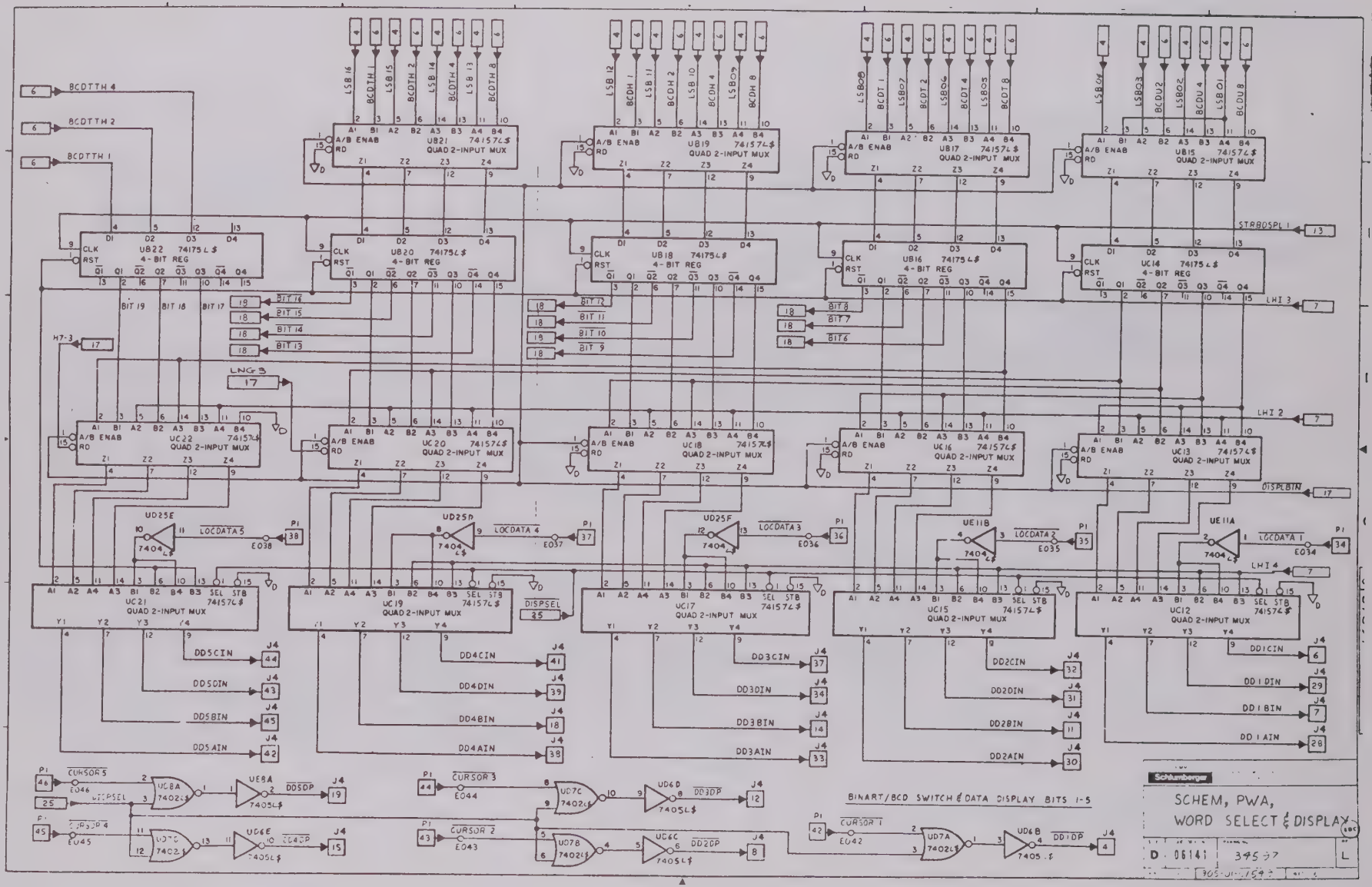
D 06141 34597 L

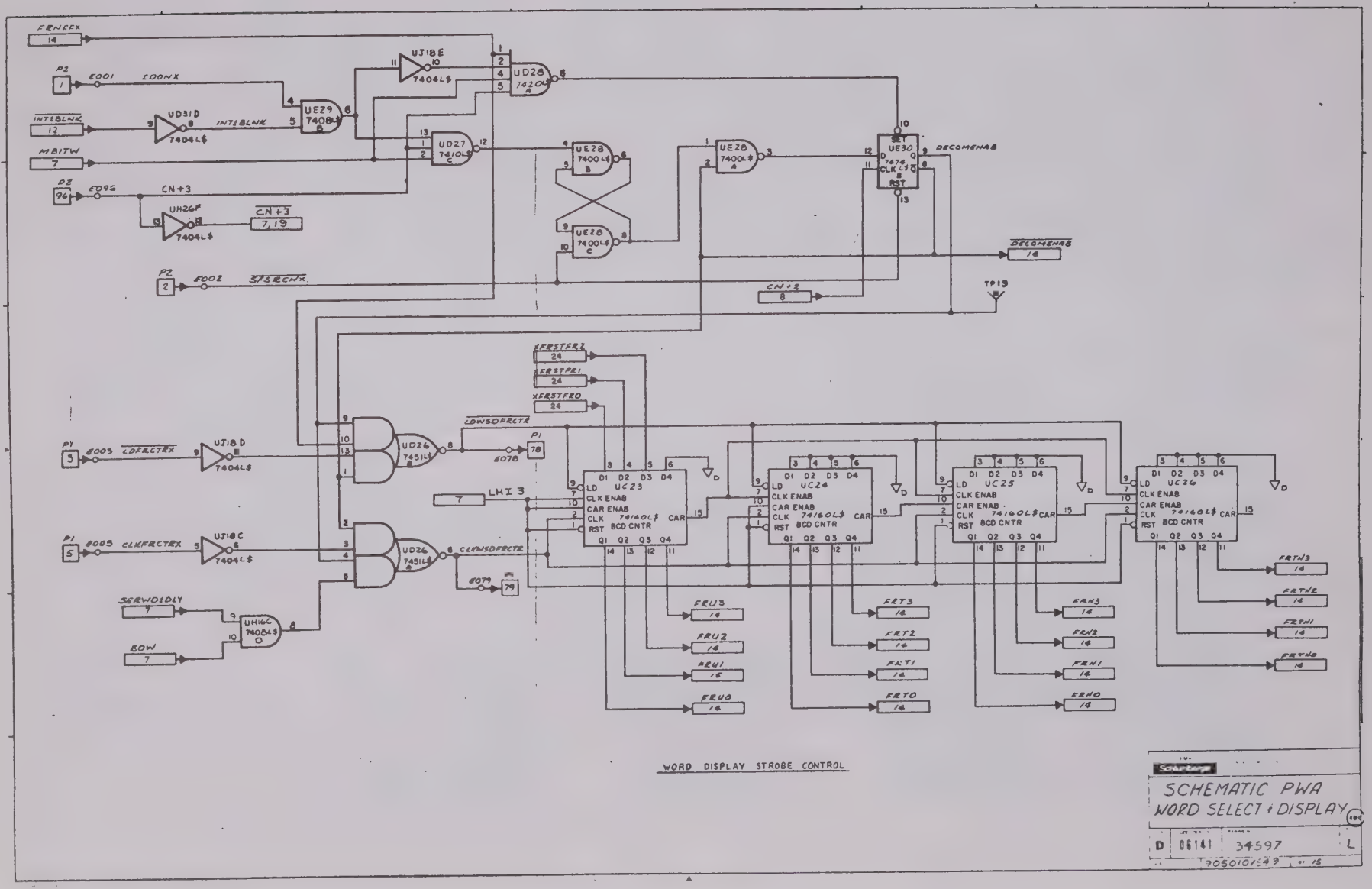

WD SEL 3
WD SEL 2
WD SEL 1
WD SEL 0
WD SEL STB
WDEN 1 WDU
WDEN 1 WDT
WDEN 1 WDH
WDEN 1 WDTH
WD ENAB
STEP
U87
U86
U85
U84
74192L$
BCD CNTR
UNITS
TENS
HUNDREDS
THOUSANDS
DSPL. WORD SEL./STEP REG.
WDEN 1 FRU
WDEN 1 FRT
WDEN 1 FRH
WDEN 1 FRTH
LWI 2
U814
U812
U810
U89
74175L$
4-BIT REG
DSPL. FRAME SEL. REG.
7/10-02
WORD SELECT & DISPLAY
DECOM WORD/FRAME SELECT
D
86141
34597
L



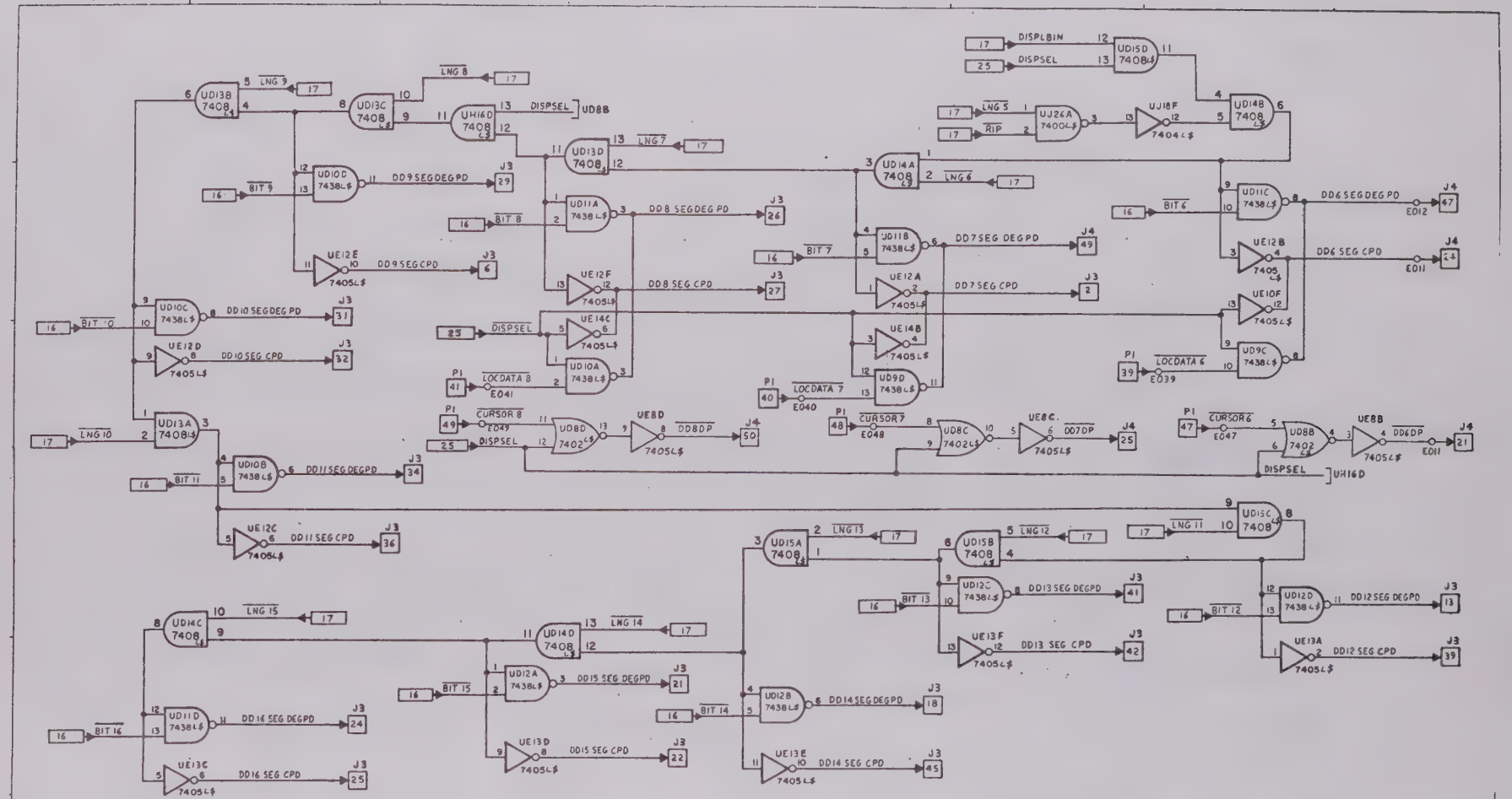
UB23 74190L$
UB24 74190L$
UB25 74190L$
UB26 74190L$
UC27 7485L$ 4-BIT COMPARATOR
UC28 7485L$ 4-BIT COMPARATOR
UC29 7485L$ 4-BIT COMPARATOR
UC30 7485L$ 4-BIT COMPARATOR
UD29 7430L$
UD30 7400L$
UD31C 7404L$
UD31B 7404L$
UE29 7408L$
UE33 7410L$
UE34 74308
UD24 7400L$
STRBDSPL1
EOW2
SERWDIDLY
LHI3
INT1BLNK
ENABFRINT
FRIBLNK
DECOMENAB
DSPLIFRCMP
FRNFFX
SFONX
TP27
TP28
TP21
FRAME DISPLAY LOCATION CONTROL
SCHEMATIC PWA
WORD SELECT & DISPLAY
D 06141 34597 L

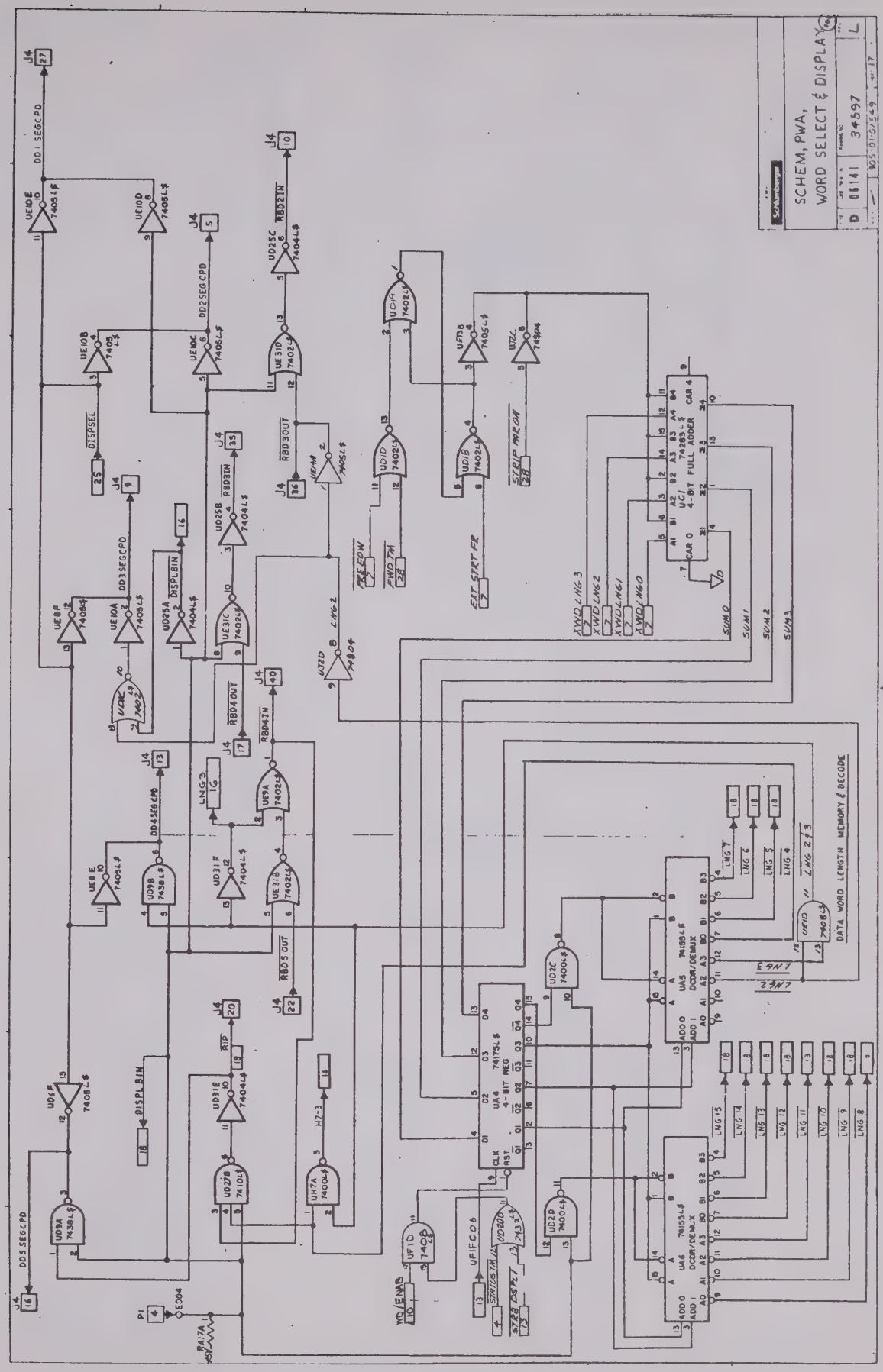

WD I INTU 3
WD I INTU 2
WD I INTU 1
WD I INTU 0
WD I INTT 3
WD I INTT 2
WD I INTT 1
WD I INTT 0
WD I INTH 3
WD I INTH 2
WD I INTH 1
WD I INTH 0
WD I INTTH 3
WD I INTTH 2
WD I INTTH 1
WD I INTTH 0
LHI 2
COWDLY
8BITW
UE33B 74104$
UD31A 7404L$
UB27 74190L$ MIN/MAX BCD UP/DN CNTR
UB28 74190L$ MIN/MAX BCD UP/DN CNTR
UB29 74190L$ MIN/MAX BCD UP/DN CNTR
UB30 74190L$ MIN/MAX BCD UP/DN CNTR
WD I WDU 0
WD I WDU 1
WD I WDU 2
WD I WDU 3
WD I WDT 0
WD I WDT 1
WD I WDT 2
WD I WDT 3
WD I WDH 0
WD I WDH 1
WD I WDH 2
WD I WDH 3
WD I WDTH 0
WD I WDTH 1
WD I WDTH 2
WD I WDTH 3
UC31 7485L$ 4-BIT COMPARATOR
UC32 7485L$ 4-BIT COMPARATOR
UC33 7485L$ 4-BIT COMPARATOR
UC34 7485L$ 4-BIT COMPARATOR
WDR TE
UF1B 7408$
UEDIF 006
UE32 7430$
UH26E 7404L$
UJ27D 7402L$
UE31A 7402L$
UE30A 7474 CLK L$ SET RST
TP20
DACSTRB (STRBDSPL1)
UE11E 7404L$
P1
INT I BLNK
FR I BLNK
DSPL I FRCMP
WDRATE
MBITW
STRBDSPLFP
STRBDSPL1
UJ26C 7400L$
UJ26D 7400L$
EXTSTRT FR
WORD DISPLAY LOCATION CONTROL
Schlumberger
SCHEM, PWA,
WORD SELECT & DISPLAY
D 06141 34597 L

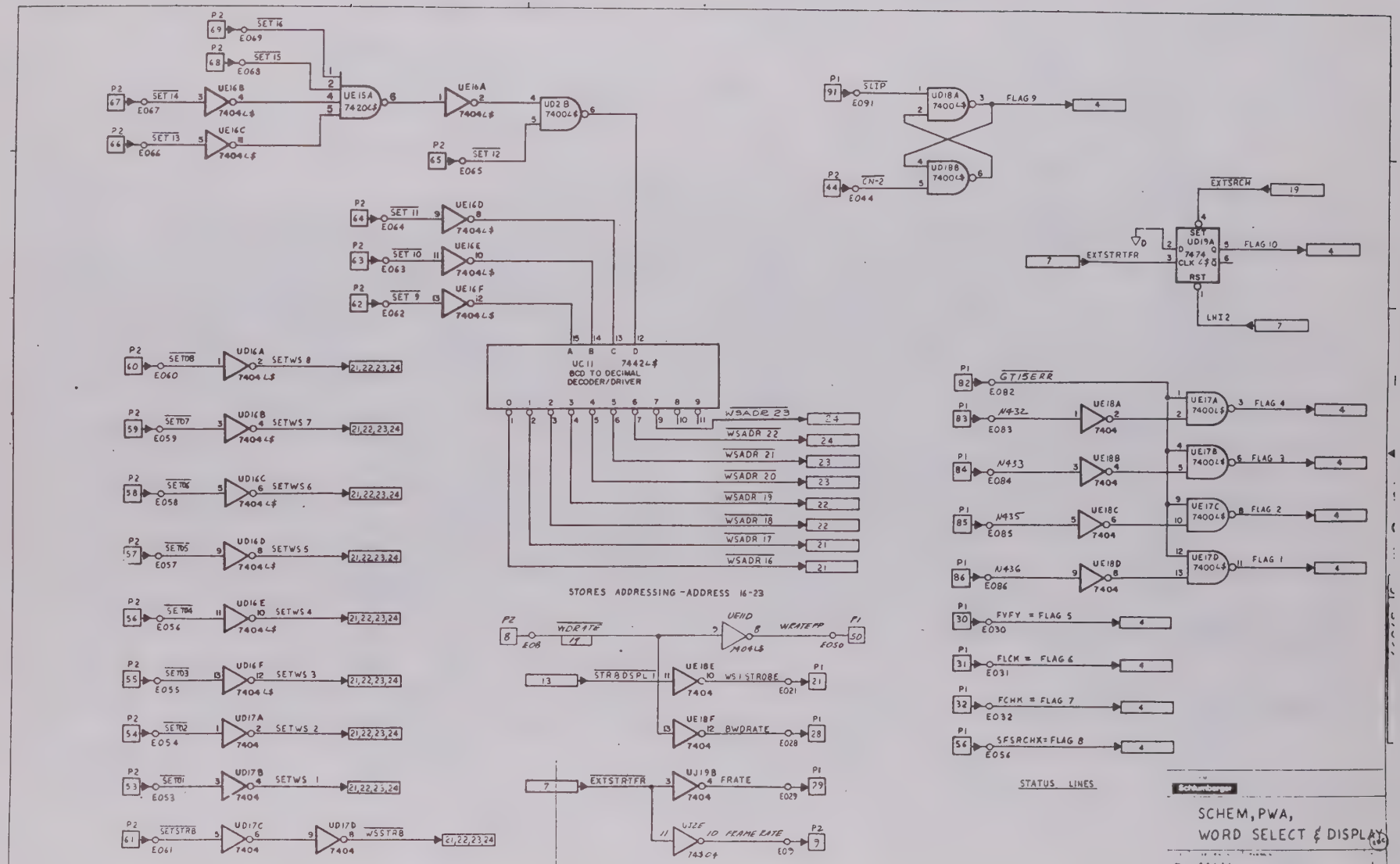

BCDTTH 4
BCDTTH 2
BCDTTH 1
LSB 16
BCDTH 1
LSB 15
BCDTH 2
LSB 14
BCDTH 4
LSB 13
BCDTH 8
LSB 12
BCDH 1
LSB 11
BCDH 2
LSB 10
BCDH 4
LSB 9
BCDH 8
LSB 08
BCDT 1
LSB 07
BCDT 2
LSB 06
BCDT 4
LSB 05
BCDT 8
LSB 04
LSB 03
BCDU 2
LSB 02
BCDU 4
LSB 01
BCDU 8
UB22 74175L$ 4-BIT REG
UB21 74157L$ QUAD 2-INPUT MUX
UB20 74175L$ 4-BIT REG
UB19 74157L$ QUAD 2-INPUT MUX
UB18 74175L$ 4-BIT REG
UB17 74157L$ QUAD 2-INPUT MUX
UB16 74175L$ 4-BIT REG
UB15 74157L$ QUAD 2-INPUT MUX
UC14 74175L$ 4-BIT REG
UC13 74157L$ QUAD 2-INPUT MUX
UC22 74157L$ QUAD 2-INPUT MUX
UC20 74157L$ QUAD 2-INPUT MUX
UC18 74157L$ QUAD 2-INPUT MUX
UC16 74157L$ QUAD 2-INPUT MUX
UC21 74157L$ QUAD 2-INPUT MUX
UC19 74157L$ QUAD 2-INPUT MUX
UC17 74157L$ QUAD 2-INPUT MUX
UC15 74157L$ QUAD 2-INPUT MUX
UC12 74157L$ QUAD 2-INPUT MUX
STRBDSPL 1
LHI 3
LHI 2
LHI 4
DISPLBIN
DISPSEL
LNG 3
H7-3
BIT 19
BIT 18
BIT 17
BIT 16
BIT 15
BIT 14
BIT 13
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
LOCDATA 5
LOCDATA 4
LOCDATA 3
LOCDATA 2
LOCDATA 1
UD25E
UD25D
UD25F
UE11B
UE11A
7404L$
DD5CIN
DD5DIN
DD5BIN
DD5AIN
DD4CIN
DD4DIN
DD4BIN
DD4AIN
DD3CIN
DD3DIN
DD3BIN
DD3AIN
DD2CIN
DD2DIN
DD2BIN
DD2AIN
DD1CIN
DD1DIN
DD1BIN
DD1AIN
CURSOR 5
CURSOR 4
CURSOR 3
CURSOR 2
CURSOR 1
WIPSEL
UD8A
UD8B
UD7C
UD7D
UD7E
UD7F
UD6E
UD6D
UD6C
UD7B
UD7A
UD6B
7402L$
7405L$
DD5DP
DD4DP
DD3DP
DD2DP
DD1DP
BINART/BCD SWITCH & DATA DISPLAY BITS 1-5
SCHEM, PWA, WORD SELECT & DISPLAY
D 06141
39537



WORD DISPLAY STROBE CONTROL


DISPLBIN
DISPSEL
UD15D 7408
UJ26A 7400
UJ18F 7404
UD14B 7408
UD14A 7408
UD13D 7408
UD13C 7408
UD13B 7408
UD13A 7408
UD12C 7408
UD12B 7408
UD12A 7408
UD11C 7438
UD11B 7438
UD11A 7438
UD10D 7438
UD10C 7438
UD10B 7438
UD10A 7438
UD9C 7438
UD9D 7438
UD8D 7402
UD8C 7402
UD8B 7402
UE12E 7405
UE12F 7405
UE12D 7405
UE12C 7405
UE12B 7405
UE12A 7405
UE14C 7405
UE14B 7405
UE10F 7405
UE8D 7405
UE8C 7405
UE8B 7405
UD15C 7408
UD15B 7408
UD15A 7408
UD14C 7408
UD14D 7408
UD12D 7438
UD12C 7438
UE13F 7405
UE13A 7405
UD12A 7438
UD12B 7438
UE13D 7405
UE13E 7405
UD11D 7438
UE13C 7405
LNG 3
LNG 8
LNG 7
LNG 6
LNG 5
RIP
LNG 10
LNG 11
LNG 12
LNG 13
LNG 14
LNG 15
BIT 9
BIT 8
BIT 7
BIT 6
BIT 10
BIT 11
BIT 12
BIT 13
BIT 14
BIT 15
BIT 16
DISPSEL
UD8B
DD9 SEGDEGPD
DD8 SEGDEGPD
DD7SEG DEGPD
DD6 SEGDEGPD
DD10 SEGDEGPD
DD11 SEGDEGPD
DD12 SEG DEGPD
DD13 SEG DEGPD
DD14 SEGDEGPD
DD15 SEG DEGPD
DD16 SEG DEGPD
DD9 SEG CPD
DD8 SEG CPD
DD7 SEG CPD
DD6 SEG CPD
DD10 SEG CPD
DD11 SEG CPD
DD12 SEG CPD
DD13 SEG CPD
DD14 SEG CPD
DD15 SEG CPD
DD16 SEG CPD
LOCDATA 8
LOCDATA 7
LOCDATA 6
CURSOR 8
CURSOR 7
CURSOR 6
DD8DP
DD7DP
DD6DP
DISPSEL
UH16D
DATA DISPLAY BITS 6-16
SCHEM, PWA,
WORD SELECT & DISPLAY
D 06141 34597 L


SCHEM, PWA,
WORD SELECT & DISPLAY
D 06141 34597 L
DATA WORD LENGTH MEMORY & DECODE
UC1 4-BIT FULL ADDER 74283L$
UA4 4-BIT REG 74175L$
UA5 DCDR/DEMUX 74155L$
UA6 DCDR/DEMUX 74155L$
DD1 SEGCPD
DD2 SEGCPD
DD3 SEGCPD
DD4 SEGCPD
DD5 SEGCPD
DISPSEL
DISPLBIN
RBD2IN
RBD3OUT
RBD3IN
RBD4OUT
RBD4IN
RBD5OUT
STRIP PAR ON
EXT STRT FR
FWD TM
PRE EOW
XWD LNG3
XWD LNG2
XWD LNG1
XWD LNG0
SUM0
SUM1
SUM2
SUM3
LNG3
LNG2
LNG1
LNG7
LNG6
LNG5
LNG4
LNG15
LNG14
LNG13
LNG12
LNG11
LNG10
LNG9
LNG8
WD/ENAB
STATUS TM
STRB DSPLT
RAI7A
E004
H7-3
RIP



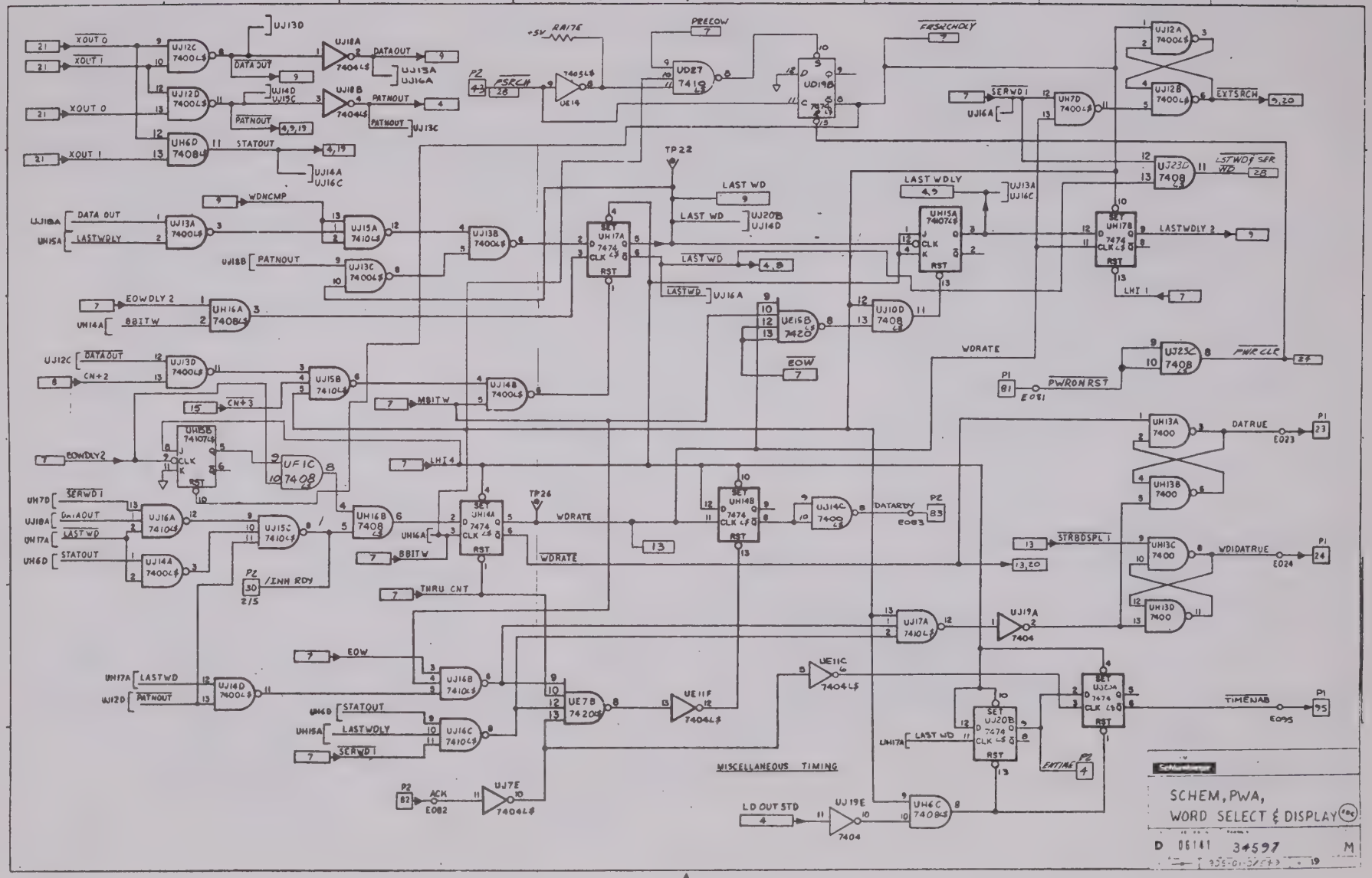
Schlumberger

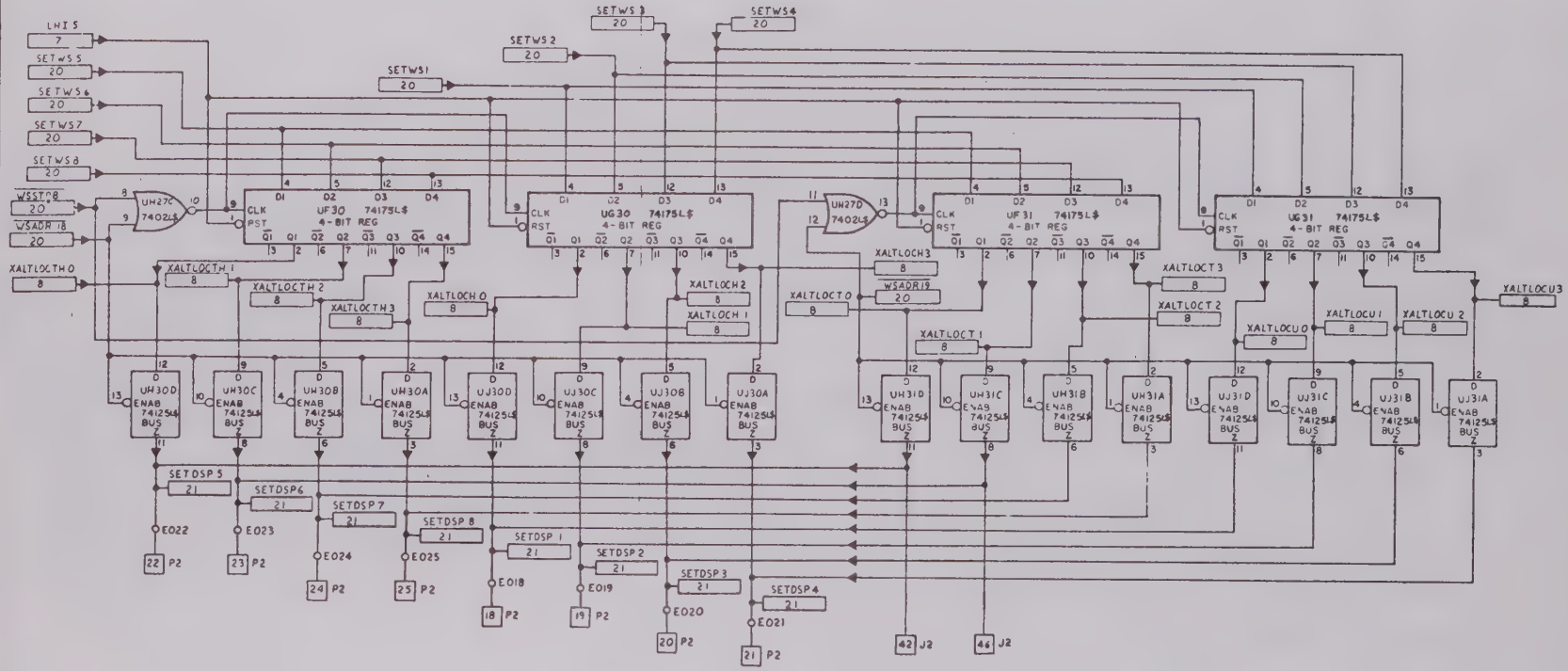
SCHEM, PWA,
WORD SELECT & DISPLAY

D 06141 24597 L

905-01-0

9-56

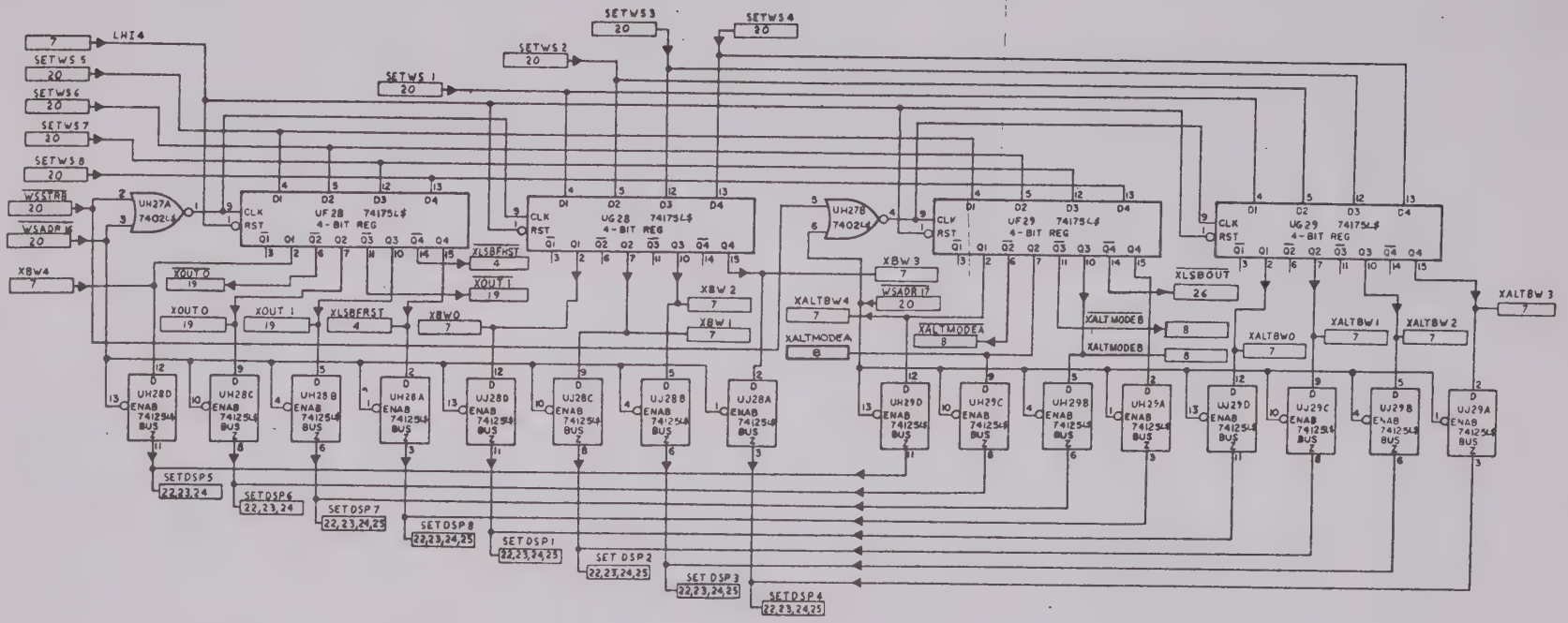

SCHEM, PWA,
WORD SELECT & DISPLAY
D 06141 34597 M
MISCELLANEOUS TIMING



SETUP STORES 1-18 & 1-19

SCHEM, PWA,
WORD SELECT & DISPLAY

D | 14597 | L

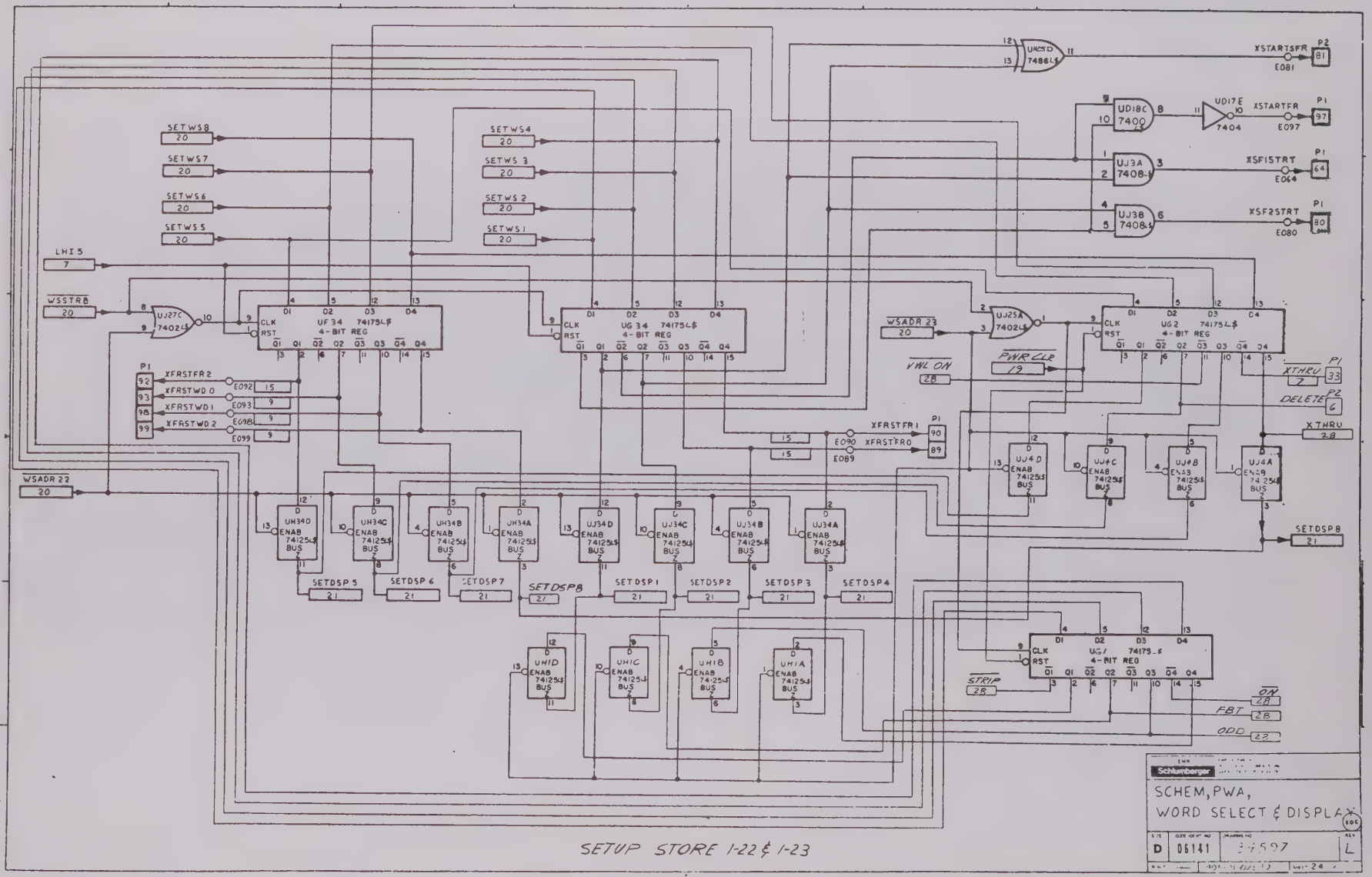


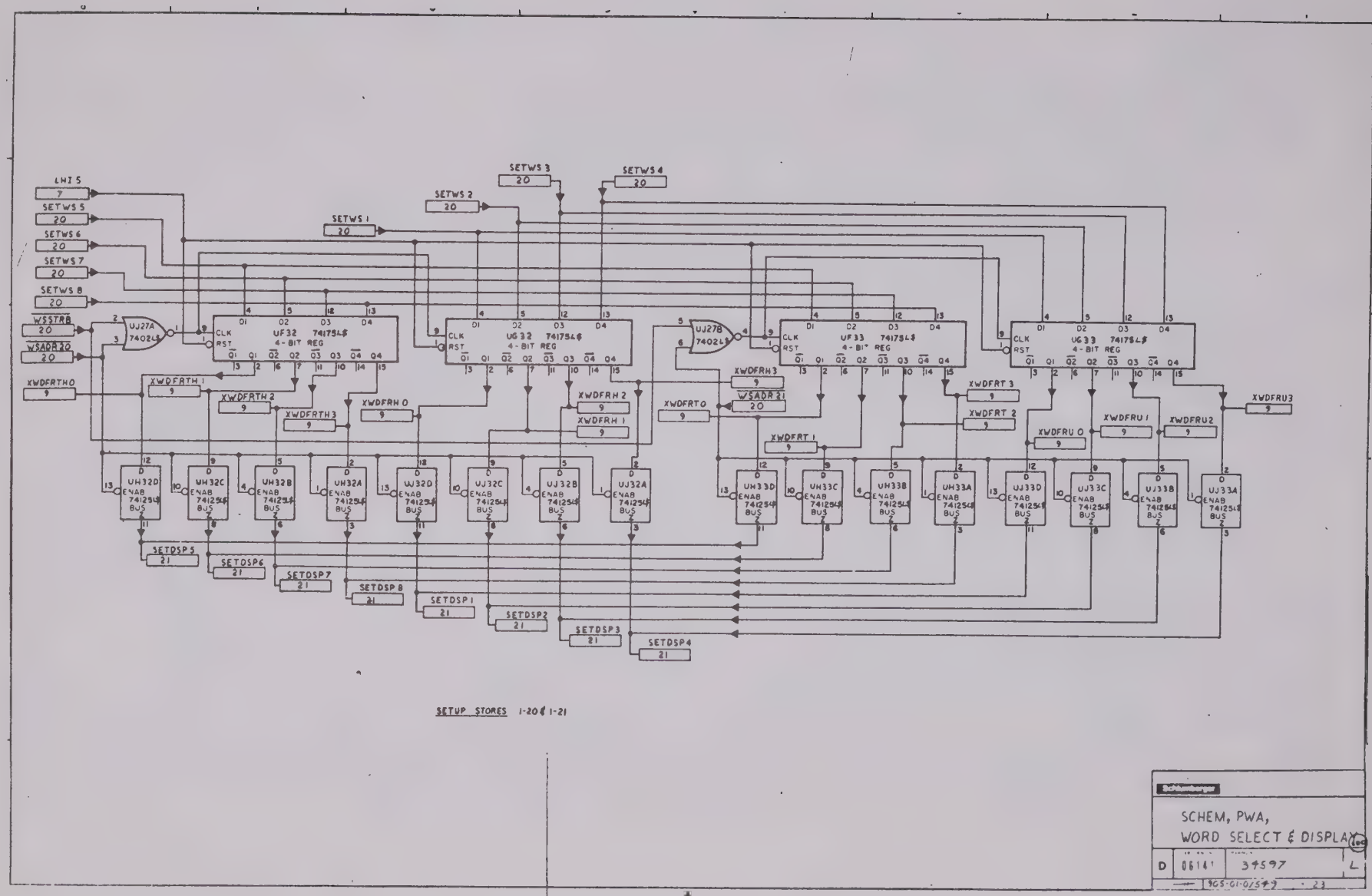
SETUP STORES 1-16 & 1-17

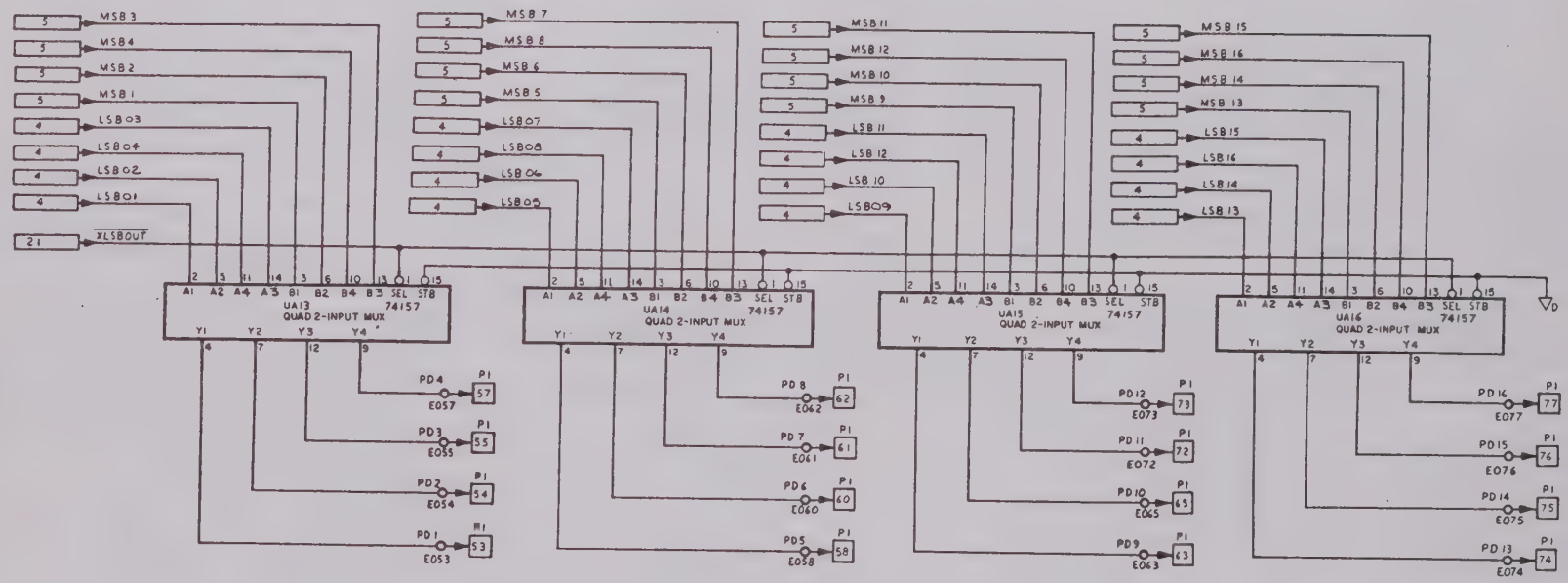
SCHEM, PWA,
WORD SELECT & DISPLAY

D | 05:41 | 34597 | L

905-01-01549 | 21


SETWS8
SETWS7
SETWS6
SETWS5
SETWS4
SETWS3
SETWS2
SETWS1
LHIS
WSSTRB
WSADR22
WSADR23
VWLON
PWRCLR
XFRSTFR2
XFRSTWD0
XFRSTWD1
XFRSTWD2
XFRSTFR1
XFRSTFR0
XSTARTSFR
XSTARTFR
XSF1STRT
XSF2STRT
XTHRU
DELETE
SETDSP1
SETDSP2
SETDSP3
SETDSP4
SETDSP5
SETDSP6
SETDSP7
SETDSP8
STRIP
ON
FBT
ODD
SCHEM,PWA,
WORD SELECT & DISPLAY
D
06141
37597
L
SETUP STORE 1-22 & 1-23
6-09

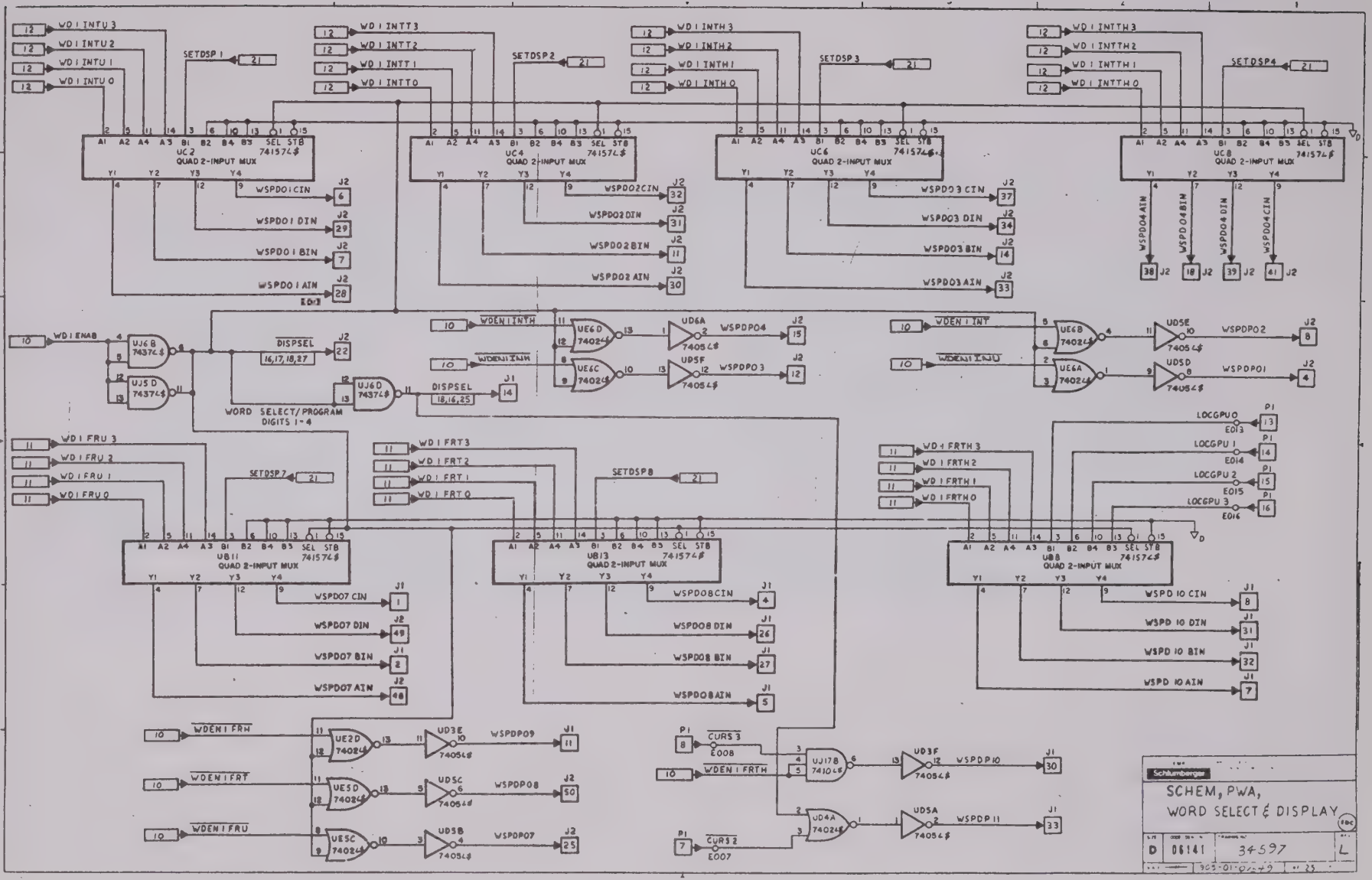

LHI 5
SETWS 5
SETWS 6
SETWS 7
SETWS 8
WSSTRB
WSADR 20
XWDFRTH 0
XWDFRTH 1
XWDFRTH 2
XWDFRTH 3
XWDFRH 0
XWDFRH 2
XWDFRH 1
XWDFRH 3
XWDFRT 0
XWDFRT 1
XWDFRT 2
XWDFRT 3
XWDFRU 0
XWDFRU 1
XWDFRU 2
XWDFRU 3
SETWS 1
SETWS 2
SETWS 3
SETWS 4
UJ27A 7402LS
UF32 74175LS 4-BIT REG
UG32 74175LS 4-BIT REG
UJ27B 7402LS
UF33 74175LS 4-BIT REG
UG33 74175LS 4-BIT REG
UH32D
UH32C
UH32B
UH32A
UJ32D
UJ32C
UJ32B
UJ32A
UH33D
UH33C
UH33B
UH33A
UJ33D
UJ33C
UJ33B
UJ33A
SETDSP 5
SETDSP 6
SETDSP 7
SETDSP 8
SETDSP 1
SETDSP 2
SETDSP 3
SETDSP 4
SETUP STORES 1-20 & 1-21
SCHEM, PWA,
WORD SELECT & DISPLAY
D
06141
34597
L
905-01-01549

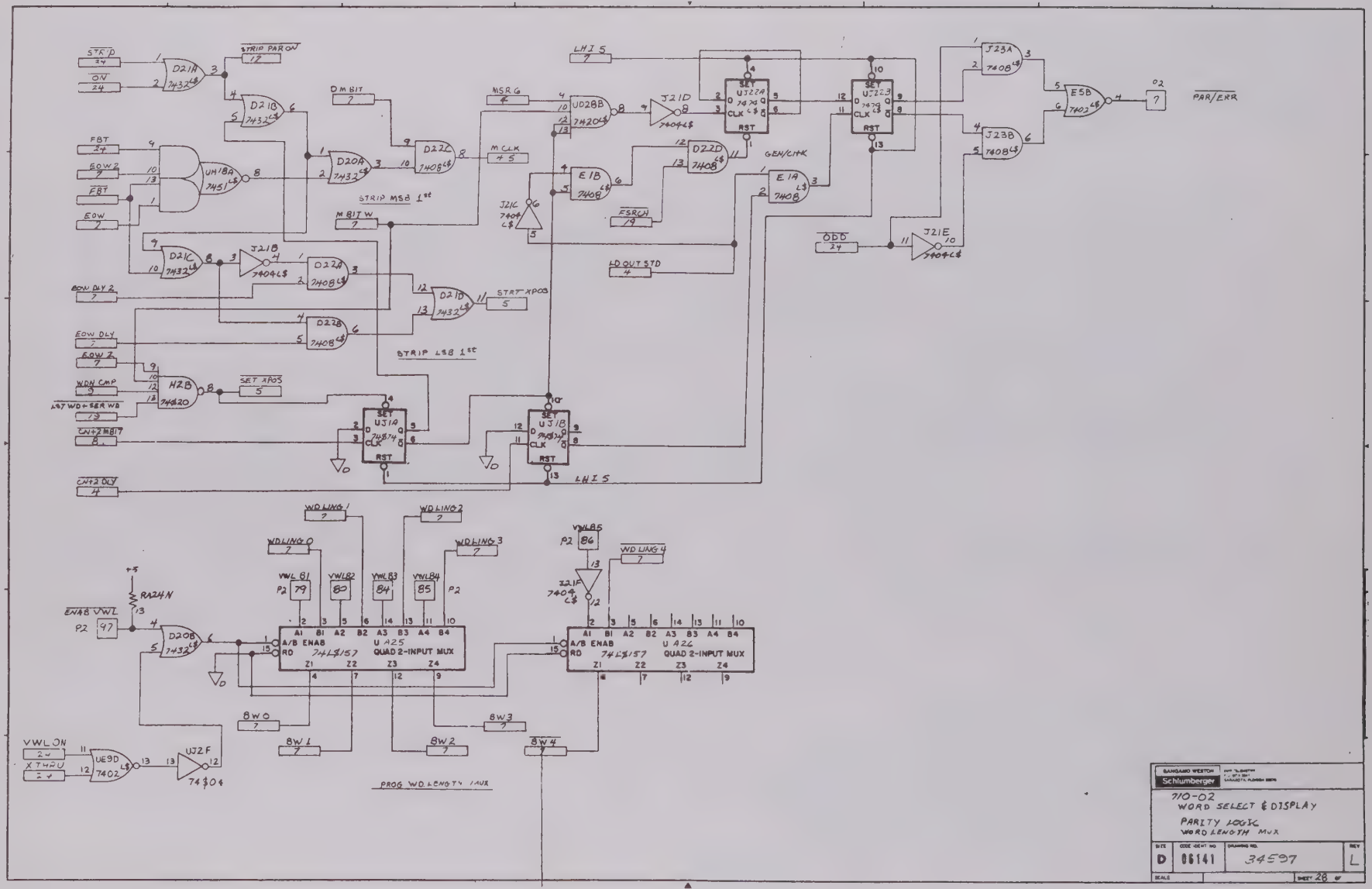


Schlumberger

SCHEM, PWA,
WORD SELECT & DISPLAY

D 06141 345937

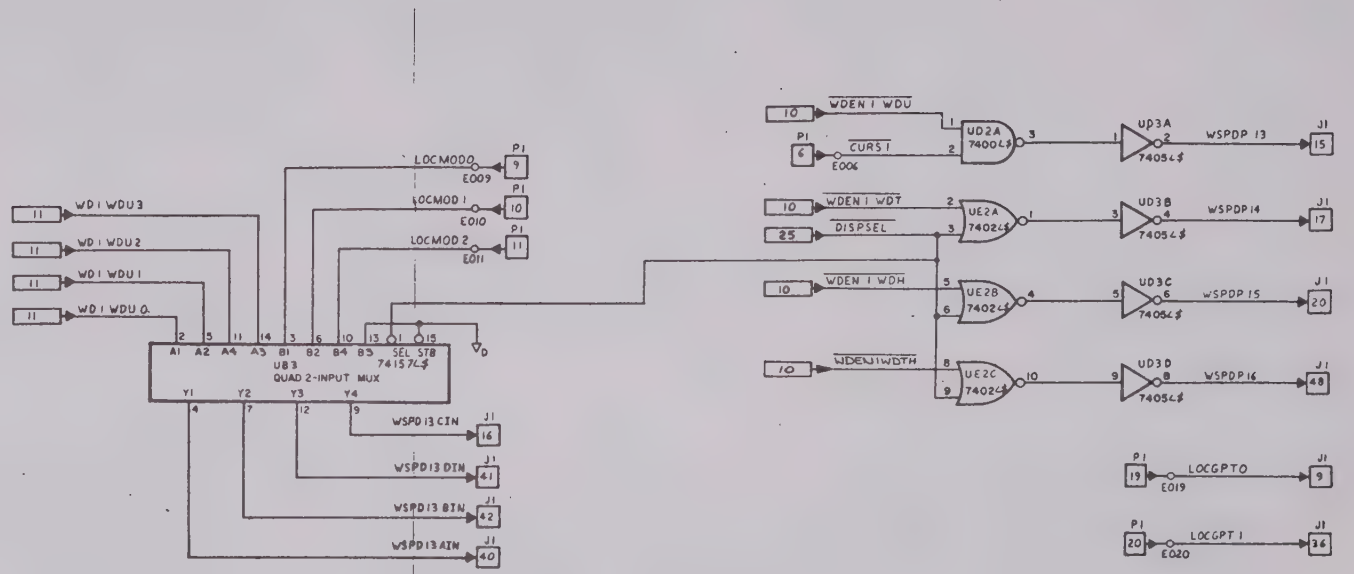

WD I INTU 3
WD I INTU 2
WD I INTU 1
WD I INTU 0
SETDSP 1
UC2
QUAD 2-INPUT MUX
WSPDO1CIN
WSPDO1 DIN
WSPDO1 BIN
WSPDO1 AIN
WD I INTT 3
WD I INTT 2
WD I INTT 1
WD I INTT 0
SETDSP2
UC4
QUAD 2-INPUT MUX
WSPDO2CIN
WSPDO2DIN
WSPDO2BIN
WSPDO2AIN
WD I INTH 3
WD I INTH 2
WD I INTH 1
WD I INTH 0
SETDSP3
UC6
QUAD 2-INPUT MUX
WSPDO3 CIN
WSPDO3 DIN
WSPDO3BIN
WSPDO3AIN
WD I INTTH 3
WD I INTTH 2
WD I INTTH 1
WD I INTTH 0
SETDSP4
UC8
QUAD 2-INPUT MUX
WSPDO4AIN
WSPDO4BIN
WSPDO4DIN
WSPDO4CIN
WD I ENAB
UJ6B 74374
UJ5D 74374
DISPSEL
16,17,18,27
DISPSEL
18,16,25
WORD SELECT/PROGRAM DIGITS 1-4
WDEN I INTH
WDEN I INTH
UE6D 74024
UE6C 74024
UD6A
UD5F
7405 4
WSPDPO4
WSPDPO3
WDEN I INT
WDEN I INTU
UE6B 74024
UE6A 74024
UD5E
UD5D
7405 4
WSPDPO2
WSPDPO1
WD I FRU 3
WD I FRU 2
WD I FRU 1
WD I FRU 0
SETDSP7
UB11
QUAD 2-INPUT MUX
WSPDO7 CIN
WSPDO7 DIN
WSPDO7 BIN
WSPDO7 AIN
WD I FRT 3
WD I FRT 2
WD I FRT 1
WD I FRT 0
SETDSP8
UB13
QUAD 2-INPUT MUX
WSPDO8CIN
WSPDO8 DIN
WSPDO8 BIN
WSPDO8AIN
WD I FRTH 3
WD I FRTH 2
WD I FRTH 1
WD I FRTH 0
LOCGPU 0
LOCGPU 1
LOCGPU 2
LOCGPU 3
UB8
QUAD 2-INPUT MUX
WSPD 10 CIN
WSPD 10 DIN
WSPD 10 BIN
WSPD 10 AIN
WDEN I FRH
WDEN I FRT
WDEN I FRU
UE2D 74024
UE5D 74024
UE5C 74024
UD3E
UDSC
UD3B
7405 4
WSPDPO9
WSPDPO8
WSPDPO7
CURS 3
CURS 2
WDEN I FRTH
UJ17B 74104
UD4A 74024
UD3F
UDSA
7405 4
WSPDP10
WSPDP11
Schlumberger
SCHEM, PWA,
WORD SELECT & DISPLAY
D
06141
34597
L
905-01-0249



710-02
WORD SELECT & DISPLAY
PARITY LOGIC
WORD LENGTH MUX

SIZE	CODE IDENT NO	DRAWING NO.	REV
D	06141	34597	L

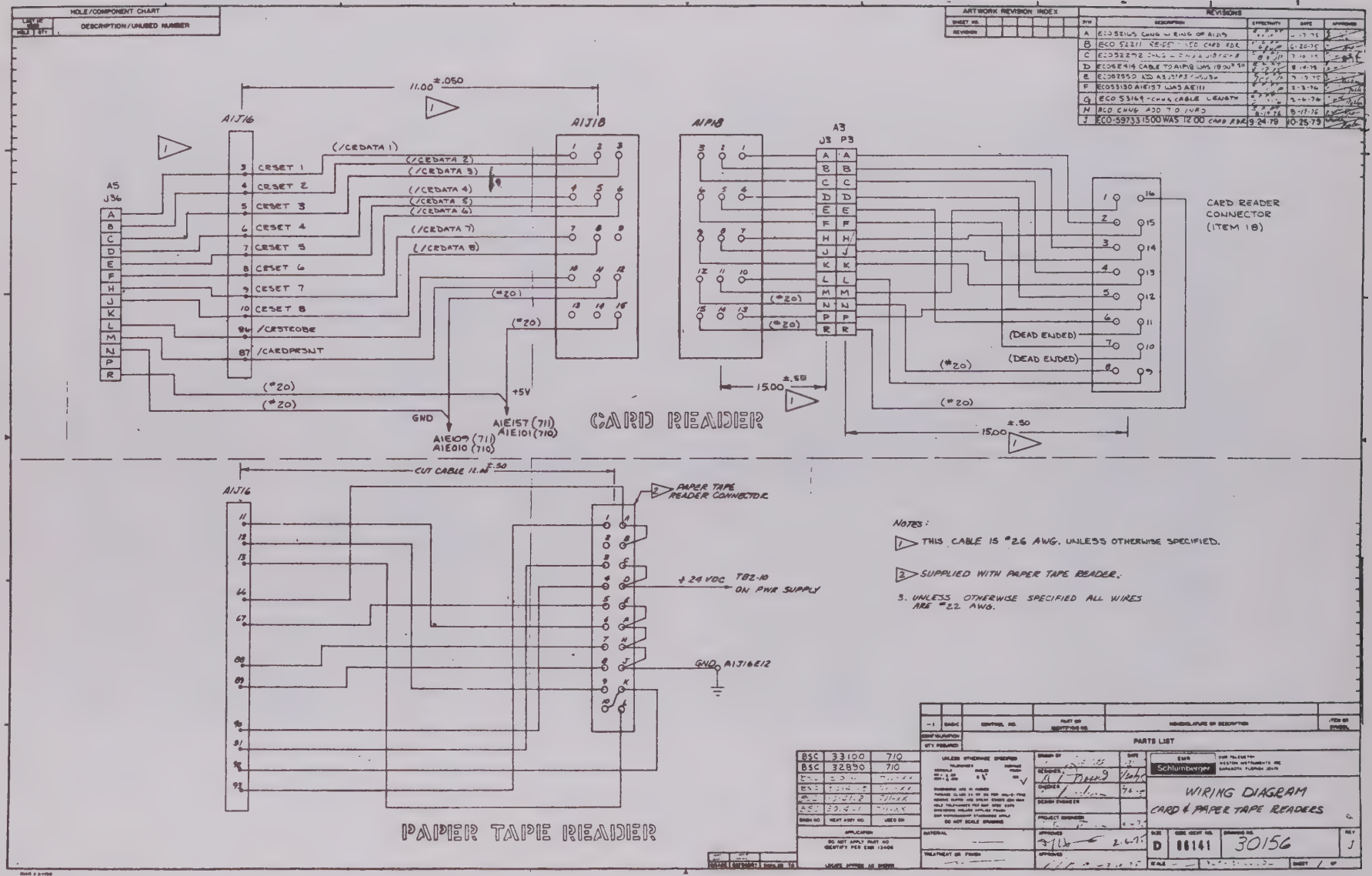
SCALE | SHEET 28 OF



Schlumberger

SCHEM, PWA,
WORD SELECT & DISPLAY

D 06141


HOLE/COMPONENT CHART
DESCRIPTION/UNUSED NUMBER
ARTWORK REVISION INDEX
REVISIONS
A1J16
A1J1B
A1P1B
A3 J3 P3
A5 J36
11.00 ±.050
(/CEDATA 1)
(/CEDATA 2)
(/CEDATA 3)
(/CEDATA 4)
(/CEDATA 5)
(/CEDATA 6)
(/CEDATA 7)
(/CEDATA 8)
CRESET 1
CRESET 2
CRESET 3
CRESET 4
CRESET 5
CRESET 6
CRESET 7
CRESET 8
/CRSTCOBE
/CARDPRSNT
(*20)
+5V
GND
A1E57 (711)
A1E101 (710)
A1E09 (711)
A1E010 (710)
CARD READER
CARD READER CONNECTOR (ITEM 18)
(DEAD ENDED)
15.00
±.50
CUT CABLE 12.00 ±.50
PAPER TAPE READER CONNECTOR
+24 VDC TB2-10 ON PWR SUPPLY
GND A1J16E12
PAPER TAPE READER
NOTES:
1. THIS CABLE IS #26 AWG. UNLESS OTHERWISE SPECIFIED.
2. SUPPLIED WITH PAPER TAPE READER.
3. UNLESS OTHERWISE SPECIFIED ALL WIRES ARE #22 AWG.
PARTS LIST
WIRING DIAGRAM
CARD & PAPER TAPE READERS
Schlumberger
D
88141
30156
J

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
1	DGND	1	10
2	+5V	1	10
3	/LDFRCTRX	15	5/8
4	DISPLBIN	17	FP/3
5	CLKFRCTRX	15	5/8
6	/CUR31	27	4/5
7	/CUR32	25	4/5
8	/CUR33	25	4/5
9	LOCMOD0	27	4/5
10	LOCMOD1	27	4/5
11	LOCMOD2	27	4/5
12	/STEP	11	FP/3
13	LOCGPU0	25	4/5
14	LOCGPU1	25	4/5
15	LOCGPU2	25	4/5
16	LOCGPU3	25	4/5
17	/SETUPMOM	10	FP/3
18	/WDIMOM	10	FP/3
19	LOCGPT0	27	4/5
20	LOCGPT1	27	4/5
21	WORD SELSTROBE	20	RP/J34G4
22	/FREE3E	10	FP/3
23	DATRUE	19	9/5
24	WDIDATRUE	19	9/5
25	/WDINC	9	4/7 2/5
26	/WDRS	9	4/7 2/5
27	WDPRESEN	9	RP/J34H13
28	WORD RATE	20	RP/J34G2,
29	FRATE	20	RP/J33G10
30	FVFY	20	4/11
31	FLCK	20	4/11
32	FCHK	20	4/11
33	/XTHRU	24	4/7
34	/LOCDATA1	16	4/4
35	/LOCDATA2	16	4/4
36	/LOCDATA3	16	4/4
37	/LOCDATA4	16	4/4
38	/LOCDATA5	16	4/4
39	/LOCDATA6	18	4/4
40	/LOCDATA7	18	4/4
41	/LOCDATA8	18	4/4
42	/CURSOR1	16	4/4
43	/CURSOR2	16	4/4
44	/CURSOR3	16	4/4
45	/CURSOR4	16	4/4
46	/CURSOR5	16	4/4
47	/CURSOR6	18	4/4
48	/CURSOR7	18	4/4
49	/CURSOR8	18	4/4
50	W RATEFP	20	FP/4

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
51	DGND		10
52	+5V	1	10
53	PRLDATAOUT 1	26	RP/J34A2
54	PRLDATAOUT 2	26	RP/J34A4
55	PRLDATAOUT 3	26	RP/J34A6
56	SFSRCHX	20	5/8
57	PRLDATAOUT 4	26	RP/J34A8
58	PRLDATAOUT 5		RP/J34A10
59	SFONX	14	5/8
60	PRLDATAOUT 6	26	RP/J34A12
61	PRLDATAOUT 7	26	RP/J34D13
62	PRLDATAOUT 8	26	RP/J34C2
63	PRLDATAOUT 9	26	RP/J34C4
64	XSF1STRT	24	5/11
65	PRLDATAOUT 10	26	RP/J34C6
66	FLAG 11	4	RP/J32E12
67	FLAG 12	4	RP/J32H13
68	FLAG 13	4	RP/J32G2
69	FLAG 14	4	RP/J32G4
70	FLAG 15	4	RP/J32G6
71	FLAG 16	4	RP/J32G8
72	PRLDATAOUT 11	26	RP/J34C8
73	PRLDATAOUT 12	26	RP/J34C10
74	PRLDATAOUT 13	26	RP/J34C12
75	PRLDATAOUT 14	26	RP/J34E2
76	PRLDATAOUT 15	26	RP/J34E4
77	PRLDATAOUT 16	26	RP/J34E6
78	/LDWSDFRCTR	15	9/2
79	CLKWSDFRCTR	15	9/2
80	XSF2STRT	24	5/23
81	/PNRONRST	19	4/8
82	/GT15ERR	20	4/13
83	N432	20	4/13
84	N433	20	4/13
85	N435	20	4/13
86	N436	20	4/13
87	CLKWSDWCTR	9	9/3
88	/LDWSDWCTR	9	9/3
89	XFRSTFR0	24	9/2
90	XFRSTFR1	24	9/2
91	/SLIP	20	4/10
92	XFRSTFR2	24	9/2
93	XFRSTWD0	24	9/3, 2/2
94	/EXTSTRTFR	7	5/11, 5/23, 10/6
95	/TIMENAB	19	4/7, 2/5
96	EXTSTRTSFR	7	10/6
97	XSTARTFR	24	10/6
98	XFRSTWD1	24	9/3, 2/2
99	XFRSTWD2	24	9/3, 2/2
100	STRBDSPLFP	13	FP4

P2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
1	IDONX	15	5/8
2	/ SFSRCHX	15	5/8
3	/FRNFFX	7	5/11
4	ENTIME	19	2/5
5	FRNFFX	14	5/8
6	DELETE	24	2/5
7	/MAR-ERR	28	4/7, 2/5
8	/WDRATE	20	3/5
9	FRAME RATE	20	RP/J34PE12
10			
11			
12			
13			
14			
15			
16			
17			
18	SETDSP1	22	4/16
19	SETDSP2	22	4/16
20	SETDSP3	22	4/16
21	SETDSP4	22	4/16
22	SETDSP5	22	4/16
23	SETDSP6	22	4/16
24	SETDSP7	22	4/16
25	SETDSP8	22	4/16
26			
27			
28			
29			
30	/INH RDY	19	2/3
31	F SRCH DLY	7	2/3
32	BCDTTH2	6	9/4
33	BCDTTH4	6	9/4
34	LSB01	4	9/4, 10/6
35	LSB02	4	9/4, 10/6
36	LSB03	4	9/4, 10/6
37	LSB04	4	9/4, 10/6
38	/BBIT	7	4/7
39	/MBIT	7	4/7
40	LSB05	4	9/4, 10/6
41	CN+2	8	4/12
42	EOW	7	2/5
43	/FSRCH	7	4/11
44	/CN-2	20	4/12
45	CN+1	7	4/12
46	/CPWIN	7	4/7
47	/EOW2	7	2/5
48	/CN+2DLY	4	4/12
49	+5V	1	10
50	DGND	1	10

P2

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
51	LSB06	4	9/4, 10/6
52	LSB07	4	9/4, 10/6
53	/SET01	20	4/5
54	/SET02	20	4/5
55	/SET03	20	4/5
56	/SET04	20	4/5
57	/SET05	20	4/5
58	/SET06	20	4/5
59	/SET07	20	4/5
60	/SET08	20	4/5
61	/SETSTRB	20	4/5
62	/SET09	20	4/5
63	/SET10	20	4/5
64	/SET11	20	4/5
65	/SET12	20	4/5
66	/SET13	20	4/5
67	/SET14	20	4/5
68	/SET15	20	4/5
69	/SET16	20	4/5
70	LSB11	4	9/4, 10/6
71	LSB12	4	9/4, 10/6
72	LSB13	4	9/4, 10/6
73	LSB08	4	9/4, 10/6
74	LSB09	4	9/4, 10/6
75	LSB10	4	9/4, 10/6
76	LSB14	4	9/4, 10/6
77	LSB15	4	9/4, 10/6
78	LSB16	4	9/4, 10/6
79	VWL B1	28	2/4
80	VWL B2	28	2/4
81	XSTARTSFR	24	10/6
82	ACK	19	RP/J31E10
83	DATARDY	19	RP/J31E8
84	VWL B3	28	2/4
85	VWL B4	28	2/4
86	VWL B5	28	2/4
87	MSRG	4	4/6
88	/CRWIN	7	4/10
89	/CURSRITE	10	4/4
90	/CURSLEFT	10	4/4
91	KEYMSB	10	4/5
92	KEYDATA2	10	4/5
93	KEYDATA1	10	4/5
94	KEYLSB	10	4/5
95	KEYSTRB	10	4/5
96	CN+3	15	4/12
97	/CN48 VWL	28	2/5
98	BW	7	2/2
99	+5V	1	10
100	DGND	1	10

ABBREVIATIONS USED FOR SIGNAL SOURCE AND/OR SIGNAL DESTINATION ADDRESSING & RELATED REF. DOCUMENTS ARE AS FOLLOWS:

FP = FRONT PANEL (DWG. 28070)
PS = POWER SUPPLY (DWG. 32945)
4 = CARD 4 (DWG 34595)
5 = CARD 5 (DWG 34599)
7 = CARD 7 (DWG. 34593)
8 = CARD 8 (DWG. 34597)
2 = CARD 2 (DWG 34307)

RP = REAR PANEL (DWG. ——— , REF I/O LIST DWG 32938) CONNECTIONS ARE INDICATED BY CONNECTOR "J" NO & PIN NO.

10 POWER WIRING SHOWN ON WIRING DIAGRAM 32945.

NOTES: CONTINUED

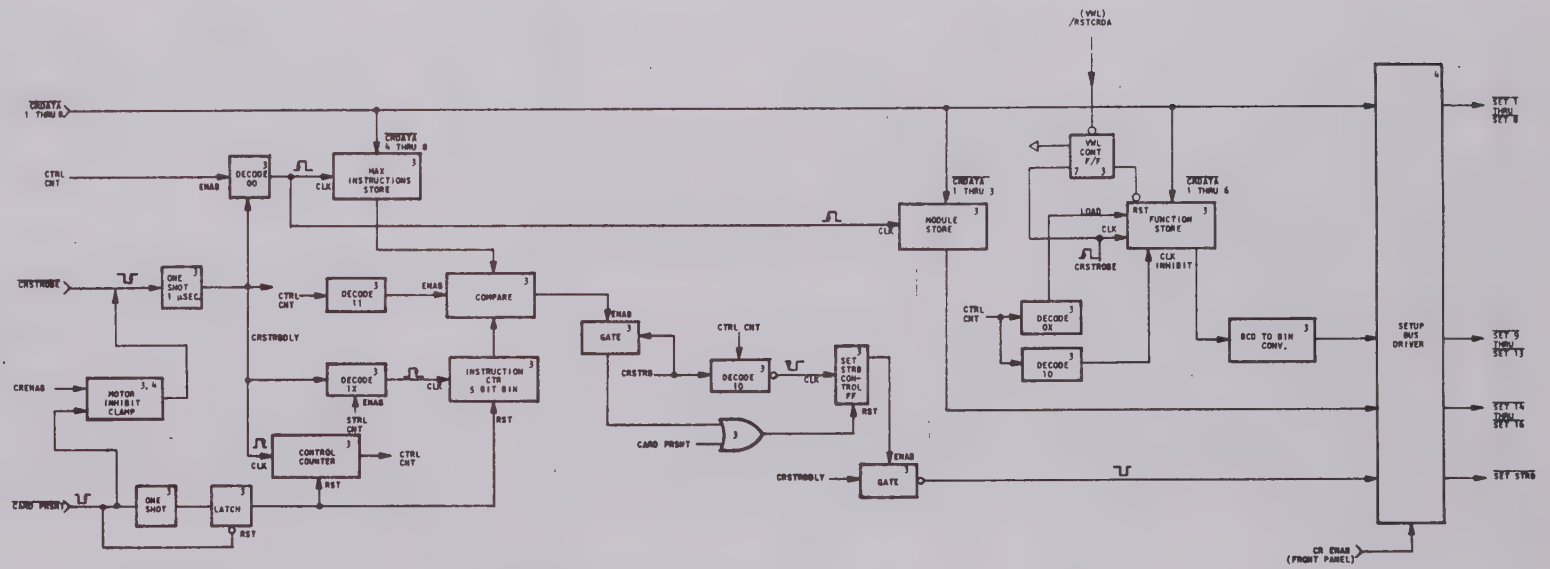
Schlumberger

SCHEMATIC, PWA,
WORD SELECT / DISPLAY
FUNCTION "8

SIZE	CODE IDENT NO	DRAWING NO	REV
D	05141	34597	M

SHEET 29

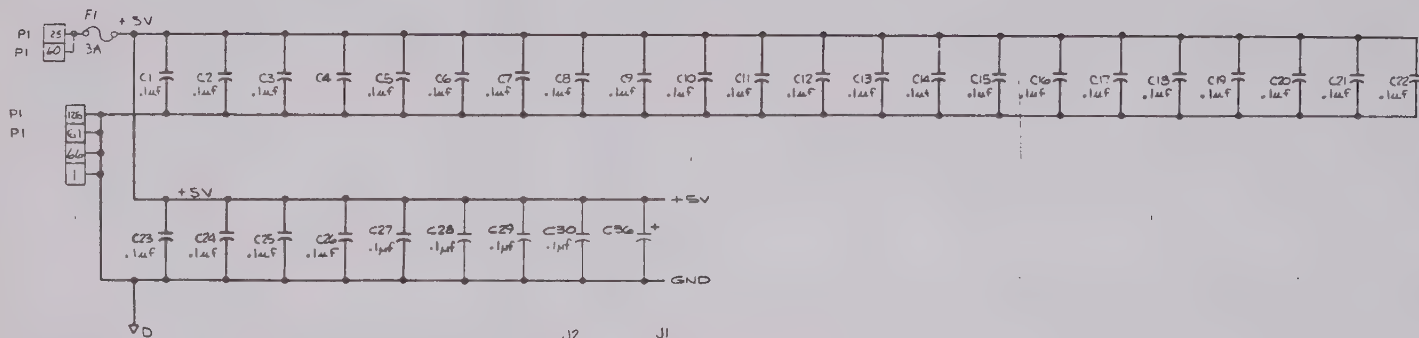
6-65

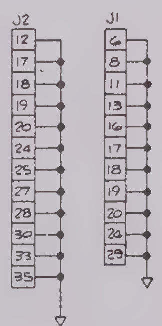


Schlumberger		SCHEM, PWA, DATA ENTRY	
SIZE D	CODE IDENT NO. 88141	DRAWING NO. 34309	REV A
SCALE —		SHEET 2 OF	

POWER PINS								
REF DES	+5V	GND						
U1	14	7	U19	16	8	U39	14	7
U2	14	7	U20	16	8	U40	14	7
U3	14	7	U21	16	8	U41	14	7
U4	14	7	U22	14	7	U42	14	7
U5	16	8	U23	14	7	U43	14	7
U6	14	7	U24	14	7	U44	14	7
U7	14	7	U25	14	7	U45	14	7
U8	16	8	U26	14	7	U46	14	7
U10	14	7				U47	14	7
U11	14	7	U28	16	8	U48	14	7
U12	5	10	U29	16	8	U49	16	8
U13	14	7	U30	14	7	U50	16	8
U14	14	7	U31	14	7	U51	16	8
U15	14	7	U32	14	7	U52	14	7
U16	14	7	U33	14	7	U53	16	8
U17	14	7	U34	14	7	U54	14	7
U18	8	1	U35	14	7			
			U36	14	7			
			U37	14	7			
			U38	14	7			

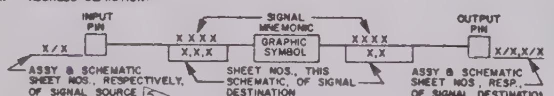
UNUSED CIRCUITS		
REF DES	TYPE	UNUSED CIRCUITS
U6	7414	F
U17	7404	A,B,D
U23	7414	C
U30	7404	A
U34	7404	C
U48	7404	F
U52	7404	E,F





NOTES:
UNLESS OTHERWISE SPECIFIED:

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.
2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.
3. CIRCUIT RETURN SYMBOLS: DIGITAL GND. ANALOG GND.
4. ADDRESS DEFINITION:



5. ABBREVIATIONS USED FOR SIGNAL SOURCE AND/OR SIGNAL DESTINATION ADDRESSING & RELATED REF. DOCUMENTS ARE AS FOLLOWS:
   - FP = FRONT PANEL (DWG. 28070)
   - PS = POWER SUPPLY (DWG. 32945)
   - 4 = CARD 4 (DWG. 34595)
   - 5 = CARD 5 (DWG 34599)
   - 7 = CARD 7 (DWG 34593)
   - RP = REAR PANEL (DWG. —, REF I/O LIST DWG 32738) CONNECTIONS ARE INDICATED BY CONNECTOR "J" NO. & PIN NO.
   - 8 = CARD 8 (DWG 34597)
6. ALL REFERENCES TO J1 & J2 ARE -1 CONFIG; J1 & J2 INTERFACE WITH COMPUTER MODULE
7. SEE SHEET 7 FOR NOTE 7

REVISIONS: D ECO 55935 REV CKT ON SEC.

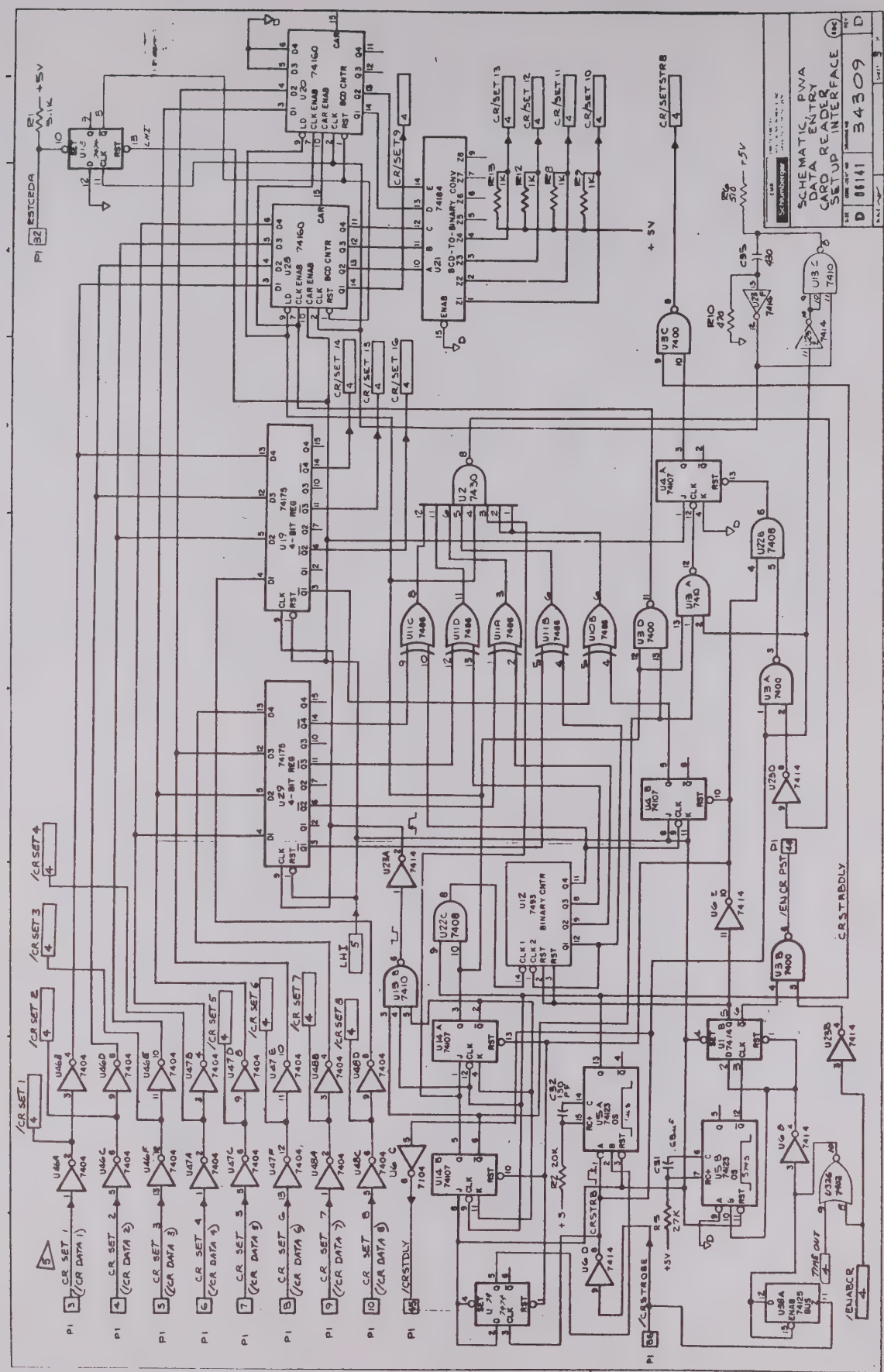
FUNCTION #10

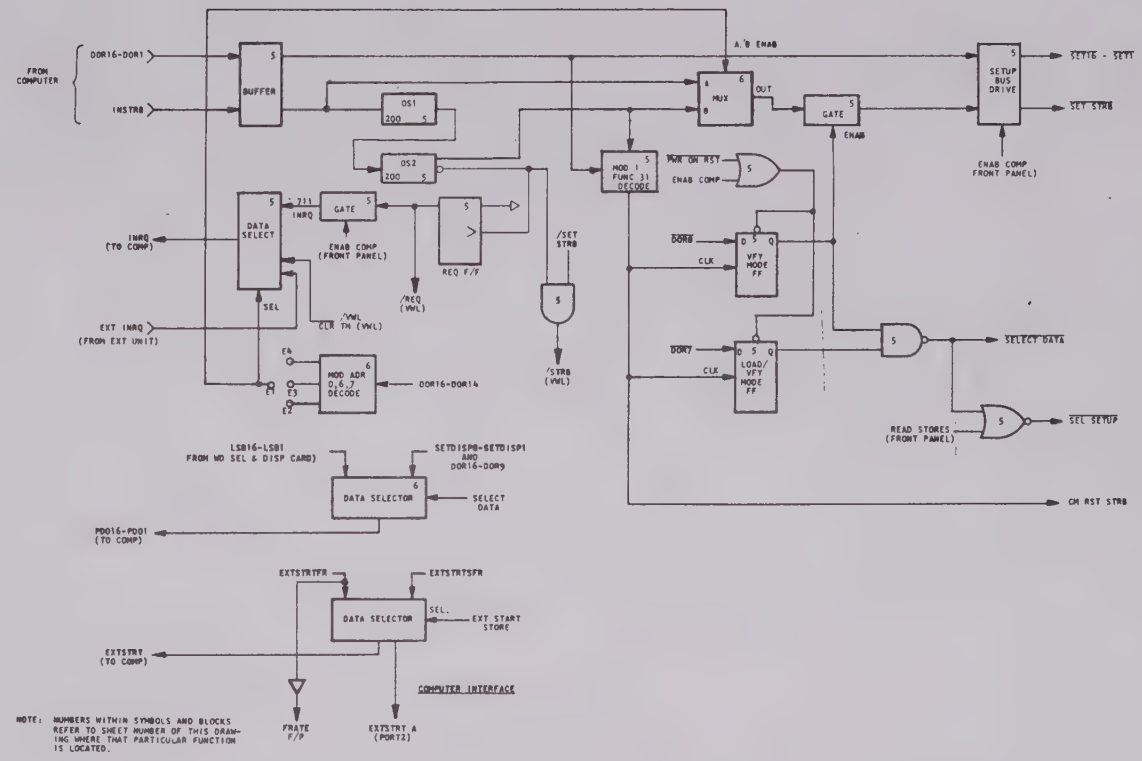
PARTS LIST

Schlumberger

SCHEMATIC, PWA DATA ENTRY

D 06141 34309 D


SCHEMATIC, PWA
DATA ENTRY
CARD READER
SETUP INTERFACE
34309
D
U20 74160
U28 74160
U21 74184
BCD-TO-BINARY CONV
U19 74175
4-BIT REG
U29 74175
4-BIT REG
U12 7493
BINARY CNTR
U2 7430
U1 74123
U5A 74123
U5B 74123
U36A 74125
U13 7410
U22C 7408
U28 7408
U3 7400
U4 7407
U14 7407
U23A 7414
U23B 7414
U6 7414
U46 7404
U47 7404
U48 7404
U11 7486
U10 7486
U26 7402
U32 7402
U6 7104
U12 7474
CR SET 1
CR SET 2
CR SET 3
CR SET 4
CR SET 5
CR SET 6
CR SET 7
CR SET 8
CR SET 9
CR SET 10
CR SET 11
CR SET 12
CR SET 13
CR SET 14
CR SET 15
CR SET 16
CR SETSTRB
CR DATA 1
CR DATA 2
CR DATA 3
CR DATA 4
CR DATA 5
CR DATA 6
CR DATA 7
CR DATA 8
CRSTDLY
CRSTRB
CRSTROBE
CRSTRBDLY
/EN CR PST
/ENABCR
TIME OUT
LHI
RSTCRDA
+5V
P1



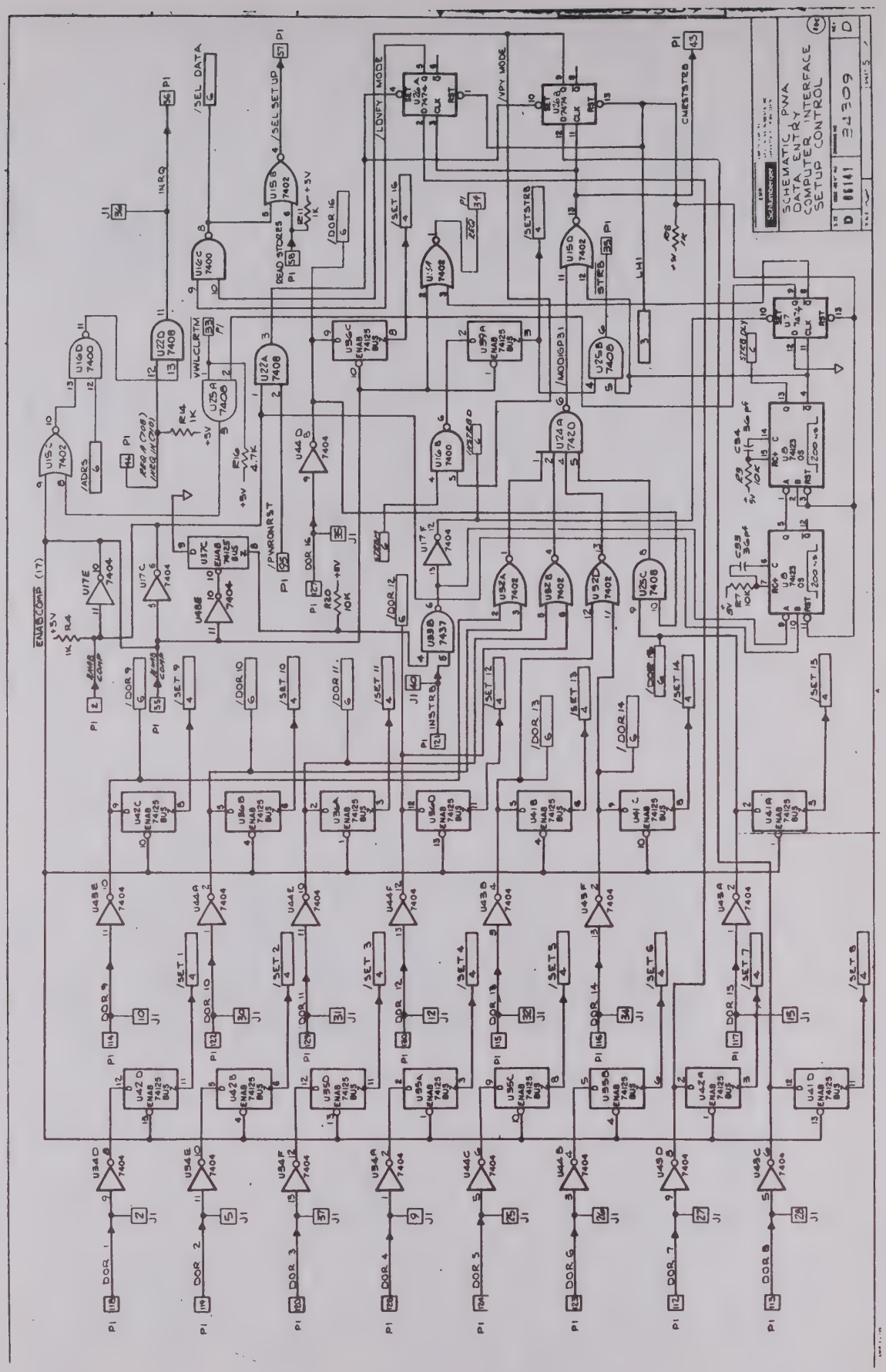
NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

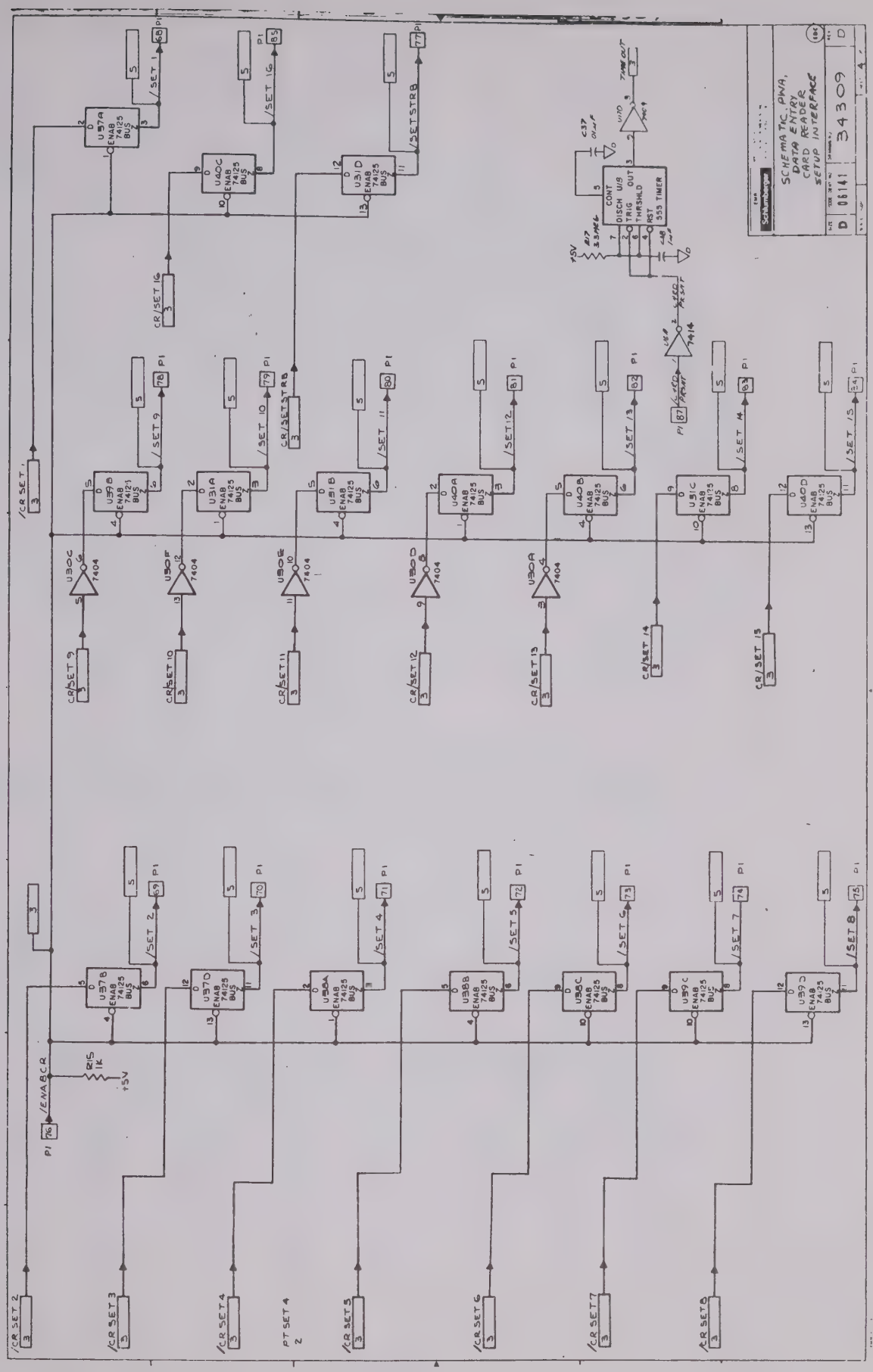
Schlumberger

SCHEM. P.I.A. DATA ENTRY

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	86141	84309	-

SCALE — — SHEET -- OF


SCHEMATIC PWA
DATA ENTRY
COMPUTER INTERFACE
SETUP CONTROL
34309


SCHEMATIC, PWA,
DATA ENTRY
CARD READER
SETUP INTERFACE
D 06141 34309 D
U37A ENAB 74125 BUS
U40C ENAB 74125 BUS
U31D ENAB 74125 BUS
U39B ENAB 74125 BUS
U31A ENAB 74125 BUS
U31B ENAB 74125 BUS
U40A ENAB 74125 BUS
U40B ENAB 74125 BUS
U31C ENAB 74125 BUS
U40D ENAB 74125 BUS
U37B ENAB 74125 BUS
U37D ENAB 74125 BUS
U38A ENAB 74125 BUS
U38B ENAB 74125 BUS
U38C ENAB 74125 BUS
U39C ENAB 74125 BUS
U39D ENAB 74125 BUS
U30C 7404
U30F 7404
U30E 7404
U30D 7404
U30A 7404
U37D 7404
U38A 7404
U38B 7404
U38C 7404
U39C 7404
U39D 7404
CONT
DISCH U18
TRIG OUT
THRSHLD
RST
555 TIMER
/CR SET 1
/CR SET 2
/CR SET 3
/CR SET 4
PT SET 4
/CR SET 5
/CR SET 6
/CR SET 7
/CR SET 8
/CR SET 9
/CR SET 10
/CR SET 11
/CR SET 12
/CR SET 13
/CR SET 14
/CR SET 15
/CR SET 16
/SET 1
/SET 2
/SET 3
/SET 4
/SET 5
/SET 6
/SET 7
/SET 8
/SET 9
/SET 10
/SET 11
/SET 12
/SET 13
/SET 14
/SET 15
/SET 16
/SET STRB
/ENABCR
R15 1K
+5V
P1

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO
1	DGND	1	TO PAPER TAPE READER PER [illegible]
2	ENABCOMP	5	FP/5
3	/CRDATA1	3	
4	/CRDATA2	3	
5	/CRDATA3	3	
6	/CRDATA4	3	
7	/CRDATA5	3	TO CALD READER VIA
8	/CRDATA6	3	AIJIB AS SHOWN ON
9	/CRDATA7	3	DIAGRAM 30136
10	/CRDATA8	3	
11	REQ B	6	
12	DATA TRANS	6	
13	INIT	6	
14			
15			
16	LSB06	6	8/4
17	SETDSP6	6	4/16
18	CMPD6	6	RP/J31PA12
19	LSB01	6	8/4
20	SETDSP1	6	4/16
21	CMPD1	6	RP/J31PA2
22	LSB02	6	8/4
23	SETDSP2	6	4/16
24	CMPD2	6	RP/J31PA4
25	CMPD8	6	RP/J31PC2
26	LSB03	6	8/4
27	SETDSP3	6	4/16
28	CMPD3	6	RP/J31PA6
29	LSB04	6	8/4
30	SETDSP4	6	4/16
31	CMPD4	6	RP/J31PA8
32	RSTCRDA	3	2/3
33	NVWL CLRTM	5	
34	/REV	5	
35	/STRB		2/3
36	EXT STRT	6	
37	FRATE FP	6	
38			
39			
40			
41			
42			
43	CMRSTSTRB	5	4/8
44	/ENCRPST	3	RP/J32PG10
45	/CRSTDLY	3	RP/J32PG12
46	INRQ IN	5	RP/J32PE10
47	LSB13	6	8/4
48	CMPD13	6	RP/J31PC12
49	LSB14	6	8/4
50	CMPD14	6	RP/J31PE2

P1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO
51	LSB09	6	8/4
52	CMPD9	6	RP/J31PC4
53	LSB10	6	8/4
54	CMPD10	6	RP/J31PC6
55	/ENABCOMP	5	FP/5
56	INRQ	5	RP/J30PB10
57	/SELSETUP	5	5/9, 5/21, 7/14, FP/4, 4/7
58	READSTORES	5	FP/4
59	EXTSTRT	6	RP/J31PB12
60	+5V	1	
61	DGND	1	
62	EXTSTRTSFR	6	9/7
63	XSTARTFR	6	8/24
64	XSTARTSFR	6	8/24
65	/EXTSTRTFR	6	8/7
66	D GND		
67			
68	/SET01	4	4/5
69	/SET02	4	4/5
70	/SET03	4	4/5
71	/SET04	4	4/5
72	/SET05	4	4/5
73	/SET06	4	4/5
74	/SET07	4	4/5
75	/SET08	4	4/5
76	/ENABCR	4	FP/5
77	/SETSTRB	4	4/5
78	/SET09	4	4/5
79	/SET10	4	4/5
80	/SET11	4	4/5
81	/SET12	4	4/5
82	/SET13	4	4/5
83	/SET14	4	4/5
84	/SET15	4	4/5
85	/SET16	4	4/5
86	/CRSTPGBF	3	TO CARD READER VIA AIJIB
87	/CARDPRSNT	3	AS SHOWN ON DIAGRAM 30136
88			
89			
90			
91			
92			
93			
94			
95	/PWRONRST	5	4/8
96	SETDSP5	6	4/16
97	CMPD5	6	RP/J31PA10
98	LSB05	6	8/4
99	SETDSP7	6	4/16
100	CMPD7	6	RP/J31PD13

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
101	LSB08	6	10/6
102	SETDSP8	6	4/16
103	LSB07	6	10/6
104	LSB15	6	8/4
105	CMPD15	6	RP/J31PE4
106	LSB16	6	8/4
107	CMPD16	6	RP/J31PE6
108	CMPD12	6	RP/J31PC10
109	LSB12	6	8/4
110	CMPD11	6	RP/J31PC8
111	LSB11	6	8/4
112	DOR7	5	RP/J30PC13
113	DOR8	5	RP/J30PC2
114	DOR9	5	RP/J30PC4
115	DOR13	5	RP/J30PC12
116	DOR14	5	RP/J30PE2
117	DOR15	5	RP/J30PE4
118	DOR1	5	RP/J30PA2
119	DOR2	5	RP/J30PA4
120	DOR3	5	RP/J30PA6
121	INSTR3	5	RP/J30PE8
122	DOR10	5	RP/J30PC6
123	DOR6	5	RP/J30PA12
124	DOR5	5	RP/J30PA10
125	+5V	1	
126	DGND	1	
127	DOR16	5	RP/J30PE6
128	DOR4	5	RP/J30PA8
129	DOR11	5	RP/J30PC8
130	DOR12	5	RP/J30PC10

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.

FOR ALL ELECTRICAL CROSS REF AS INDICATED IN NOTE 5 SEE ABOVE TABLE. ABBREVIATIONS USED FOR SOURCE AND DESTINATION DEFINITIONS ARE:

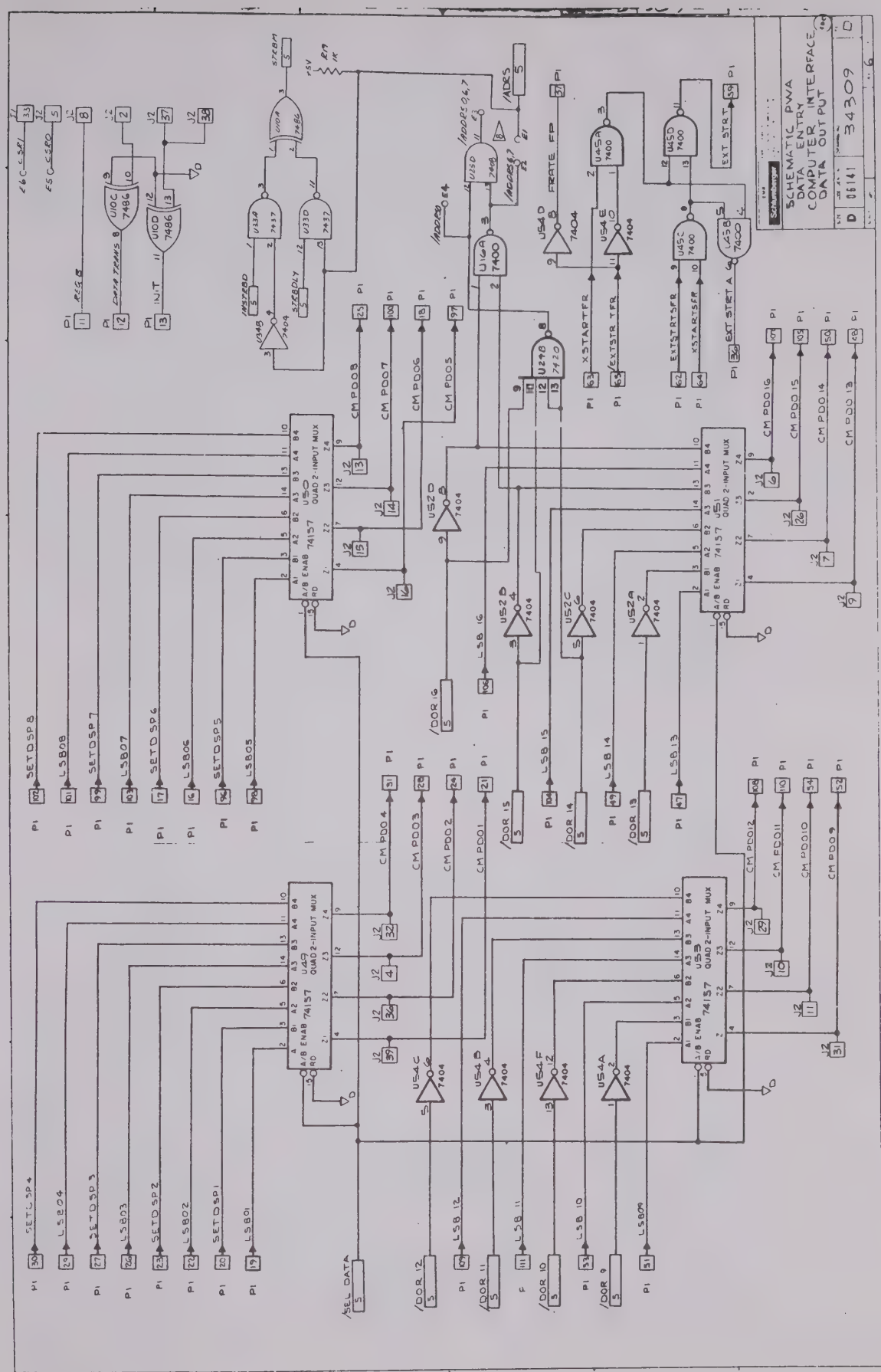
RP - INPUT OUTPUT TABLE 32938
FP - FRONT SUB-PANEL SCHEMATIC 28070
- WIRING DIAGRAM 32945

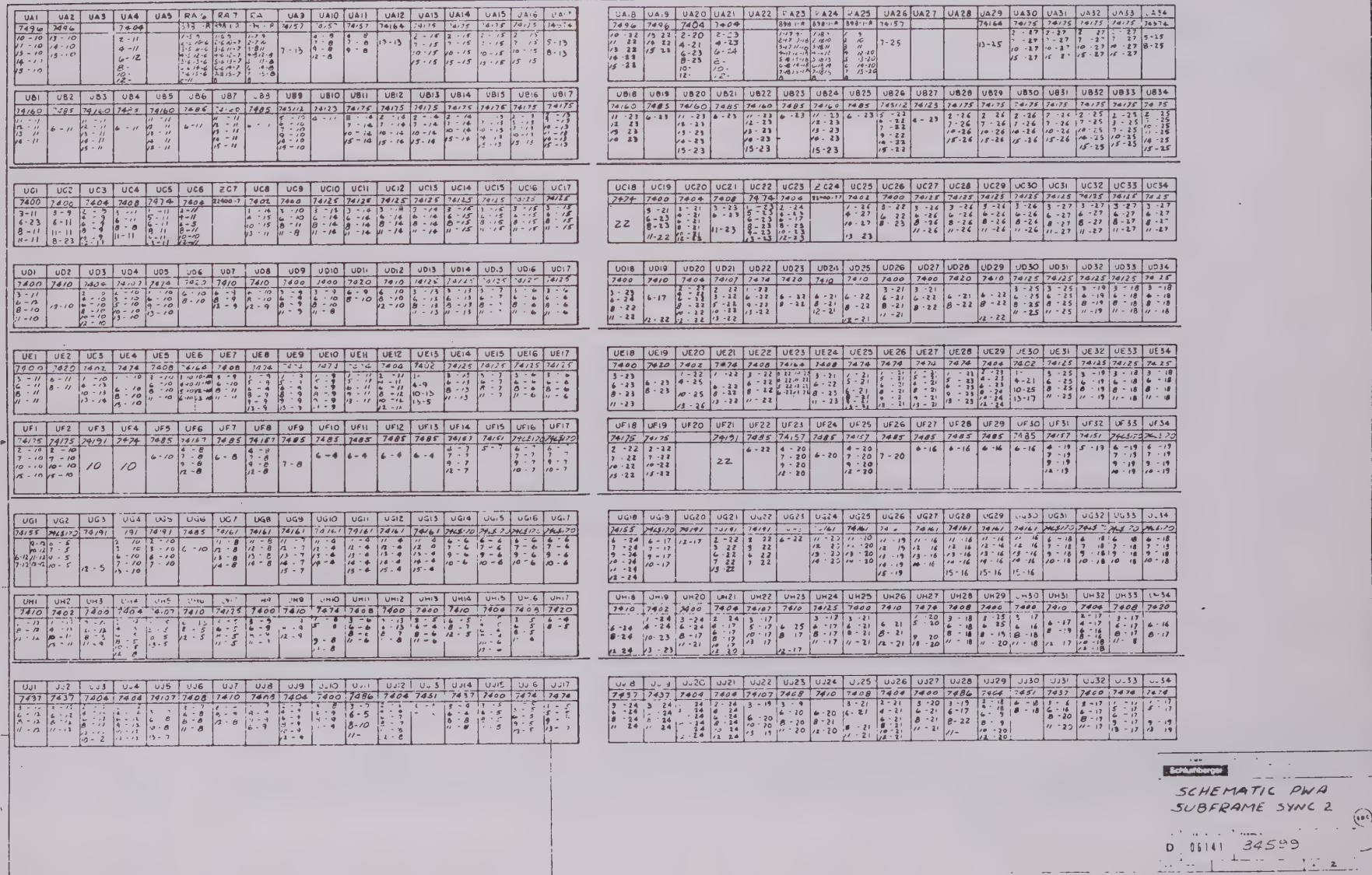
NOTES: CONTINUED

Schlumberger

SCHEMATIC, PWA,
DATA ENTRY
FUNCTION 10

SIZE	DRAWING NO	REV
D	05141	31309 C


SCHEMATIC PWA
DATA ENTRY
COMPUTER INTERFACE
DATA OUTPUT
34309
U50 QUAD 2-INPUT MUX
U51 QUAD 2-INPUT MUX
U49 QUAD 2-INPUT MUX
U53 QUAD 2-INPUT MUX
74157
ENAB
FRATE FP
XSTARTFR
EXTSTR TFR
EXTSTRTSFR
XSTARTSFR
EXT STRT A
EXT STRT
SEL DATA



SCHEMATIC PWA
SUBFRAME SYNC 2

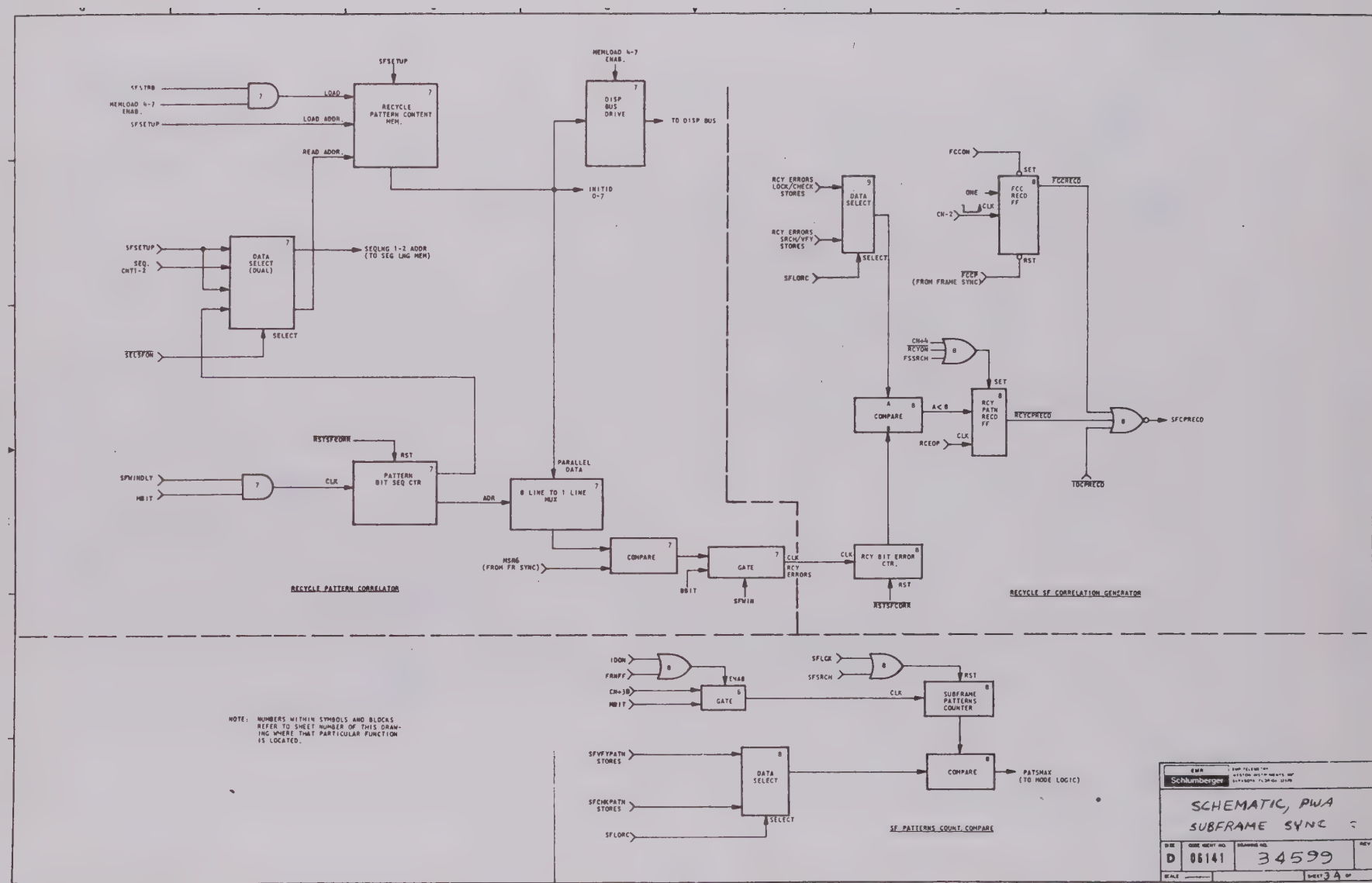
D 06141 34599

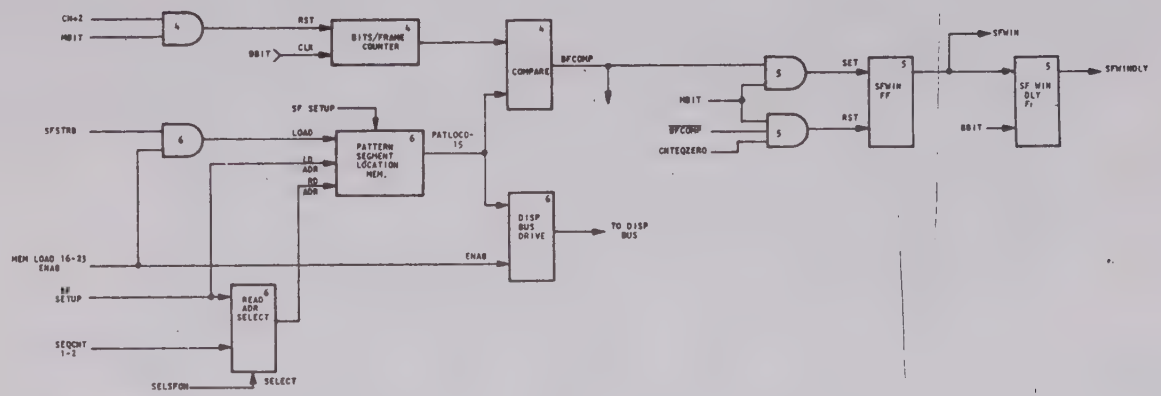
97-9

HOLE / COMPONENT CHART	
PART NO.	DESCRIPTION / ANALOG NUMBER
UA 34	UA 3-5, 21, 22, 27, 28
UB 34	
UC 34	
UD 34	
UE 34	
UF 34	UF20
UG 34	
UH 34	
UJ 34	
C136	
F2	

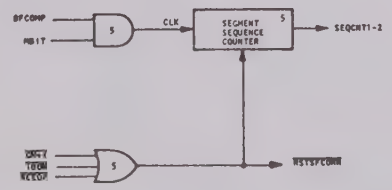
UNUSED CIRCUITS		
REF DES	TYPE	UNUSED CIRCUITS
UA20	7404	E, F
UC21	7408	C
UC23	7404	F
UC30	7400	D
UD19	7410	B
UD27	74 ..	D
UA2	7404	D, E, F
UA27	7404	D, E, F
UB27	74123	B
UT26	7486	D
UB40	74123	B
UD3	7410	C
UE13	7402	A
UC30	74OL	A
UJ11	7486	D
RA6	898-1-R	J
RA7	898-1-R	H, J
RA8	898-1-R	E, F, G, H, K, L
RA23	898-1-R	H, J
RA24	898-1-R	H, J
RA25	898-1-R	C, D, E, F, G, H, J, K, L

| POWER PINS | | |


SFSTRB
MEMLOAD 4-7 ENAB.
SFSETUP
LOAD
LOAD ADDR.
READ ADDR.
RECYCLE PATTERN CONTENT MEM.
MEMLOAD 4-7 ENAB.
DISP BUS DRIVE
TO DISP BUS
INITID 0-7
SFSETUP
SEQ. CNT1-2
DATA SELECT (DUAL)
SEQLNG 1-2 ADDR (TO SEG LNG MEM)
SELECT
SELSFON
RSTSFCORR
RST
SFWINDLY
MBIT
CLK
PATTERN BIT SEQ CTR
ADR
PARALLEL DATA
8 LINE TO 1 LINE MUX
MSR6 (FROM FR SYNC)
COMPARE
GATE
BBIT
SFWIN
CLK
RCY ERRORS
RCY BIT ERROR CTR.
RST
RSTSFCORR
RCY ERRORS LOCK/CHECK STORES
RCY ERRORS SRCH/VFY STORES
SFLORC
DATA SELECT
SELECT
FCCON
SET
ONE
CN-2
CLK
FCC RECD FF
RST
FCCP (FROM FRAME SYNC)
FCCRECD
CN+4
RCYON
FSSRCH
SET
COMPARE
A<B
RCY PATN RECD FF
RCEOP
CLK
RCYCPRECD
SFCPRECD
TDCPRECD
RECYCLE PATTERN CORRELATOR
RECYCLE SF CORRELATION GENERATOR
IDON
FRNFF
CN+3B
MBIT
ENAB
GATE
SFLCK
SFSRCH
RST
CLK
SUBFRAME PATTERNS COUNTER
SFVFYPATN STORES
SFCHKPATN STORES
SFLORC
DATA SELECT
SELECT
COMPARE
PATSMAX (TO MODE LOGIC)
SF PATTERNS COUNT, COMPARE
NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.
Schlumberger
SCHEMATIC, PWA
SUBFRAME SYNC
D
06141
34599
SHEET 3A OF

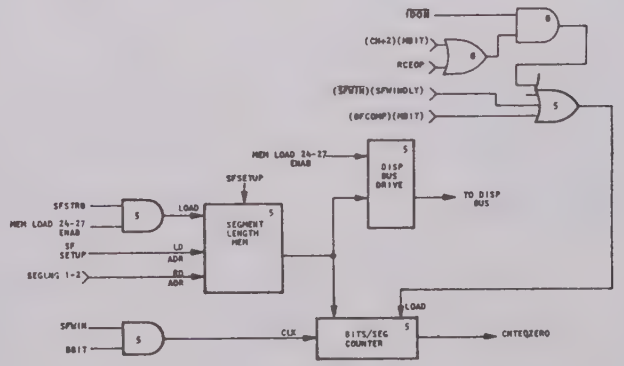


SF WINDOW GENERATION

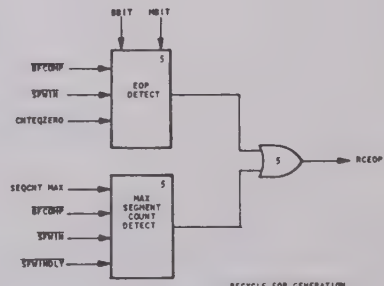


SEGMENT SEQUENCE COUNTER

NOTE: THE NUMBER IN THE UPPER RIGHT CORNER OF EACH BLOCK INDICATES THE LOGIC SHEET LOCATION OF THE FUNCTION FOR SF1. THE SHEET LOCATION OF THE LOGIC FOR SF2 - A SECOND, IDENTICAL SUB-FRAME CAN BE FOUND BY ADDING 12 TO THESE NUMBERS.



BITS/SEGMENT CONTROL



RECYCLE EOP GENERATION

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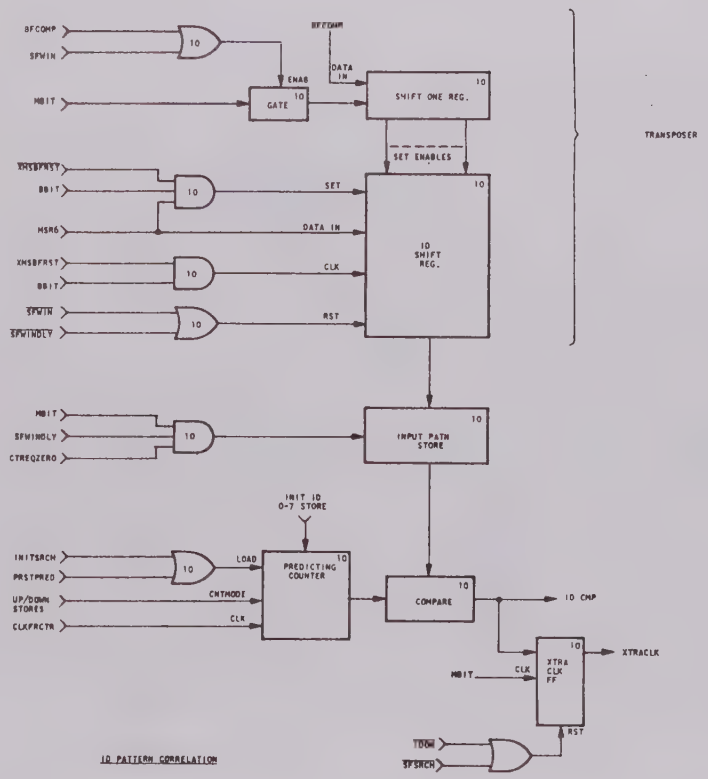
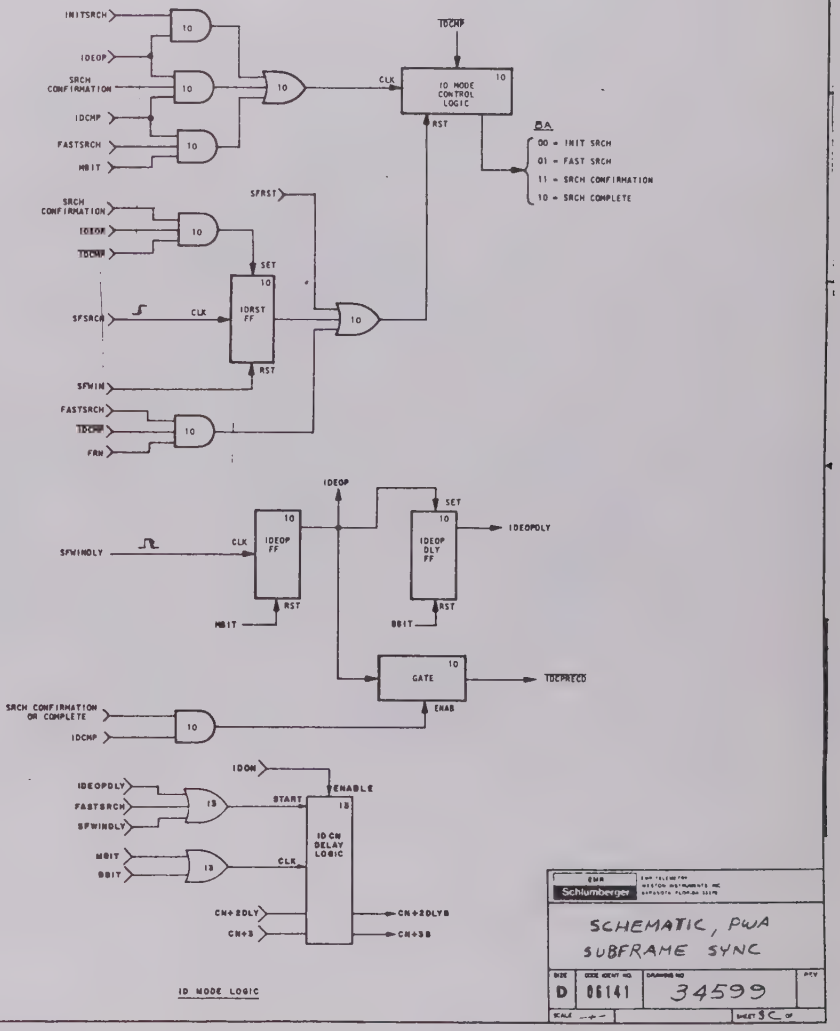
SCHEMATIC, PWA
SUBFRAME SYNC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	88141	34599	

SCALE —— SHEET 3 OF



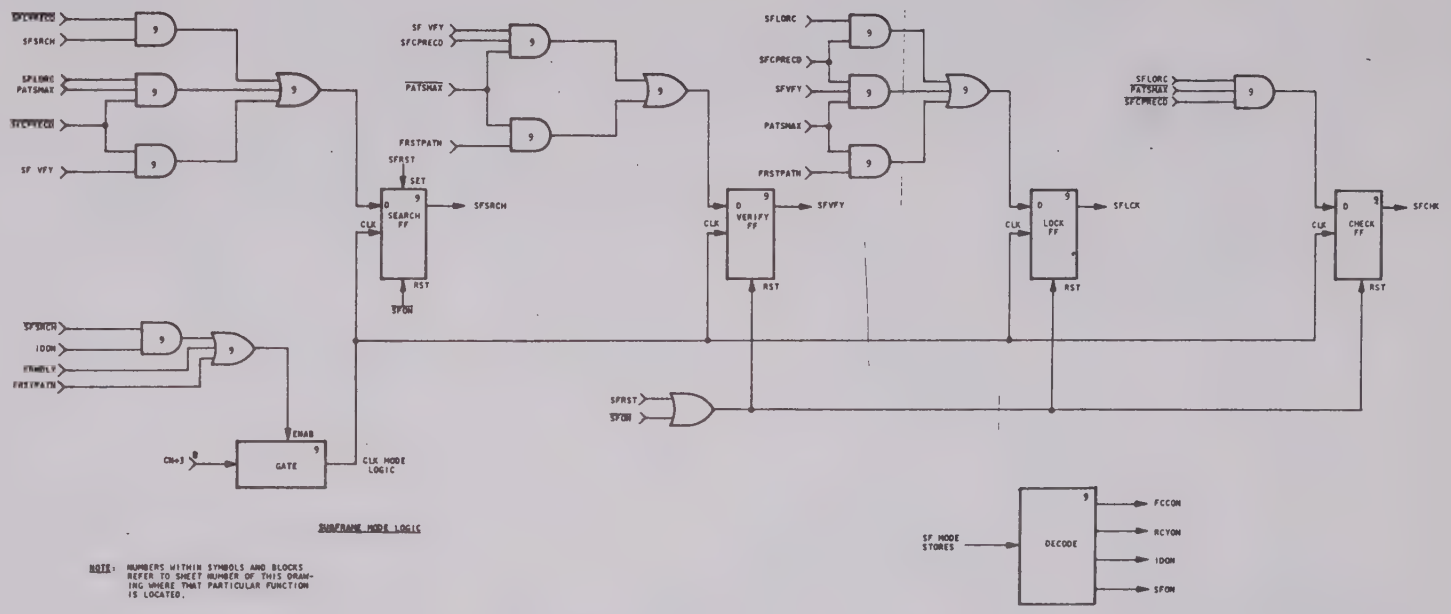


Schlumberger

SCHEMATIC, PWA
SUBFRAME SYNC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	06141	34599	

SCALE —/— SHEET 5C OF



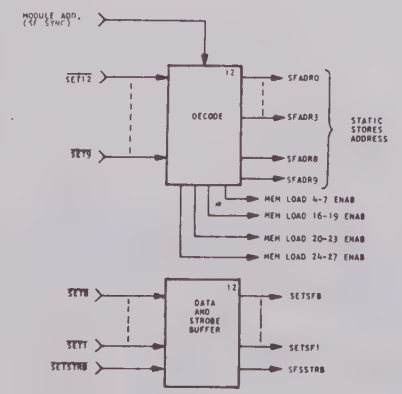
NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

Schlumberger

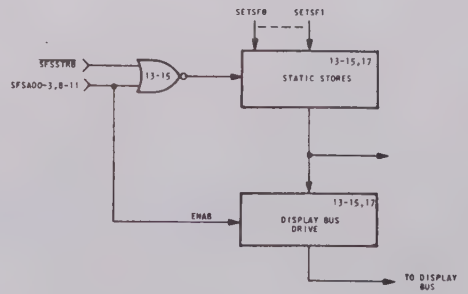
SCHEMATIC, PWA
SUBFRAME SYNC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	88141	34599	

SCALE —

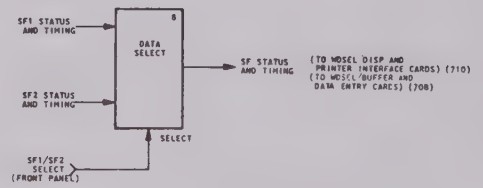


ADDRESS DECODE AND DATA BUFFER



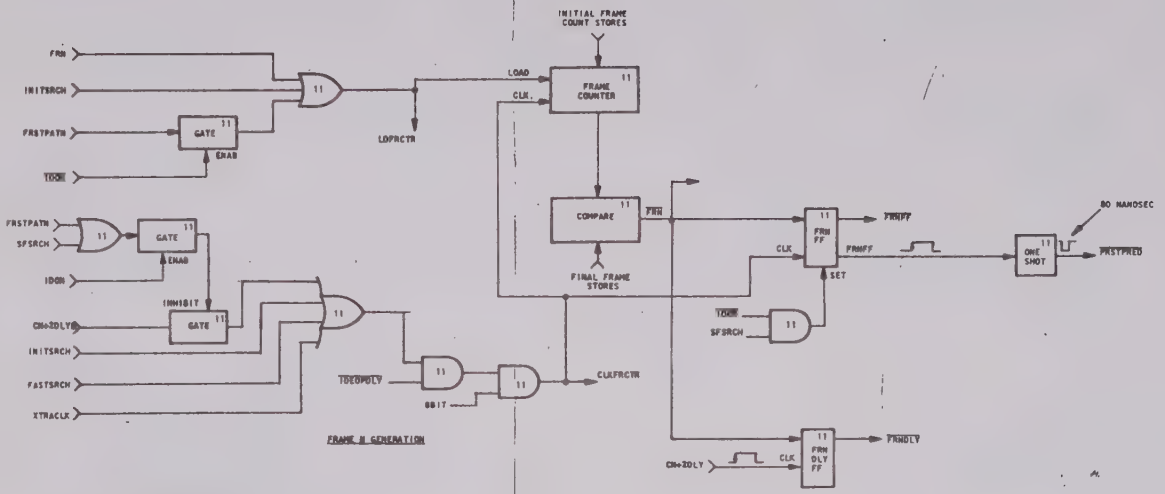
STATIC STORES

NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.



SF1/SF3 DISPLAY CONTROL SELECT

EMR Schlumberger			
SCHEMATIC, PWA SUBFRAME SYNC			
SIZE D	CODE IDENT NO 06141	DRAWING NO 34599	REV D



FRAME H GENERATION

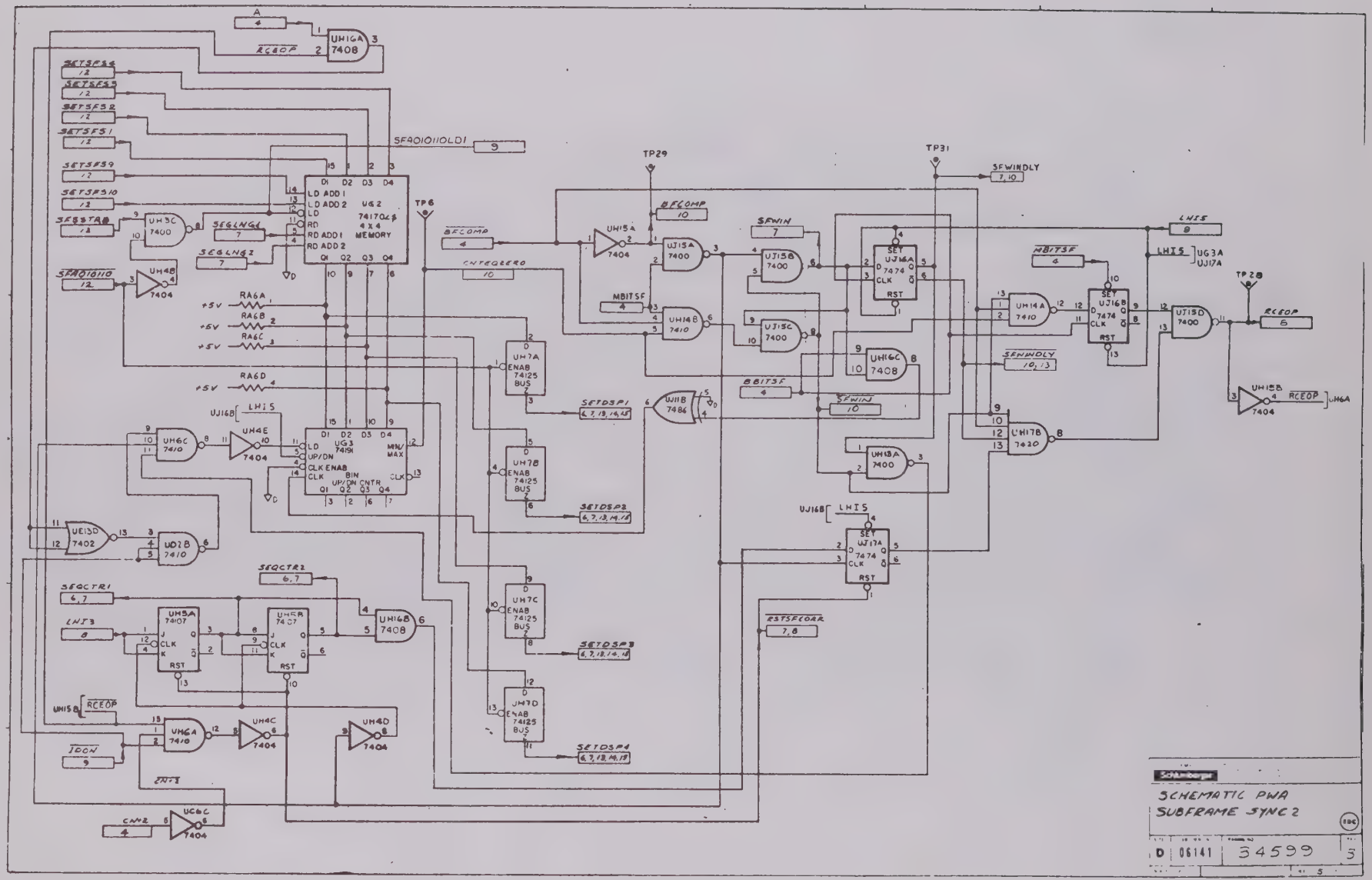
NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

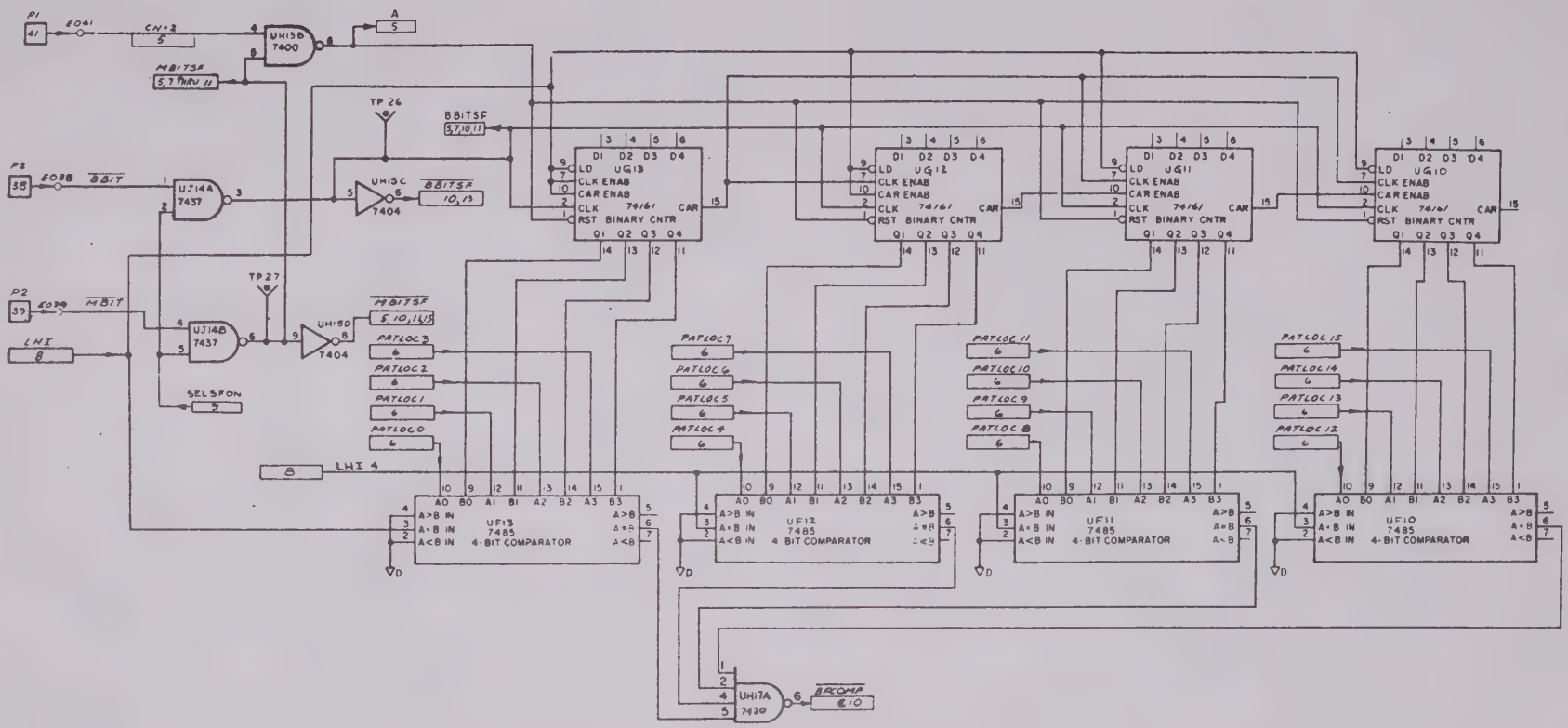
Schlumberger

SCHEMATIC, PWA
SUBFRAME SYNC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	86141	34539	

SCALE — SHEET 2 OF


SCHEMATIC PWA
SUBFRAME SYNC 2
D 06141 34599 3

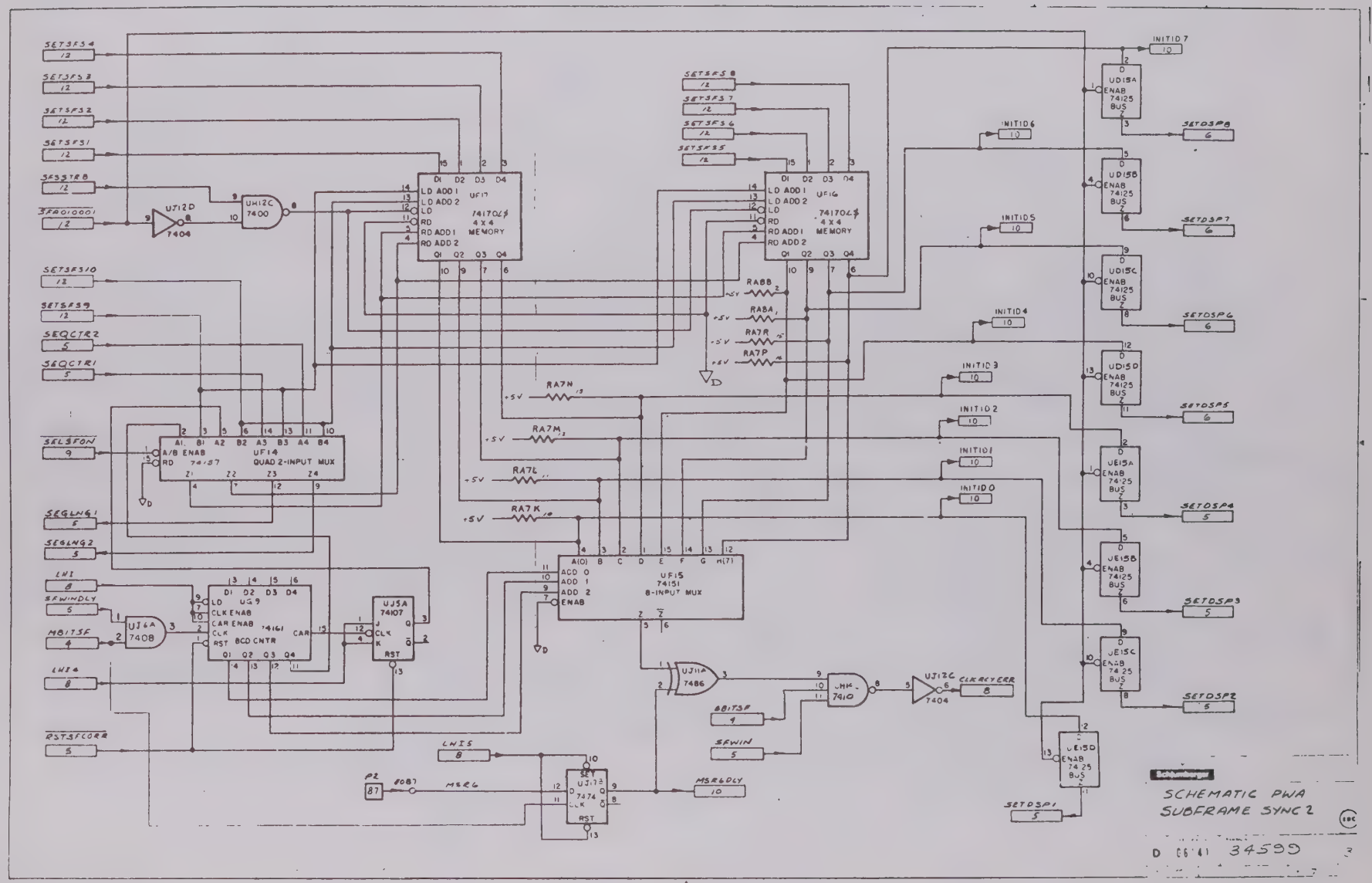


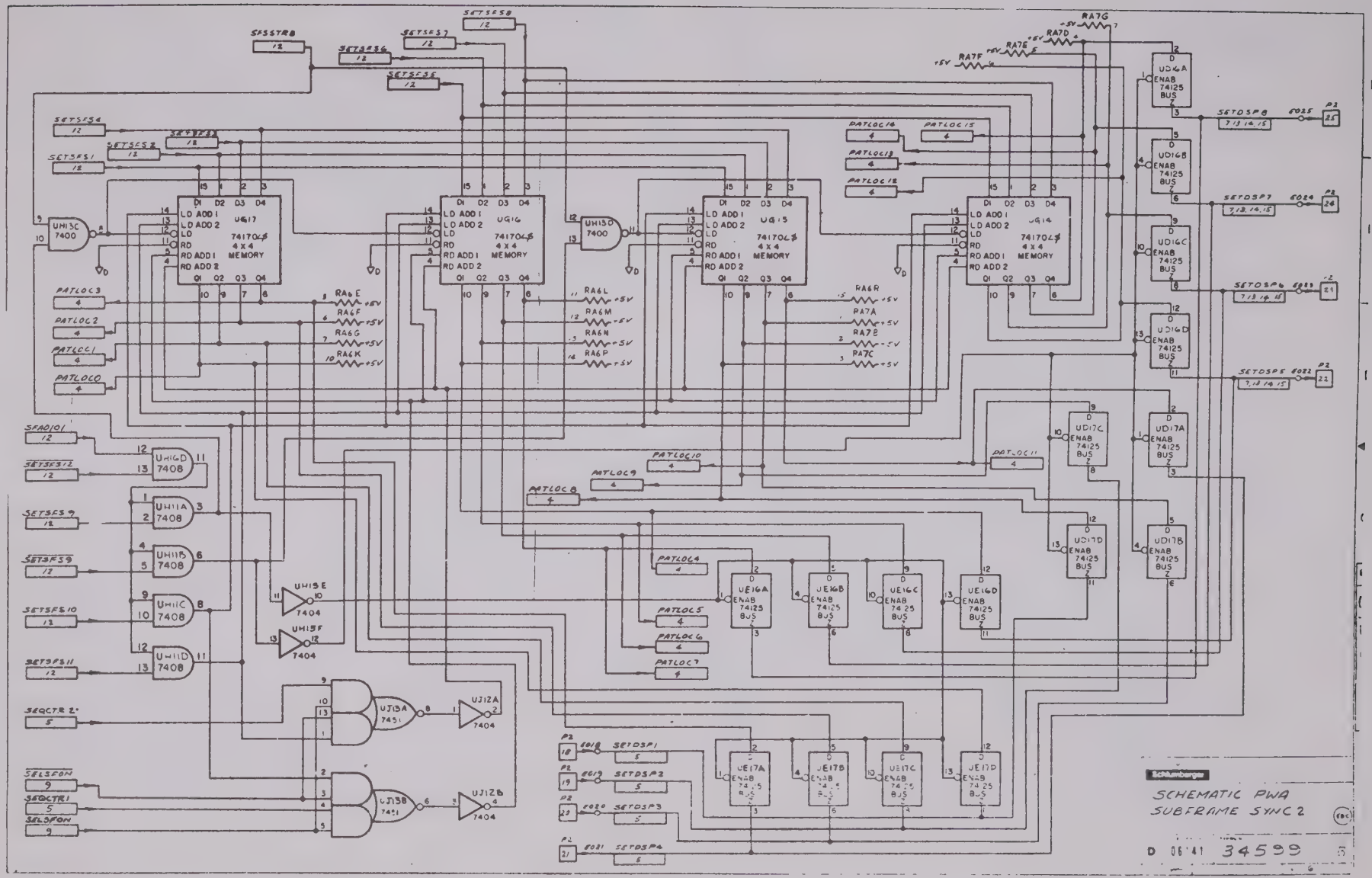
6-83

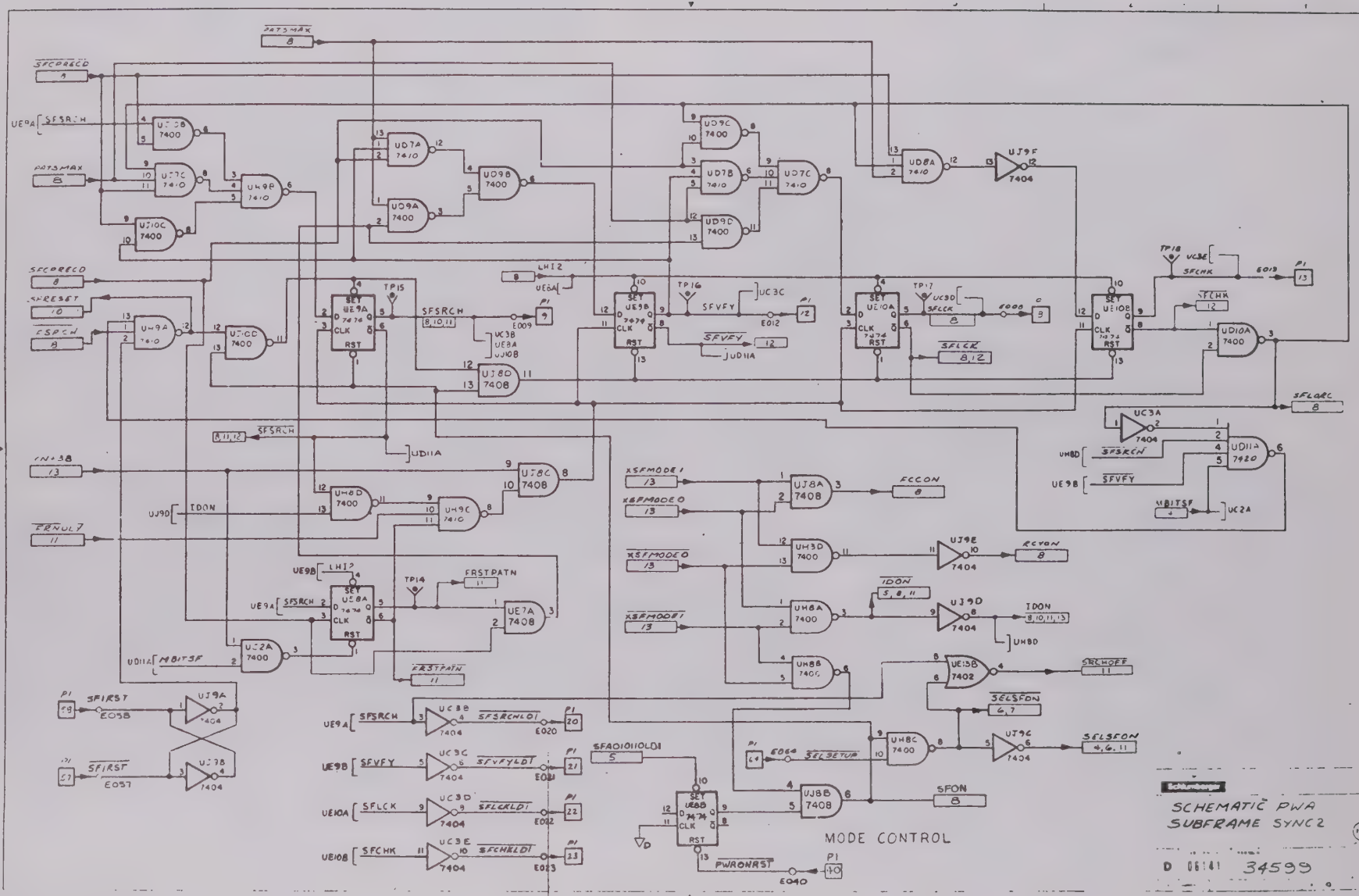
Schlumberger

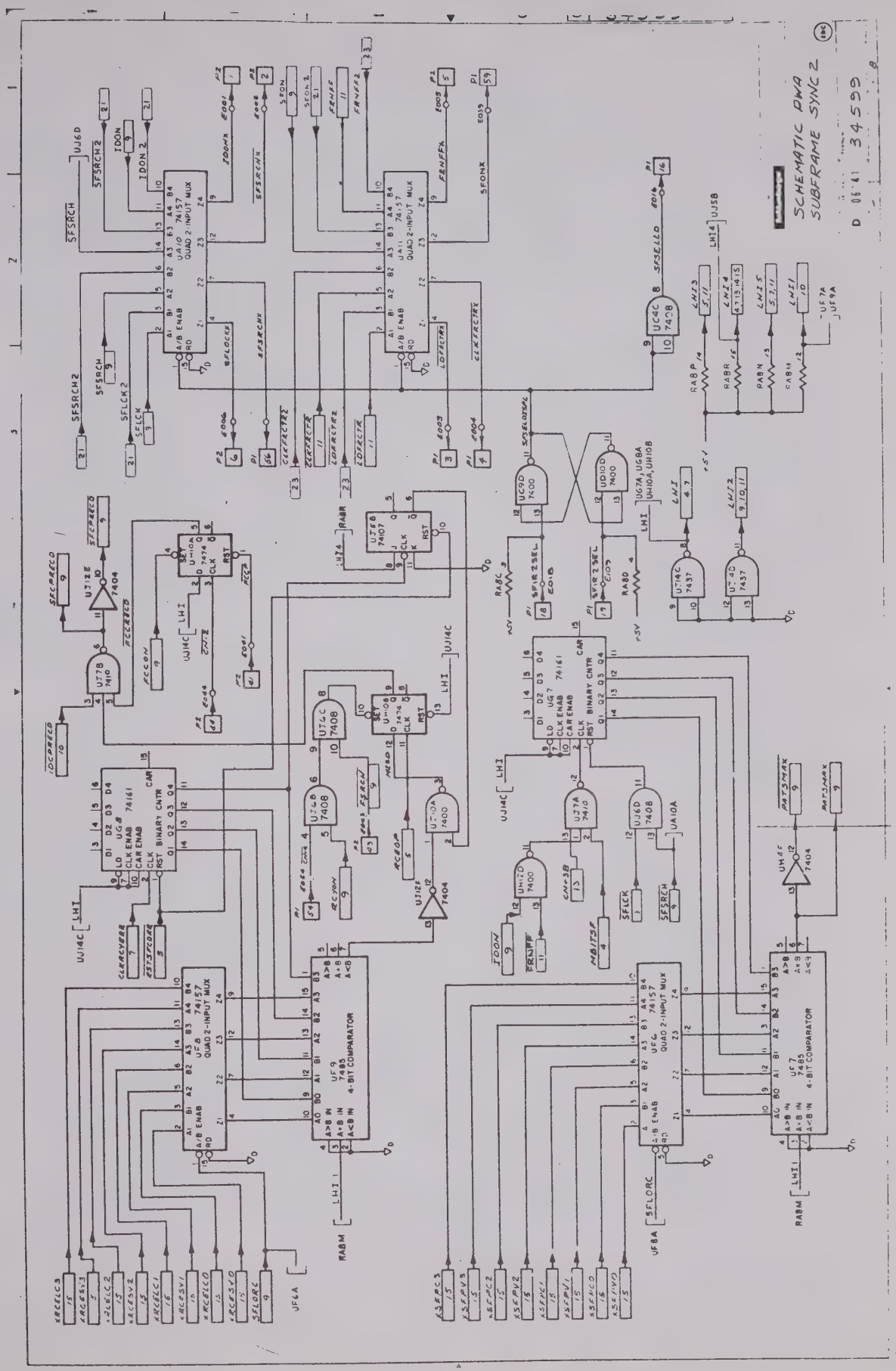
SCHEMATIC PWA
SUBFRAME SYNC 2

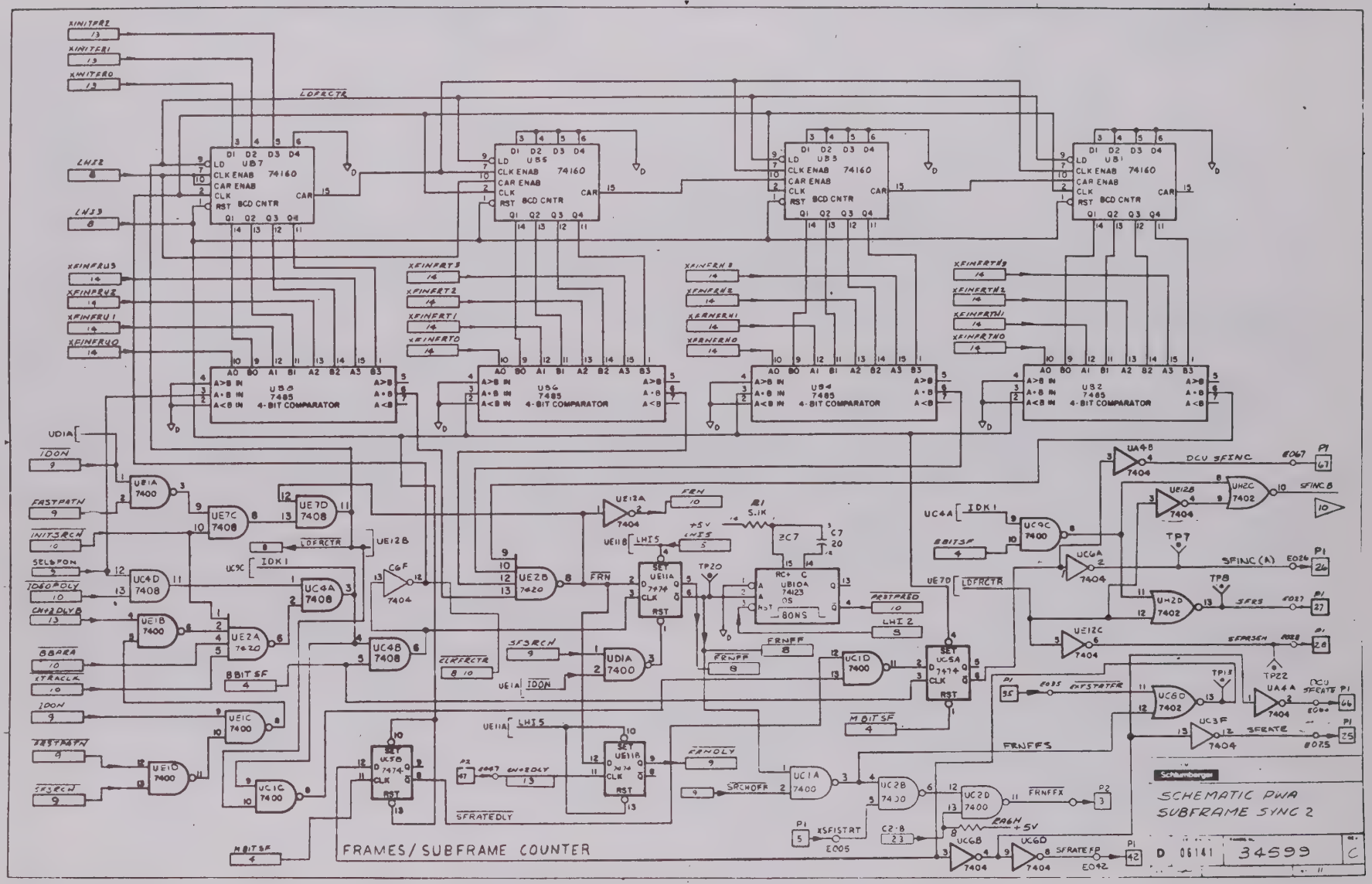
D 06141 34599

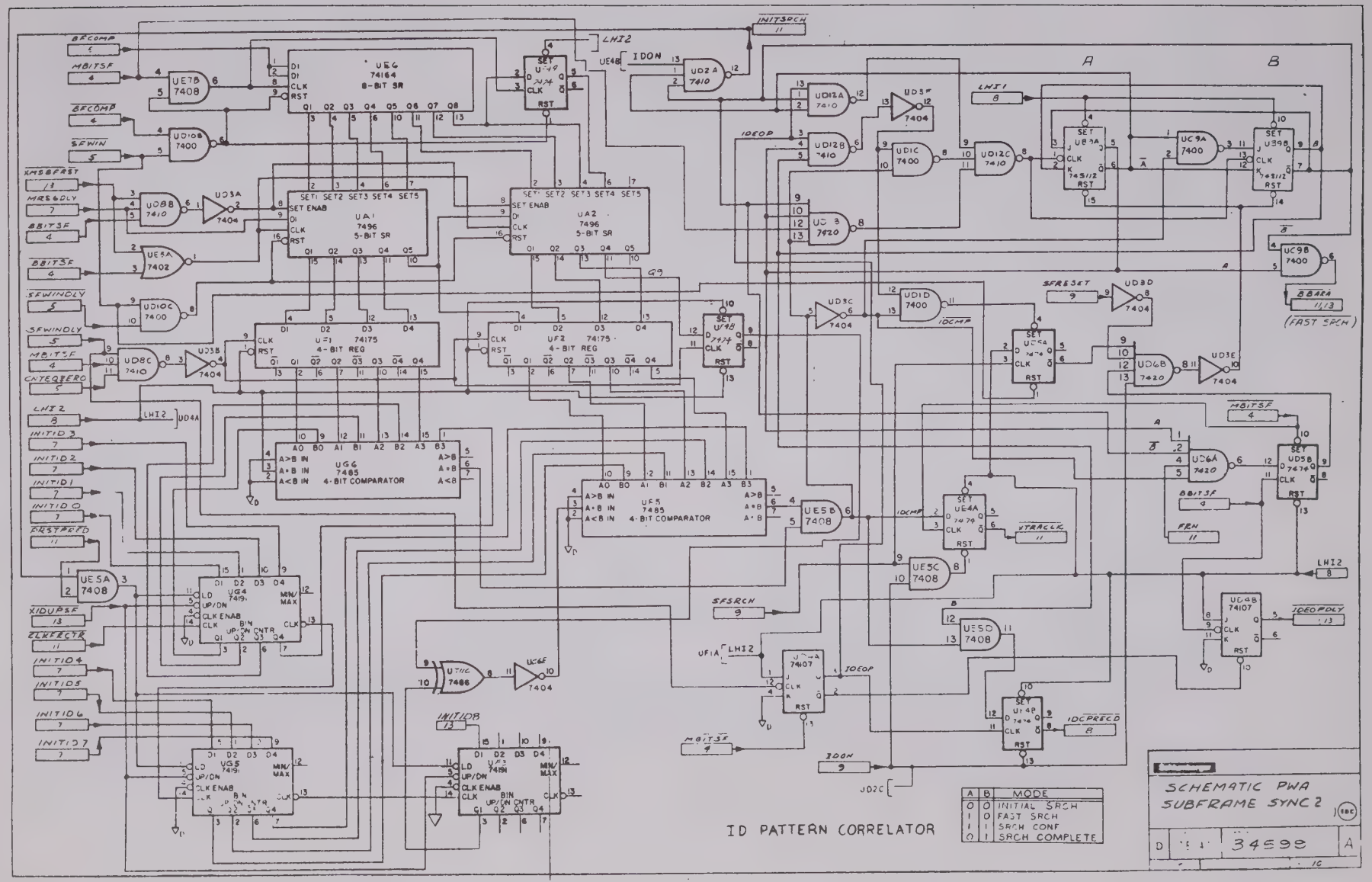

SCHEMATIC PWA
SUBFRAME SYNC 2
D 66141 34599

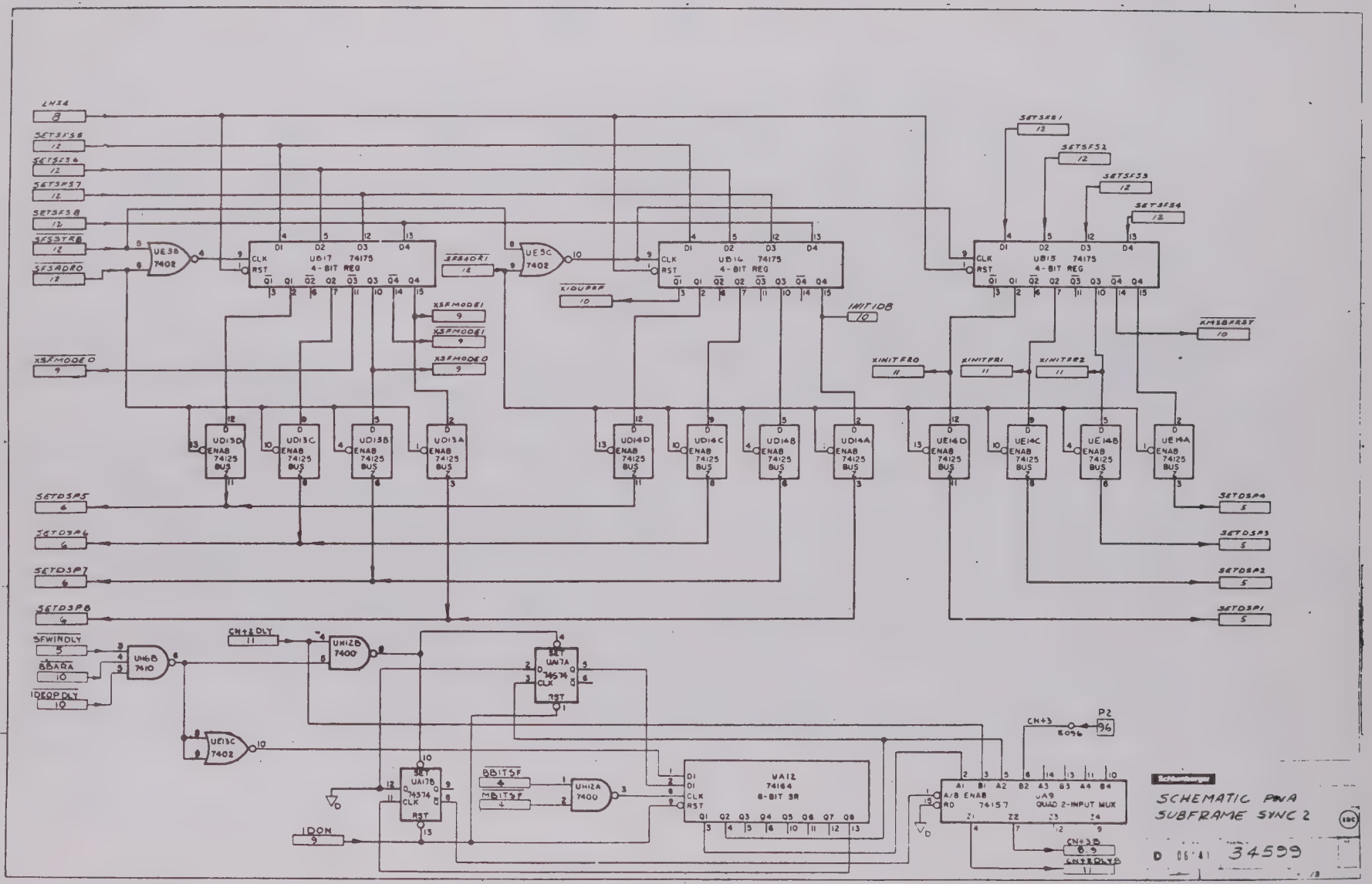

SCHEMATIC PWA
SUBFRAME SYNC 2
D 06141 34599

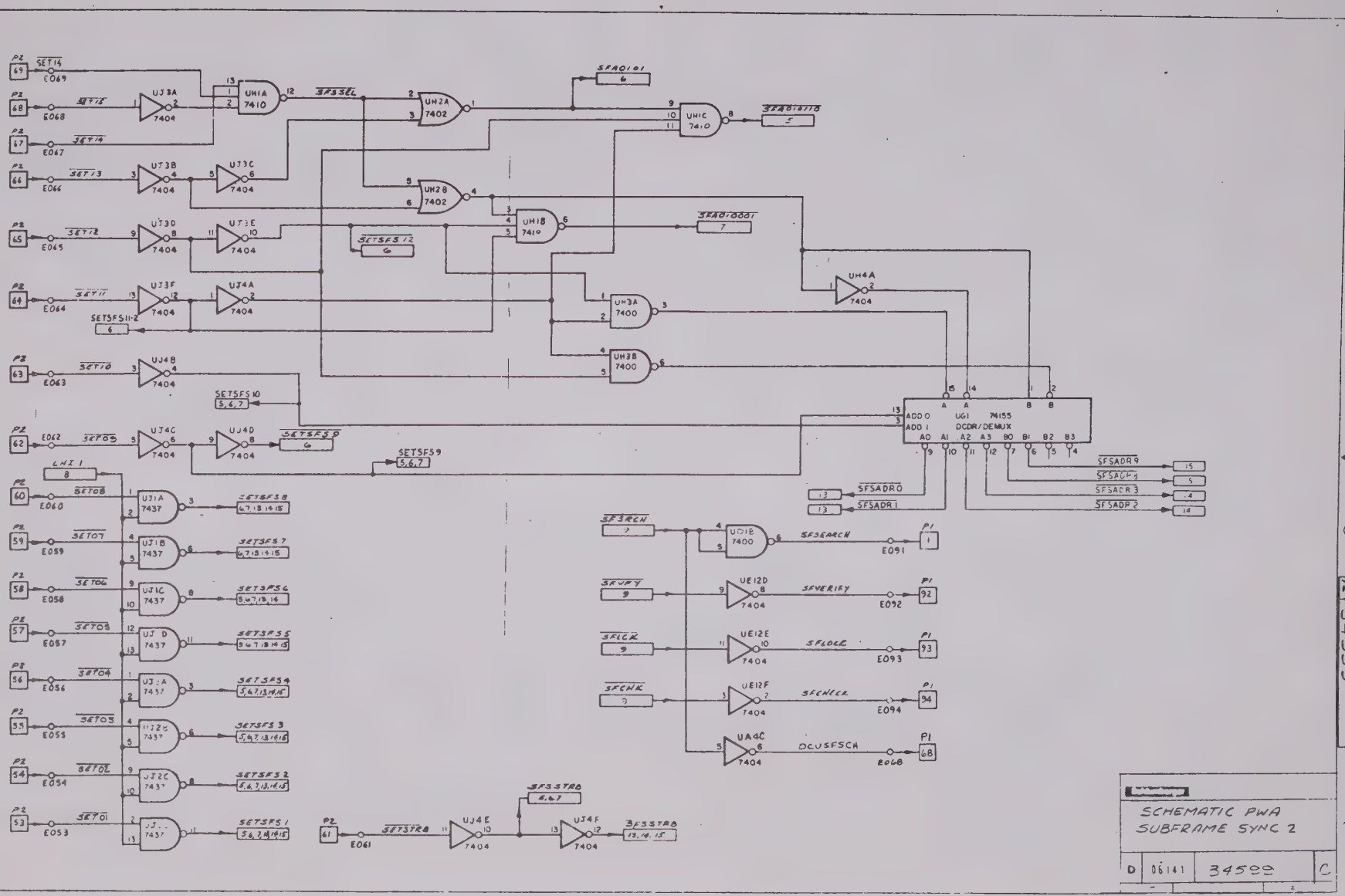

MODE CONTROL
SCHEMATIC PWA
SUBFRAME SYNC 2
D 06141 34599

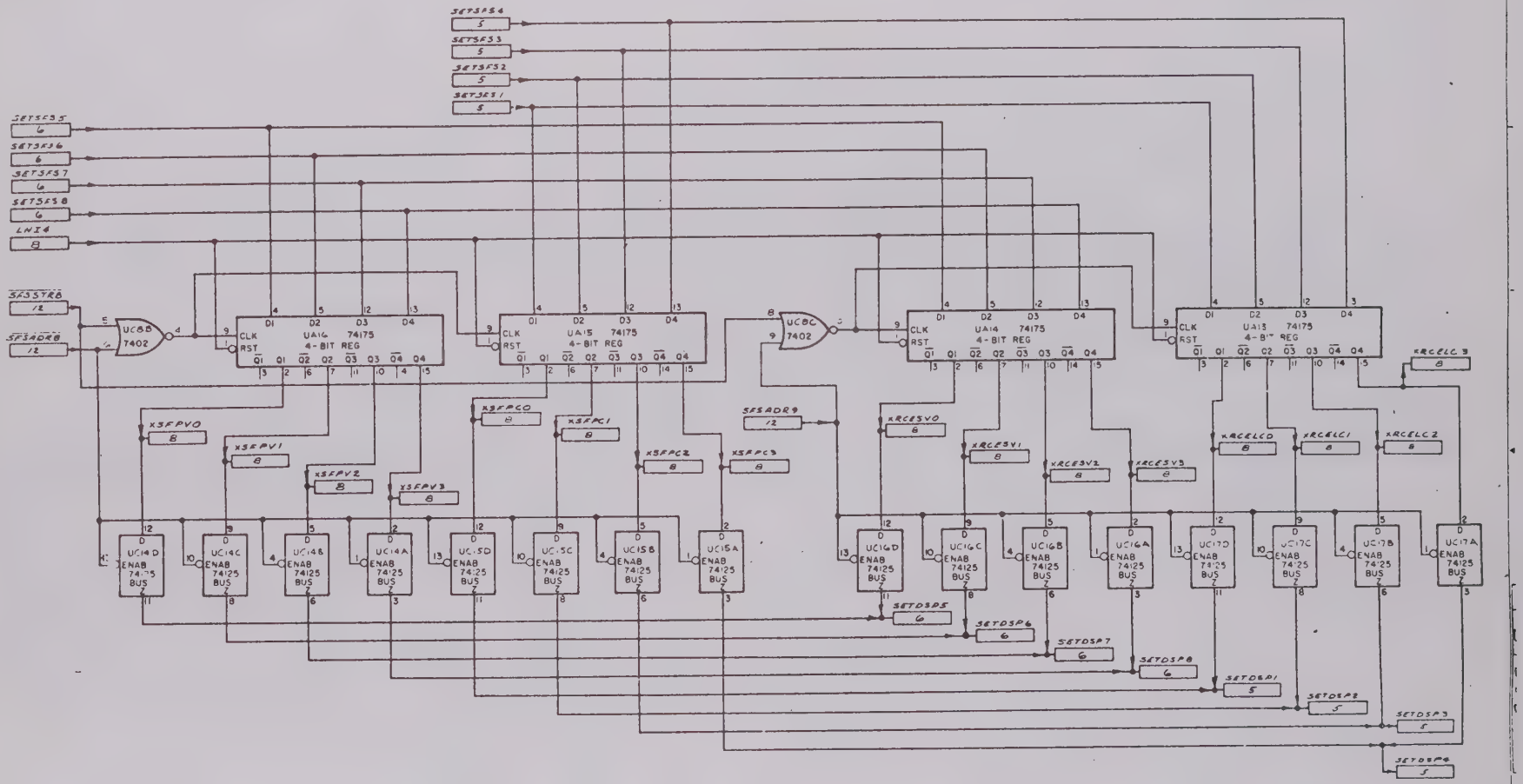

SCHEMATIC DWA
SUBFRAME SYNC 2
D 06 '41 34599


FRAMES/SUBFRAME COUNTER
SCHEMATIC PWA
SUBFRAME SYNC 2
Schlumberger
D 06141
34599
C
LDFRCTR
LHI2
LHI3
XINITPR2
XINITPR1
XINITPR0
XFINFRU3
XFINFRU2
XFINFRU1
XFINFRU0
XFINFRT3
XFINFRT2
XFINFRT1
XFINFRT0
XFINFRH3
XFINFRH2
XFINFRH1
XFINFRH0
XFINFRN3
XFINFRN2
XFINFRN1
XFINFRN0
U87 74160
U85 74160
U83 74160
U81 74160
U86 7485
U84 7485
U82 7485
4-BIT COMPARATOR
UDIA
IDON
FASTPATN
INITSRCH
SELBFON
IDSBPOLY
CH2DLYB
8BARA
STRACLR
SFSRCH
MBITSF
8BITSF
SFRATEDLY
FRNFFS
FRNFFX
SFINC(A)
DCU SFINC
DCU SFRATE
SFRATE
SFRATEFD
XSFISTART
EO05
EO42
EO67
EO27
EO26
EO35
EO36
EO75
+5V
S.1K
20
80NS


ID PATTERN CORRELATOR
SCHEMATIC PWA
SUBFRAME SYNC 2
34598
A
B
MODE
INITIAL SRCH
FAST SRCH
SRCH CONF
SRCH COMPLETE
(FAST SRCH)

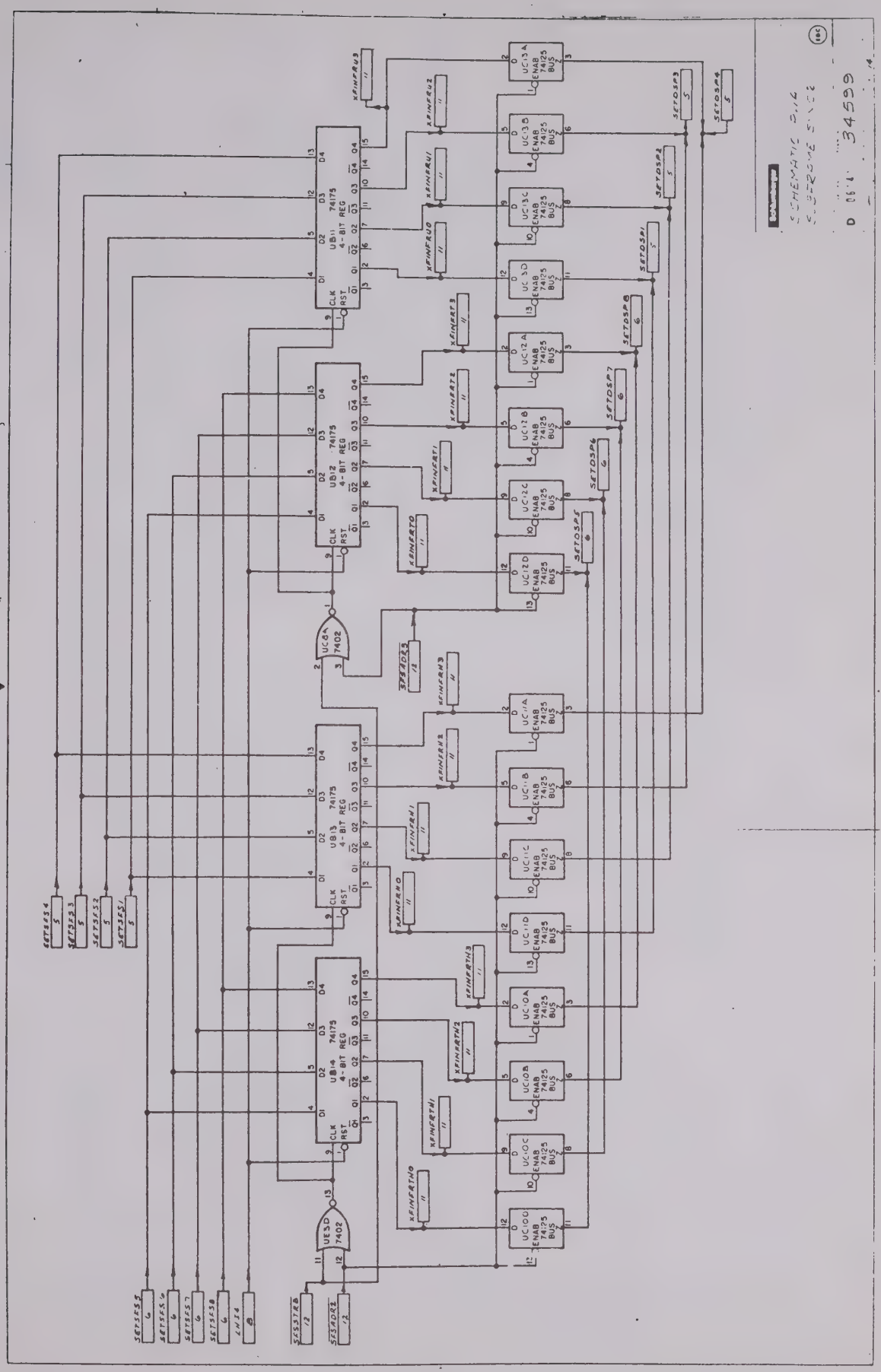

SCHEMATIC PWA
SUBFRAME SYNC 2
D 06 41 34599

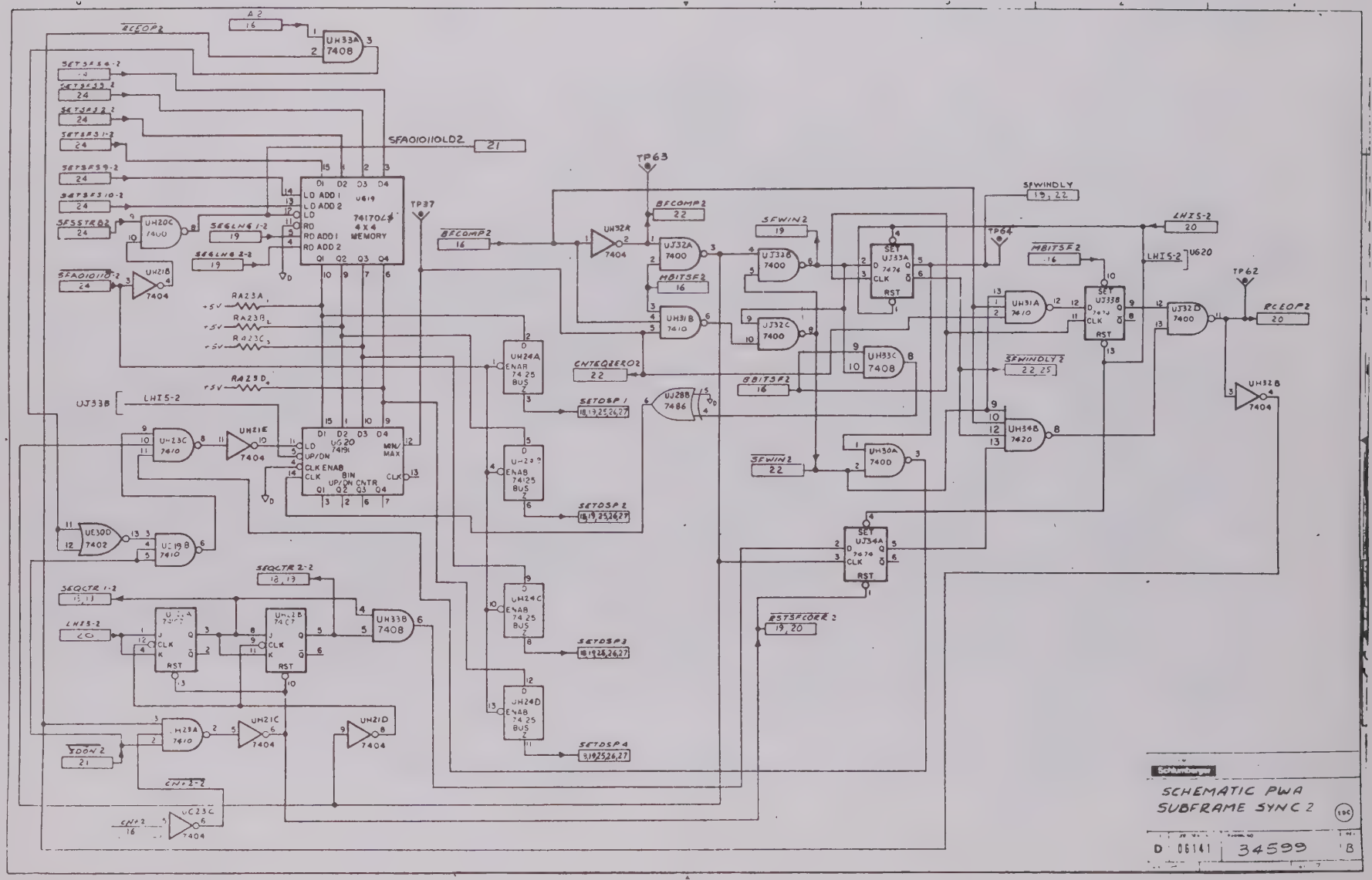

SCHEMATIC PWA
SUBFRAME SYNC 2
D
06141
34599
C

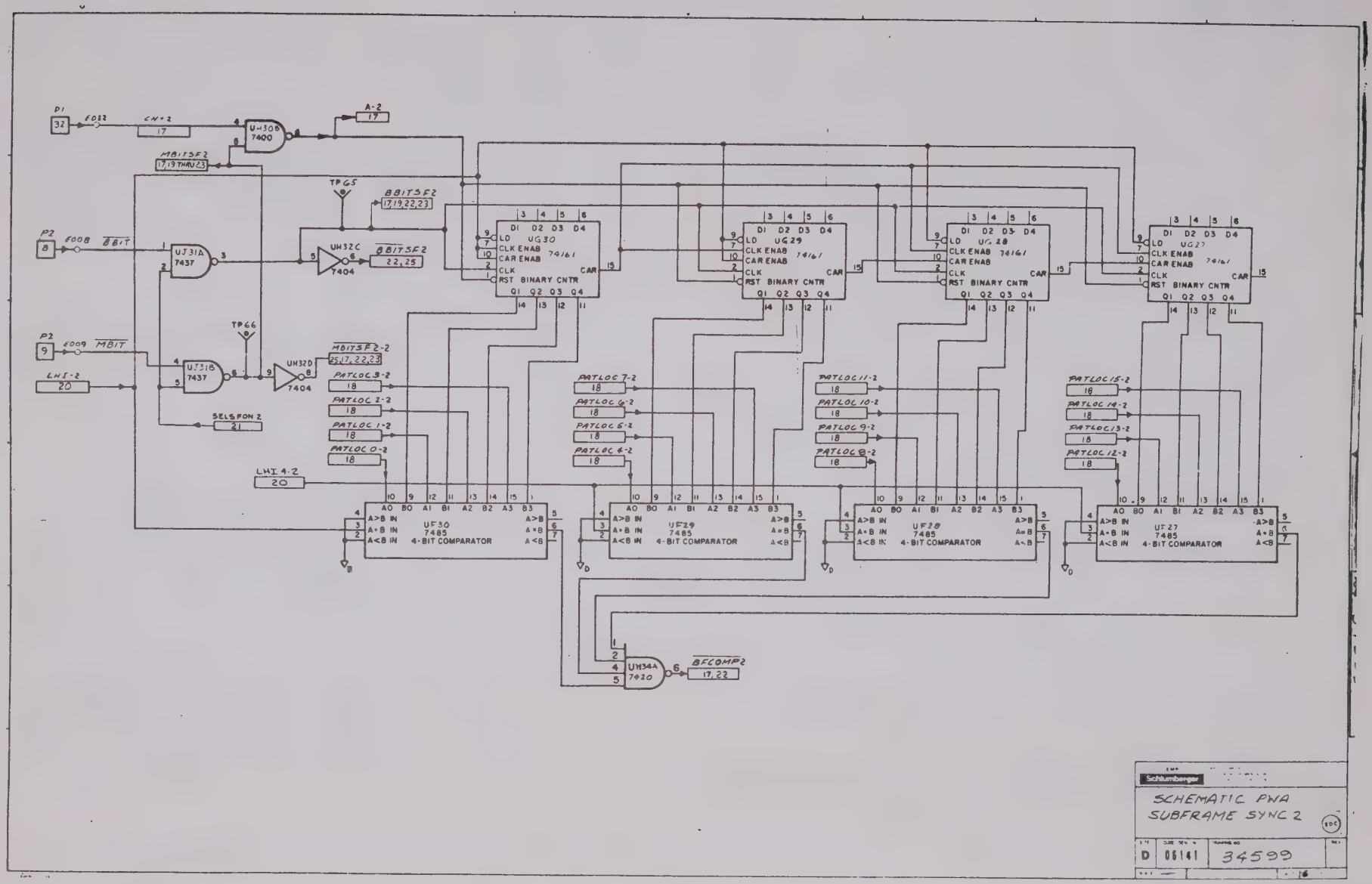


SCHEMATIC PWA
SUBFRAME SYNC 2

D 34599


SCHEMATIC DIA
SUBFRAME SYNC
D 34599
UB11 74175 4-BIT REG
UB12 74175 4-BIT REG
UB13 74175 4-BIT REG
UB14 74175 4-BIT REG
UC8A 7402
UE3D 7402
UC13A ENAB 74125 BUS
UC13B ENAB 74125 BUS
UC13C ENAB 74125 BUS
UC13D ENAB 74125 BUS
UC12A ENAB 74125 BUS
UC12B ENAB 74125 BUS
UC12C ENAB 74125 BUS
UC12D ENAB 74125 BUS
UC11A ENAB 74125 BUS
UC11B ENAB 74125 BUS
UC11C ENAB 74125 BUS
UC11D ENAB 74125 BUS
UC10A ENAB 74125 BUS
UC10B ENAB 74125 BUS
UC10C ENAB 74125 BUS
UC10D ENAB 74125 BUS
XFINFRU3
XFINFRU2
XFINFRU1
XFINFRU0
XFINFRT3
XFINFRT2
XFINFRT1
XFINFRT0
XFINFRH3
XFINFRH2
XFINFRH1
XFINFRH0
XFINFRTH3
XFINFRTH2
XFINFRTH1
XFINFRTH0
SETDSP1
SETDSP2
SETDSP3
SETDSP4
SETDSP5
SETDSP6
SETDSP7
SETDSP8
SETSFS1
SETSFS2
SETSFS3
SETSFS4
SETSFS5
SETSFS6
SETSFS7
SETSFS8
LNI4
SFSADR2
SFSADR3
SFSSTRB


SCHEMATIC PWA
SUBFRAME SYNC 2
D 06141
34599
B


P1
32
EO32
CN+2
17
U-30B
7400
A-2
17
MBITSF2
17,19 THRU 23
BBITSF2
17,19,22,23
TP65
P2
8
EO08
BBIT
UJ31A
7437
UH32C
7404
BBITSF2
22,25
UG30
UG29
UG28
UG27
74161
D1 D2 D3 D4
LD
CLK ENAB
CAR ENAB
CLK
RST
BINARY CNTR
Q1 Q2 Q3 Q4
CAR
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EO09
MBIT
UJ31B
7437
UH32D
7404
MBITSF2-2
25,17,22,23
LHI-2
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SELSFON 2
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PATLOC 14-2
PATLOC 13-2
PATLOC 12-2
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LHI 4-2
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A=B IN
A<B IN
A>B
A=B
A<B
UF30
UF29
UF28
UF27
7485
4-BIT COMPARATOR
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17,22
Schlumberger
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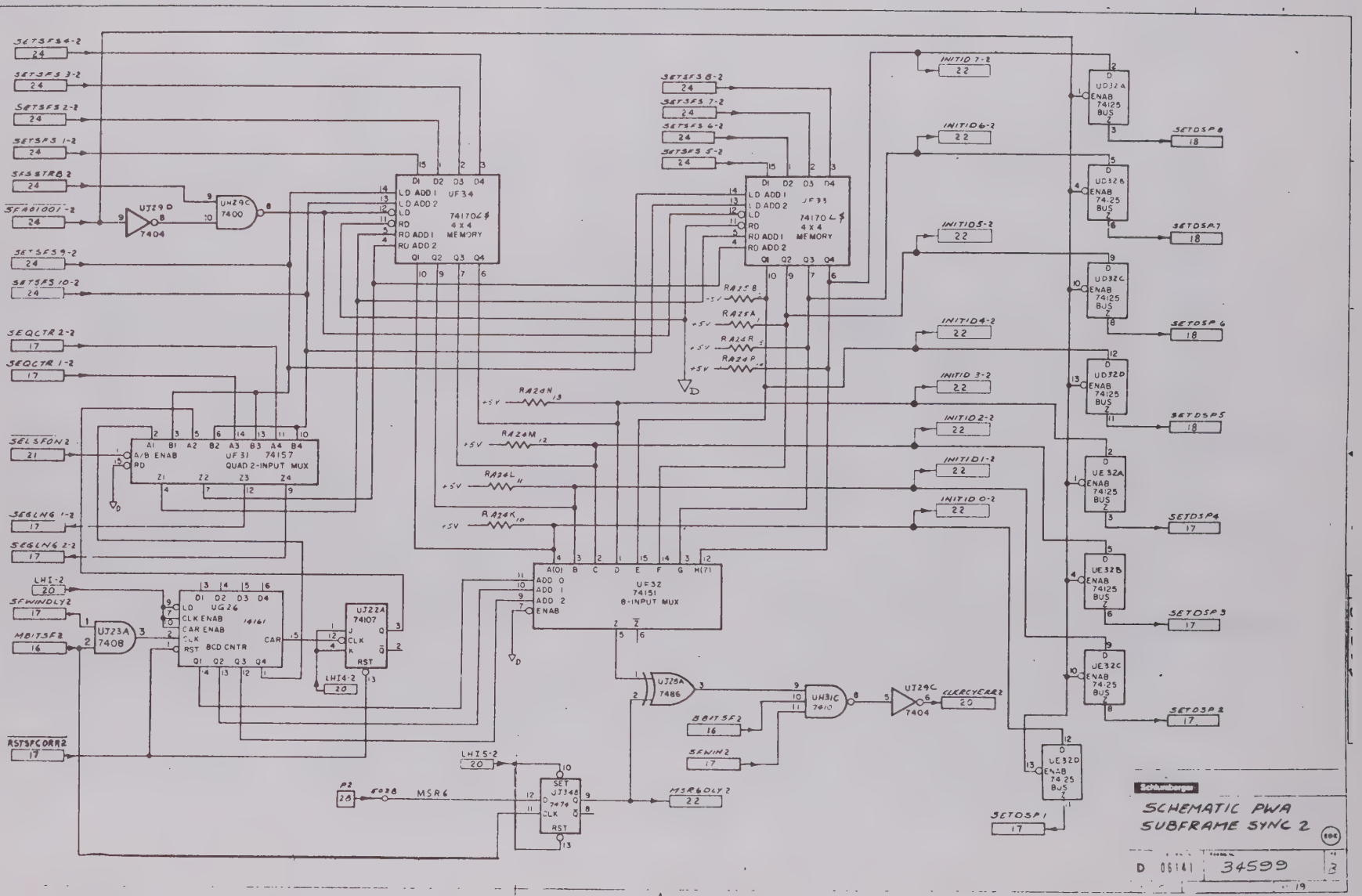
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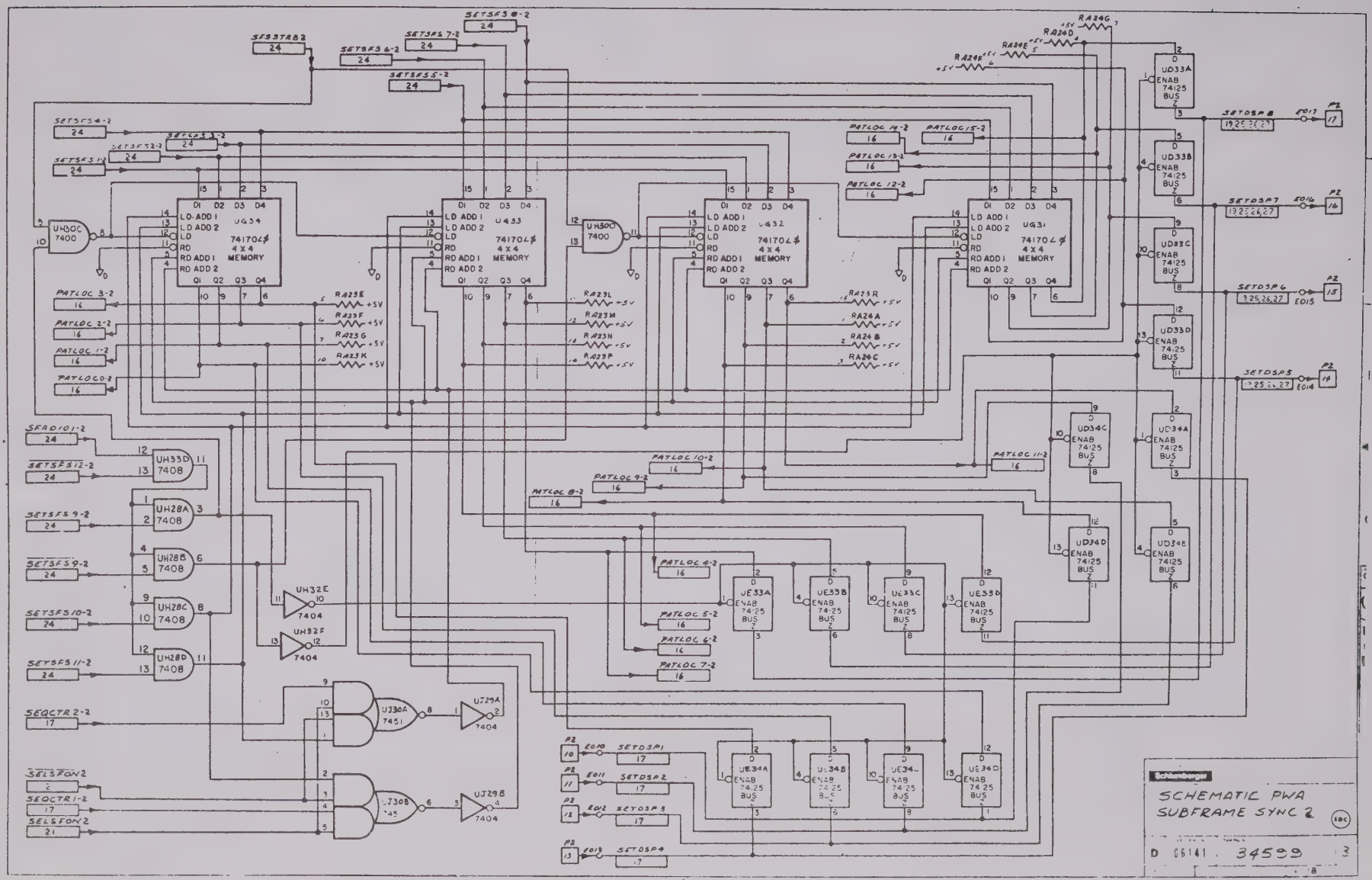
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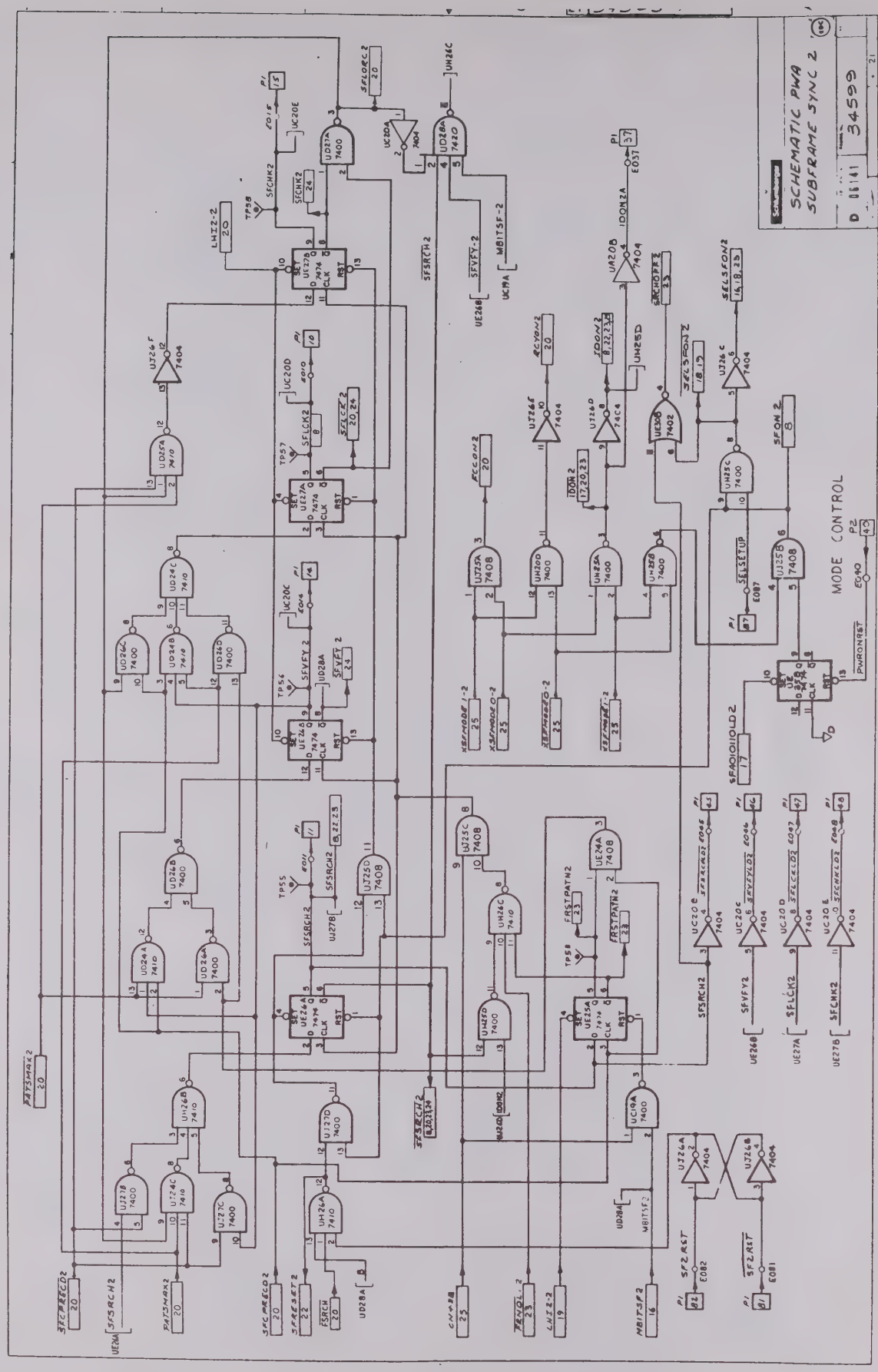
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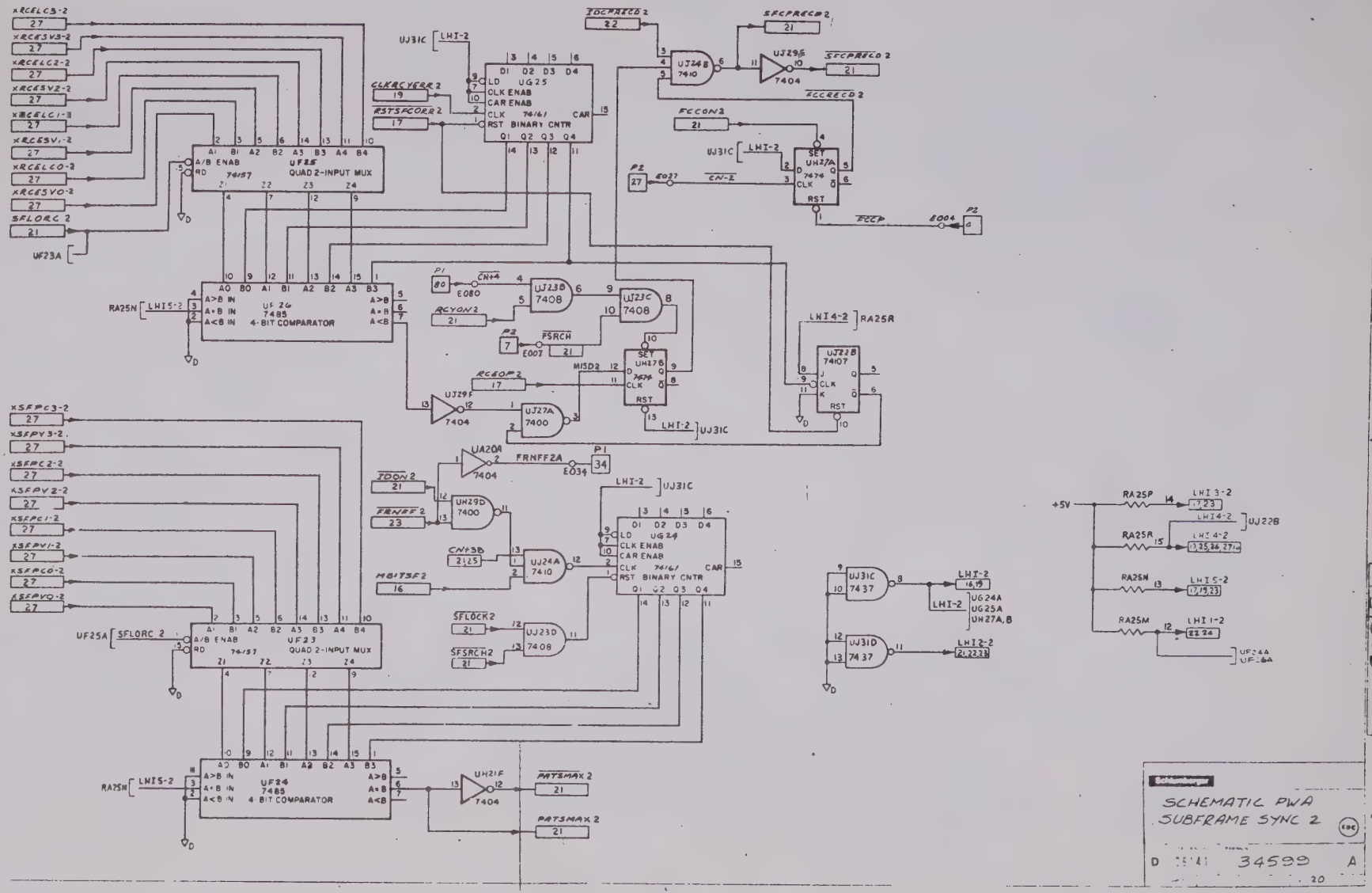
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UF26 7485 4-BIT COMPARATOR
UF23 QUAD 2-INPUT MUX
UF24 7485 4-BIT COMPARATOR
UG25 74161 BINARY CNTR
UG24 74161 BINARY CNTR
UH27A 7474
UH27B 7474
UJ22B 74107
UJ23B 7408
UJ23C 7408
UJ23D 7408
UJ24A 7410
UJ24B 7410
UJ29E 7404
UJ29F 7404
UJ27A 7400
UJ29D 7400
UJ31C 7437
UJ31D 7437
UA20A 7404
UH21F 7404
+5V
RA25P
RA25R
RA25N
RA25M
LHI 3-2
LHI 4-2
LHI 5-2
LHI 1-2
LHI 2-2
UJ22B
UF24A
UF26A
UF23A
UF25A
SFLORC 2
SFLOCK2
SFSRCH2
PATSMAX 2
MBITSF2
CN+3B
FRNFF 2
IDON 2
FRNFF2A
RCEOP 2
MISD2
RCYON 2
FSRCH
CN+4
CLKRCYERR 2
RSTSFCORR 2
IDCPRECD 2
SFCPRECD 2
FCCRECD 2
FCCON 2
CN-2
FCCP
E027
E004
E080
E007
E034
P1
P2
UJ31C
LHI-2
LHI4-2
RA25R
RA25N
LHI5-2
XRCELC3-2
XRCESV3-2
XRCELC2-2
XRCESV2-2
XRCELC1-2
XRCESV1-2
XRCELC0-2
XRCESV0-2
XSFPC3-2
XSFPV3-2
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XSFPV1-2
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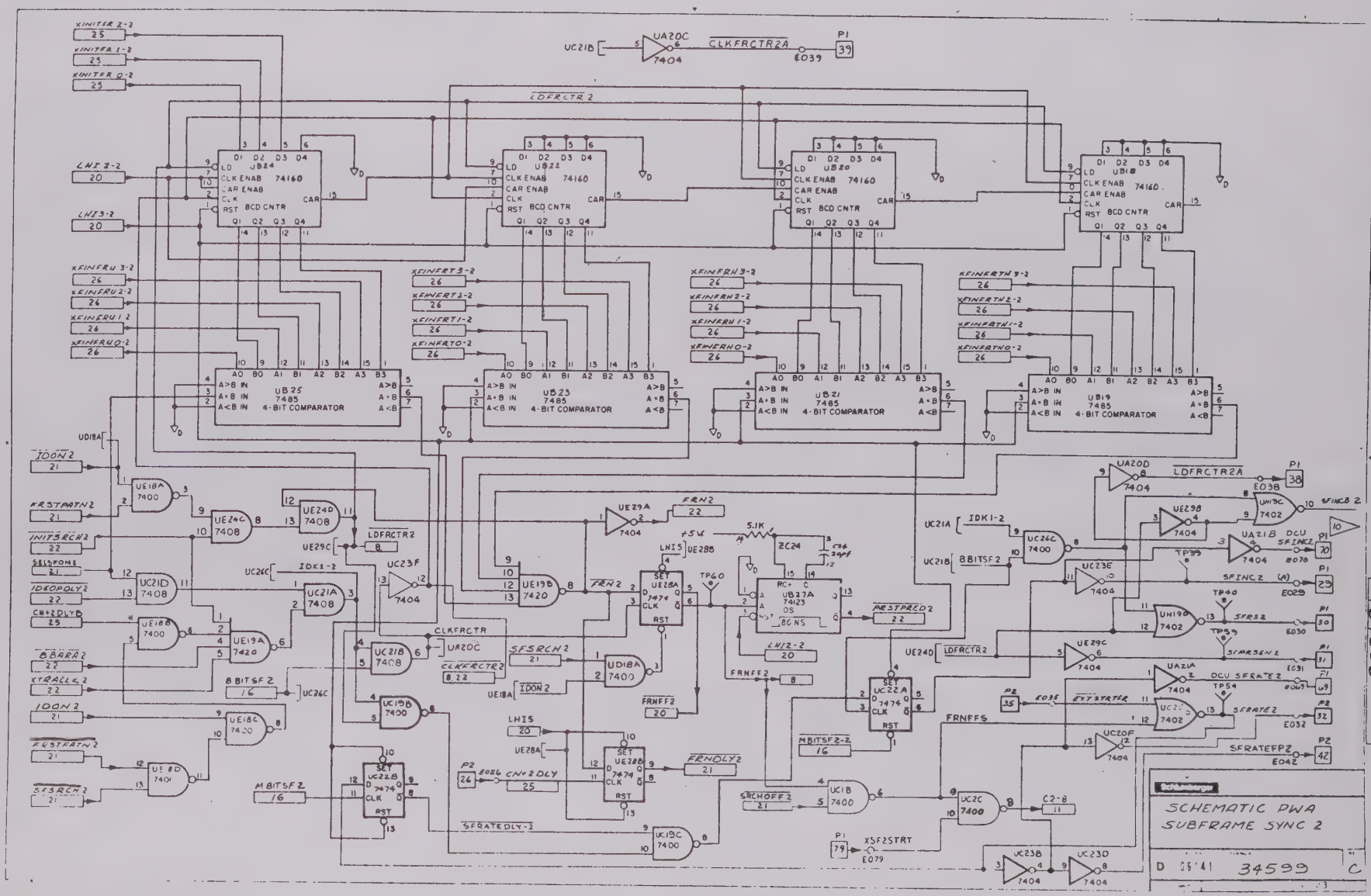
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LDFRCTR2A
CLKFRCTR
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LHIS
LHI2-2
IDON2
IDK1-2
8BITSF2
MBITSF2-2
SFSRCH2
SFRATEDLY-2
SRCHOFF2
PRSTPRED2
SFINC2
SFINC2 (A)
SFRS2
SFSRSEN2
SFRATE2
SFRATEFP2
X5F2STRT
UC21B
UA20C
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E039
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UA20D
E038
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UH13C
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E070
UE29A
UE28B
5.1K
ZC24
C36
22pf
UC21A
UC24C
7400
UC21B
UC23E
TP39
UA21B
DCU SFINC2
E029
25
TP40
UH19B
E030
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TP59
UE24D
UE29C
UA21A
DCU SFRATE2
E031
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TP54
E032
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UC22A
UC20F
E042
42
UC22B
UC18
UC2C
C2-8
11
UC23B
UC23D
P1
79
E079
UE18A
UE24C
UE24D
UC21D
UC23F
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UE28D
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UC2C
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UB24 74160 BCD CNTR
UB22 74160 BCD CNTR
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UB18 74160 BCD CNTR
UB25 7485 4-BIT COMPARATOR
UB23 7485 4-BIT COMPARATOR
UB21 7485 4-BIT COMPARATOR
UB19 7485 4-BIT COMPARATOR
UB27A 74123 DS
80 NS
RC+ C
A B CLR
Q Q
XINITER 2-2
XINITER 1-2
XINITER 0-2
LHI 2-2
LHI 3-2
XFINFRU 3-2
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UD18A
IDON2
FRSTPATN2
INITSRCH2
SBLKFOND2
IDEOPOLY2
CH+2DLYB
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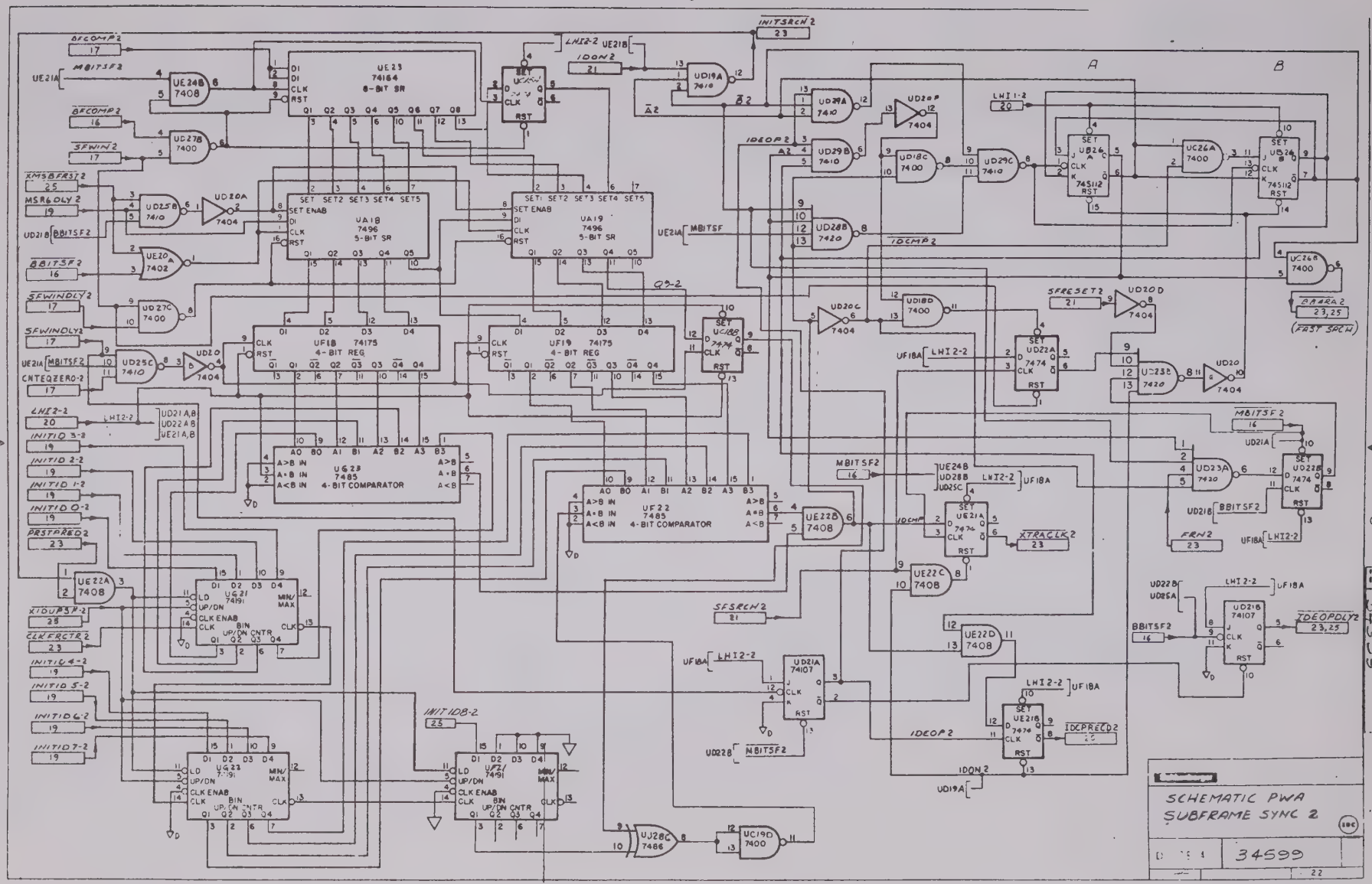
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B
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UA18 7496 5-BIT SR
UA19 7496 5-BIT SR
UF18 74175 4-BIT REG
UF19 74175 4-BIT REG
UG28 7485 4-BIT COMPARATOR
UF22 7485 4-BIT COMPARATOR
UG21 74191
UG22 74191
UF23 74191
UE21 74107
UD21 74107
UD22 74107
UD26 74107
UE24B 7408
UE22A 7408
UE22B 7408
UE22C 7408
UE22D 7408
UD27B 7410
UD27C 7400
UD25B 7410
UD25C 7410
UD19A 7410
UD29A 7410
UD29B 7410
UD29C 7410
UD28B 7420
UD23A 7420
UD23B 7420
UD18C 7400
UC26A 7400
UC26B 7400
UD18D 7400
UD20A 7404
UD20B 7404
UD20C 7404
UD20D 7404
UD20 7404
UJ28C 7486
UC19D 7400
INITSRCH 2
LHI2-2 UE21B
IDON2
IDEOP2
LHI1-2
SFRESET2
BARA2
(FAST SRCH)
XMSBFRST2
MSR6DLY2
BFCOMP2
SFWIN2
SFWINDLY2
CNTEQZERO-2
LHI2-2
INITIQ 3-2
INITID 2-2
INITID 1-2
INITID 0-2
PRSTPRED2
XIDUP3-2
CLKFRCTR2
INITIQ 4-2
INITIQ 5-2
INITIQ 6-2
INITIQ 7-2
INITIDB-2
MBITSF2
BBITSF2
SFSRCH2
IDCMP2
XTRAGLK2
FRN2
IDEOPDLY2
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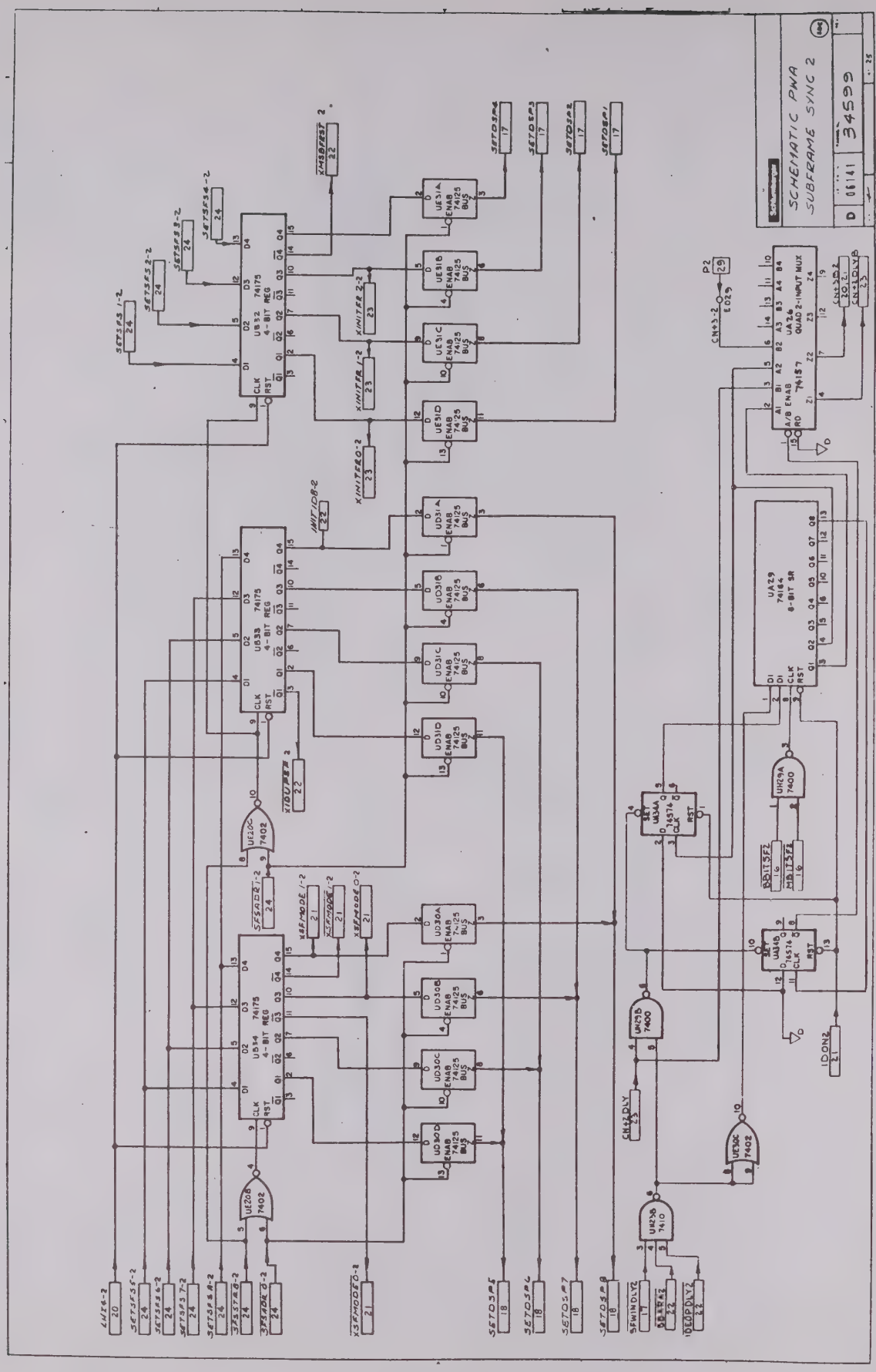
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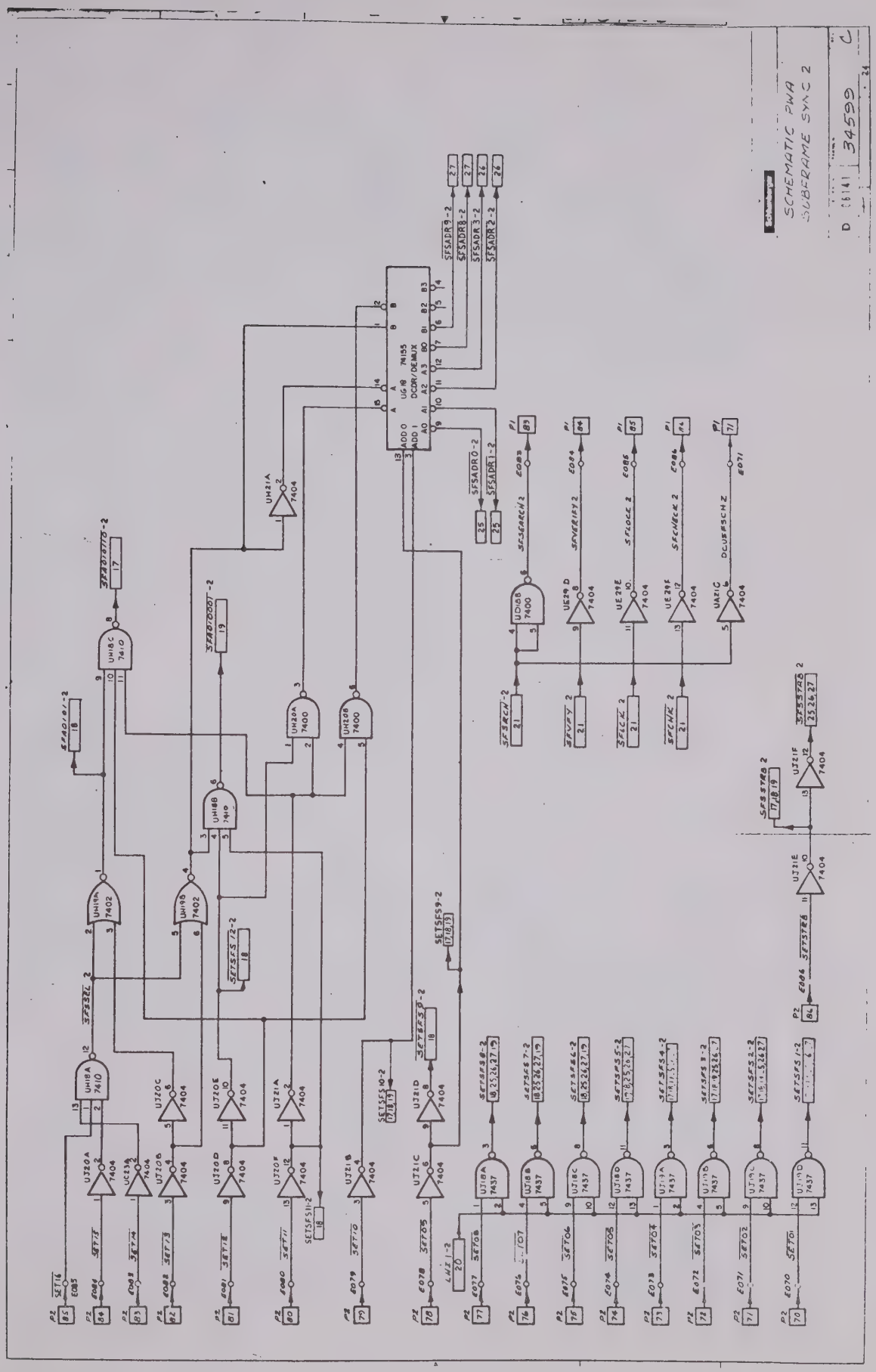
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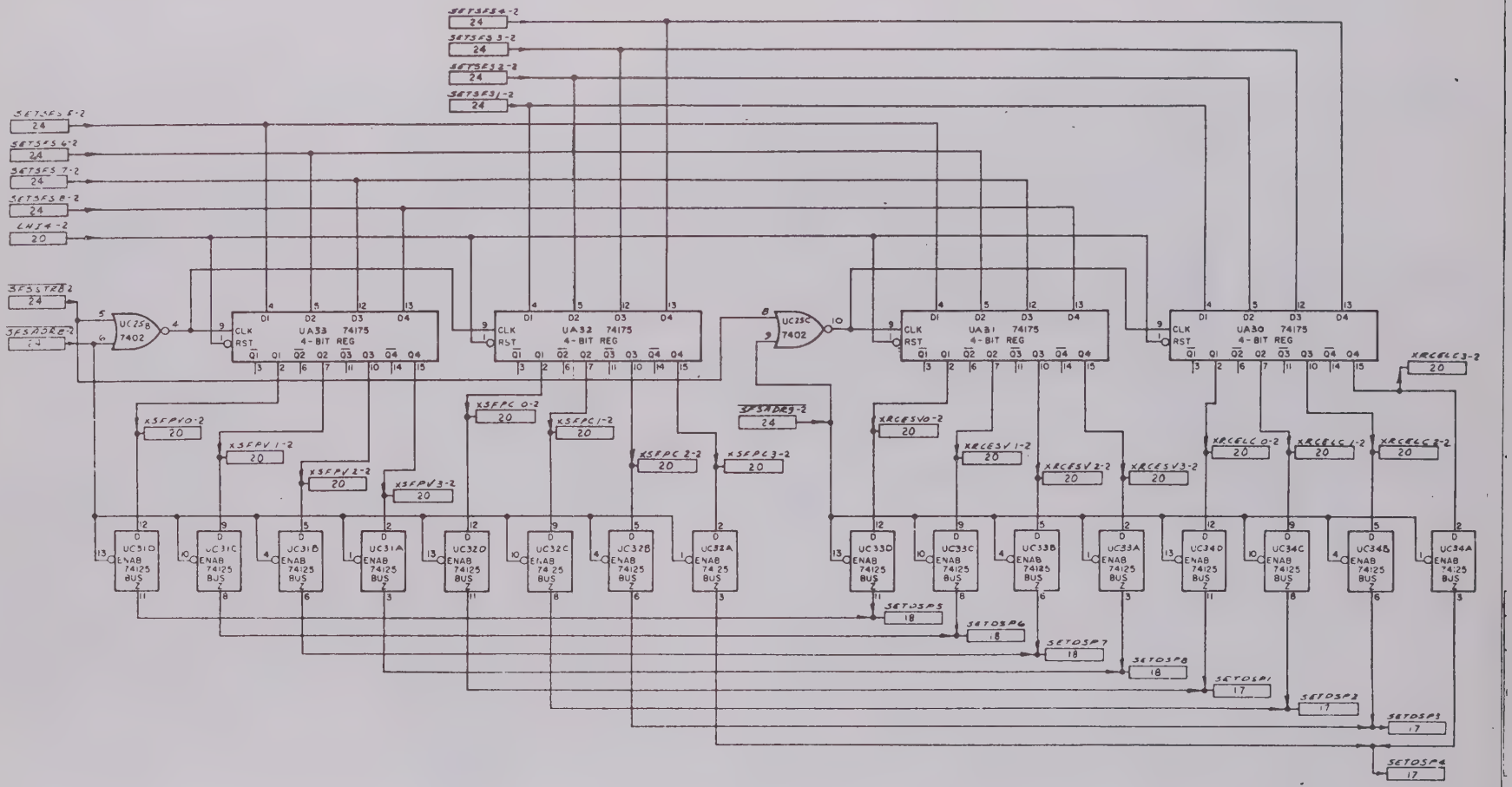
C
UG18 74155
DCDR/DEMUX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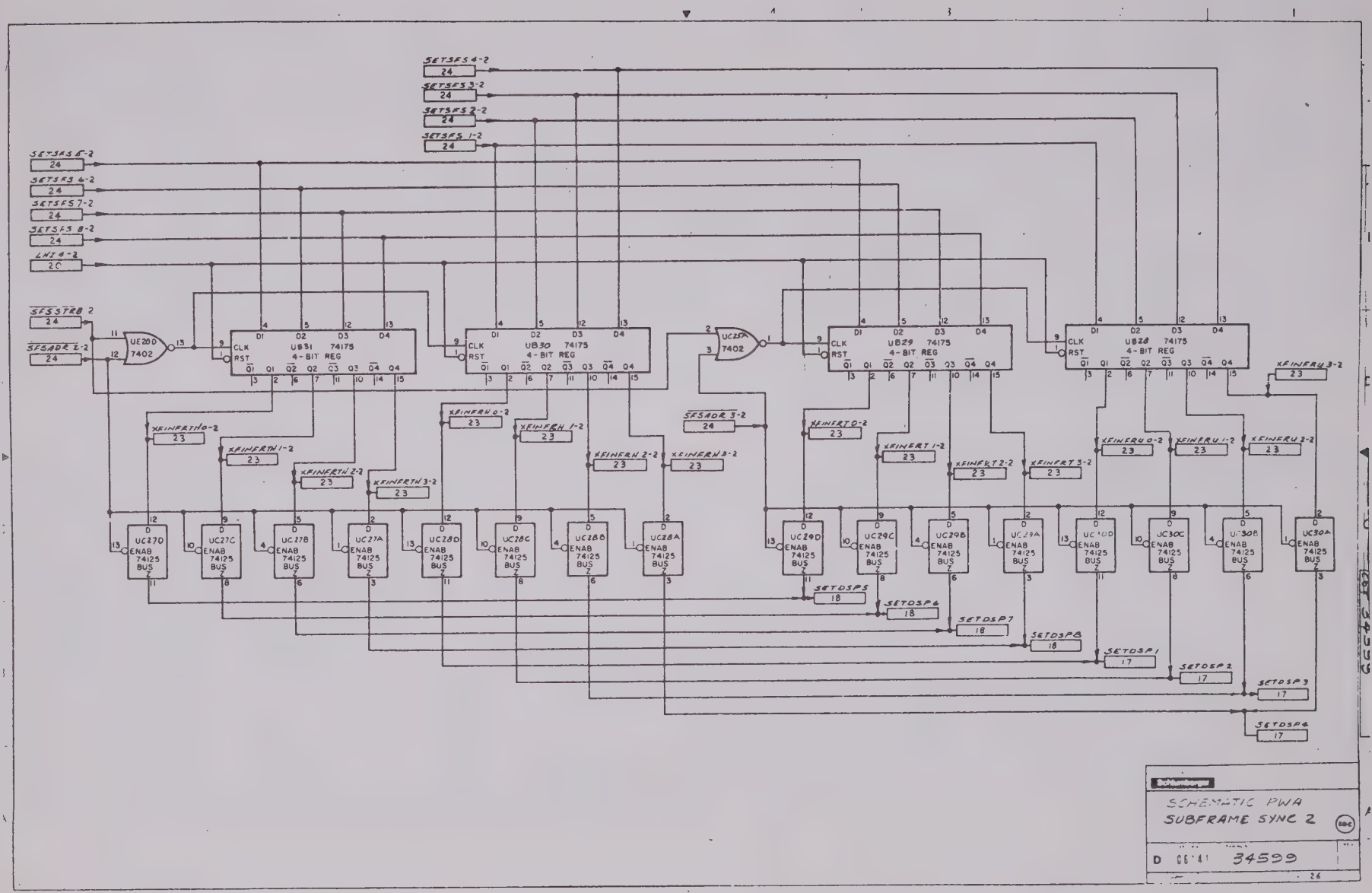
34599
27


SETSFS 4-2
SETSFS 3-2
SETSFS 2-2
SETSFS 1-2
SETSFS 5-2
SETSFS 6-2
SETSFS 7-2
SETSFS 8-2
LNI 4-2
SFS STRB 2
SFSADR 2-2
UE20D 7402
UB31 74175 4-BIT REG
UB30 74175 4-BIT REG
UC25A 7402
UB29 74175 4-BIT REG
UB28 74175 4-BIT REG
XFINFRU 3-2
XFINFRTH 0-2
XFINFRTH 1-2
XFINFRTH 2-2
XFINFRTH 3-2
XFINFRH 0-2
XFINFRH 1-2
XFINFRH 2-2
XFINFRH 3-2
SFSADR 3-2
XFINFRT 0-2
XFINFRT 1-2
XFINFRT 2-2
XFINFRT 3-2
XFINFRU 0-2
XFINFRU 1-2
XFINFRU 3-2
UC27D
UC27C
UC27B
UC27A
UC28D
UC28C
UC28B
UC28A
UC29D
UC29C
UC29B
UC29A
UC30D
UC30C
UC30B
UC30A
ENAB 74125 BUS
SETDSP5
SETDSP6
SETDSP7
SETDSP8
SETDSP1
SETDSP2
SETDSP3
SETDSP4
SCHEMATIC PWA
SUBFRAME SYNC 2
D 06841 34599

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO
1	D GND	1	14
2	+5V	1	14
3	/LDFRCTRX	8	8/13
4	CLKFRCTRX	8	8/13
5	XSIFISTRT	11	8/28
6			
7			
8	SFLOCK	9	(NOT USED)
9	SFSRCH	9	(NOT USED)
10	SFLCK2	21	
11	SFSRCH 2	21	
12	SFVFY	9	
13	SFCHK	9	
14	SFVFY 2	21	
15	SFCHK 2	21	(NOT USED)
16	SFSELLD	8	9/6 (NOT USED)
17			
18	SFIR2SEL	8	13
19	/SFIR2SEL	8	12
20	/SFSRCHLD1	9	13
21	/SFVFYLD1	9	13
22	/SFLCKLD1	9	RP/J23P19
23	/SFCHKLD1	9	13
24			
25	SFRATE	11	RP/J20P1
26	SFINC	11	RP/J20P5
27	SFRS	11	RP/J20P9
28	SFPRSEN	11	RP/J20P13
29	SFINC2	23	RP/J20P7
30	SFRS 2	23	RP/J20P11
31	SFPRSEN 2	23	RP/J20P15
32	C..+2	16	4/12 9
33			
34	FRNFF2A	20	8/13
35	/EXTSTRT R	11	8/18 9
36			
37	IDON 2A	21	8/13
38	/LDFRCTR2A	23	8/13
39	/CLKFRCTR2A	23	8/13
40	/PWRONRST	9	4/8 9
41	CN+2	4	4/12 9
42	SFRATEFP	11	13
43			
44			
45	/SFSRCHLD2	21	8/13
46	/SFVFYLD 2	21	13
47	/SFLCKLD 2	21	RP/J23P18
48	/SFCHKLD2	21	13
49			
50			

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
51	D GND	1	14
52	+5V	1	14
53			
54	/CN+4	8	4/12 9
55			
56	SFSRCHX	8	8/24
57	/SFIRST	9	13
58	SFIRST	9	12
59	SFONX	8	13
60			
61			
62			
63			
64	/SELSETUP	9	10/5 9
65			
66			
67			
68			
69			
70			
71			
72			
73			
74			
75			
76			
77			
78			
79	XSF2STRT	23	8/28
80	/CN+4	20	4/12 9
81	/SF2RST	21	13
82	SF2RST	21	12
83	SFSEARCH 2	24	RP/J20P26
84	SFVERIFY 2	24	RP/J20P28
85	SFLOCK2	24	RP/J20P30
86	SFCHECK2	24	RP/J20P32
87	/SELSETUP	21	10/5 9
88			
89			
90			
91	SFSEARCH	12	RP/J20P18
92	SFVERIFY	12	RP/J20P20
93	SFLOCK	12	RP/J20P22
94	SFCHECK	12	RP/J20P24
95			
96			
97			
98			
99			
100			

P2

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
1	IDONX	8	8/13
2	/SFSRCHX	8	8/13
3	/FRNFFX	11	8/13
4	/FCCP	20	4/9 9
5	FRNFFX	8	8/13
6	SFLOCKX	8	9/6
7	/FSRCH	20	4/11 9
8	/BBIT	16	4/7
9	/MBIT	16	4/7
10	SETDSP1	18	4/16
11	SETDSP2	18	
12	SETDSP3	18	
13	SETDSP4	18	
14	SETDSP5	18	
15	SETDSP6	18	
16	SETDSP7	18	
17	SETDSP8	18	
18	SETDSP1	6	
19	SETDSP2	6	
20	SETDSP3	6	
21	SETDSP4	6	
22	SETDSP5	6	
23	SETDSP6	6	
24	SETDSP7	6	
25	SETDSP8	6	4/16 9
26	CN+2DLY	23	4/12
27	/CN-2	20	4/12
28	MSR6	19	4/6
29	CN+3	20	4/12 9
30			
31			
32	SFRATE 2	23	RP/J20P2
33			
34			
35	/EXTSTRTFR	23	8/7 9
36			
37			
38	/BBIT	4	4/7 9
39	/MBIT	4	4/7
40	/PWRONRST	21	4/8
41	/FCCP	8	4/9 9
42	SFRATEFP2	23	13
43	/FSRCH	8	4/11 9
44	/CN-2	8	4/12 9
45			
46			
47	CN+2DLY	11	4/12 9
48			
49	+5V	1	14
50	D GND	1	14

P2

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO
51			
52			
53	/SET01	12	4/5 9
54	/SET02	12	
55	/SET03	12	
56	/SET04	12	
57	/SET05	12	
58	/SET06	12	
59	/SET07	12	
60	/SET08	12	
61	/SETSTRB	12	
62	/SET09	12	
63	/SET10	12	
64	/SET11	12	
65	/SET12	12	
66	/SET13	12	
67	/SET14	12	
68	/SET15	12	
69	/SET16	12	
70	/SETO1	24	
71	/SETO2	24	
72	/SETO3	24	
73	/SETO4	24	
74	/SETO5	24	
75	/SETO6	24	
76	/SETO7	24	
77	/SETO8	24	
78	/SET09	24	
79	/SET10	24	
80	/SET11	24	
81	/SET12	24	
82	/SET13	24	
83	/SET14	24	
84	/SET15	24	
85	/SET16	24	
86	/SETSTRB	24	4/5
87	MSR6	7	4/6 9
88			
89			
90			
91			
92			
93			
94			
95			
96	CN+3	8	4/12 9
97			
98			
99	+5V	1	14
100	D GND	1	14

12 CONNECT TO GND IN 708

9 DUPLICATE MNEMONICS ARE OF COMMON SOURCE VIA WIRE WRAP EXTERNAL TO THE PWA

14 POWER WIRING SHOWN ON WIRING DIAGRAM 33874

13 NOT USED ON 708

ABBREVIATIONS USED FOR SIGNAL SOURCE AND/OR SIGNAL DESTINATION ADDRESSING & RELATED REF DOCUMENTS ARE AS FOLLOWS ON THIS SHEET:
2: CARD 2 (3 (DWG 34601) RP = REAR PANEL (DWG , REF I/O LIST DWG 34595) CONNECTIONS ARE INDICATED BY CONNECTOR "J" NO. & PIN NO
4: CARD 4 (DWG 34593)
5: CARD 5 (DWG 34599)
6: CARD 6 (DWG 34590)
7: CARD 7 (DWG 34593)
8: CARD 8 (DWG 34604)
10: CARD 10 (DWG 34309)

NOTES: CONTINUED

SCHEMATIC, PWA.
SUBFRAME SYNC 2
FUNCTION #5

D	06141	34599	4

29

P1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
1	D GND	1	11
2	+5V	1	11
3	/LDFRCTRX	8	8/15
4	CLKFRCTRX	8	3/15
5	XSFISTRT	11	8/24
6			
7			
8	SFLOCK	9	(NOT USED)
9	SFSRCH	9	
10	SFLCK 2	21	
11	SFSRCH 2	21	
12	SFVFY	9	
13	SFCHK	9	
14	SFVFY 2	21	
15	SFCHK 2	21	(NOT USED)
16	SFSCLLD	8	9/6 (NOT USED)
17			
18	SFIR2SEL	8	FP/3
19	/SFIA2SEL	8	FP/3
20	/SFS2CHLD 1	9	FP/5
21	/SFVFYLD 1	9	FP/5
22	/SFLCKLD 1	9	FP/5
23	/SFCHKLD 1	9	FP/5
24			
25	SFRATE	11	RP/J33PA2
26	SFINC	11	RP/J33PA6
27	SFRS	11	RP/J33PA10
28	SFPRSEN	11	RP/J33PD13
29	SFINC 2	23	RP/J33PA8
30	SFRS 2	23	RP/J33PA12
31	SFPRSEN 2	23	RP/J33PC2
32	CN+2	16	4/12 9
33			
34	FRNFFA	20	16
35	/EXTSTRTFR	11	8/7 9
36			
37	IDON2A	21	16
38	/LDFRCTR2A	23	16
39	/CLKFRCTR2A	23	16
40	/PWRONRST	9	4/8 8
41	CN+2	4	4/12 8
42	SFRATEFP	11	FP/4
43			
44			
45	/SFSRCHLD 2	21	FP/5
46	/SFVFYLD 2	21	FP/5
47	/SFLCKLD 2	21	FP/5
48	/SFCHKLD 2	21	FP/5
49			
50			

P1

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51	DGND	1	11
52	+5V	1	11
53			
54	/CN+4	8	4/12 9
55			
56	SFSRCHX	8	8/20, 9/6
57	/SFIRST	9	FP/4
58	SFIRST	9	FP/4
59	SFONX	8	9/14, 9/8
60			
61			
62			
63			
64	/SELSETUP	9	0/5 9
65			
66	DCU SFRATE	11	RP/J38PA2
67	DCU SFINC	11	RP/J38PA6
68	DCU SFSCH	12	RP/J38PC4
69	DCU SFRATE 2	23	RP/J38PA4
70	DCU SFINC 2	23	RP/J38PA8
71	DCU SFSCH 2	24	RP/J38PC12
72			
73			
74			
75			
76			
77			
78			
79	XSF2STRT	23	8/24
80	/CN+4	20	4/12 9
81	/SF2RST	21	FP/4
82	SF2RST	21	FP/4
83	SFSEARCH 2	24	RP/J33PC12
84	SFVERIFY 2	24	RP/J33PE2
85	SFLOCK 2	24	RP/J33PE4
86	SFCHECK 2	24	RP/J33PE6
87	/SELSETUP	21	10/5 8
88			
89			
90			
91	SFSEARCH	12	RP/J33PC4
92	SFVERIFY	12	RP/J33PC6
93	SFLOCK	12	RP/J33PC8
94	SFCHECK	12	RP/J33PC10
95			
96			
97			
98			
99			
100			

P2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
1	IDONX	8	8/5
2	/SFSRCHX	8	8/5
3	/FRNFFX	11	8/7
4	/FCCP	20	4/9 9
5	FRNFFX	8	8/14
6	SFLOCKX	8	9/6
7	/FSRCH	20	4/11
8	/BBIT	16	4/7
9	/MBIT	16	4/7
10	SETDSP 1	18	4/16
11	SETDSP 2	18	
12	SETDSP 3	18	
13	SETDSP 4	18	
14	SETDSP 5	18	
15	SETDSP 6	18	
16	SETDSP 7	18	
17	SETDSP 8	18	
18	SETDSP 1	6	9
19	SETDSP 2	6	
20	SETDSP 3	6	
21	SETDSP 4	6	
22	SETDSP 5	6	
23	SETDSP 6	6	
24	SETDSP 7	6	
25	SETDSP 8	6	4/16
26	CN+2DLY	23	4/12
27	/CN-2	20	4/12
28	MSR6	19	4/6
29	CN+3	20	4/12
30			
31			
32	SFRATE 2	23	RP/J33PA4
33			
34			
35	/EXTSTRTFR	23	8/7 9
36			
37			
38	/BBIT	4	4/7
39	/MBIT	4	4/7 9
40	/PWRONRST	21	4/8
41	/FCCP	8	4/9
42	SFRATEFP2	23	FP/4
43	/FSRCH	8	4/11 9
44	/CN-2	8	4/12 9
45			
46			
47	CN+2DLY	11	4/12 9
48			
49	+5V	1	11
50	DGND	1	11

P2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO.
51			
52			
53	/SET01	12	4/5
54	/SET02	12	
55	/SET03	12	
56	/SET04	12	
57	/SET05	12	
58	/SET06	12	
59	/SET07	12	
60	/SET08	12	
61	/SETSTRB	12	
62	/SET09	12	
63	/SET10	12	
64	/SET11	12	
65	/SET12	12	
66	/SET13	12	
67	/SET14	12	
68	/SET15	12	
69	/SET16	12	9
70	/SET01	24	
71	/SET02	24	
72	/SET03	24	
73	/SET04	24	
74	/SET05	24	
75	/SET06	24	
76	/SET07	24	
77	/SET08	24	
78	/SET09	24	
79	/SET10	24	
80	/SET11	24	
81	/SET12	24	
82	/SET13	24	
83	/SET14	24	
84	/SET15	24	
85	/SET16	24	
86	/SETSTRB	24	4/5
87	MSR6	7	4/6
88			
89			
90			
91			
92			
93			
94			
95			
96	CN+3	8	4/12 8
97			
98			
99	+5V	1	11
100	DGND	1	11

9 DUPLICATE MNEMONICS ARE OF COMMON SOURCE VIA WIRE WRAP EXTERNAL TO THE PWA.

8 ABBREVIATIONS USED FOR SIGNAL SOURCE AND/OR SIGNAL DESTINATION ADDRESSING & RELATED REF. DOCUMENTS ARE AS FOLLOWS ON THIS SH:

FP = FRONT PANEL (DWG. 29070)
PS = POWER SUPPLY (DWG 32945)
2 = CARD2 (DWG. 34307)
4 = CARD4 (DWG. 34595)
5 = CARD5 (DWG. 34599)

RP = REAR PANEL (DWG ——, REF I/O LIST DWG 32938) CONNECTIONS ARE INDICATED BY CONNECTOR "J" NO. & PIN NO
6 = CARD6 (DWG. 34590)
7 = CARD7 (DWG. 34593)
8 = CARD8 (DWG. 34597)
10 = CARD10 (DWG. 34309)

NOTES: CONTINUED

16 NOT USED ON 710-02

11 POWER WIRING SHOWN ON WIRING DIAGRAM 32945.

FOR 710-02 ONLY

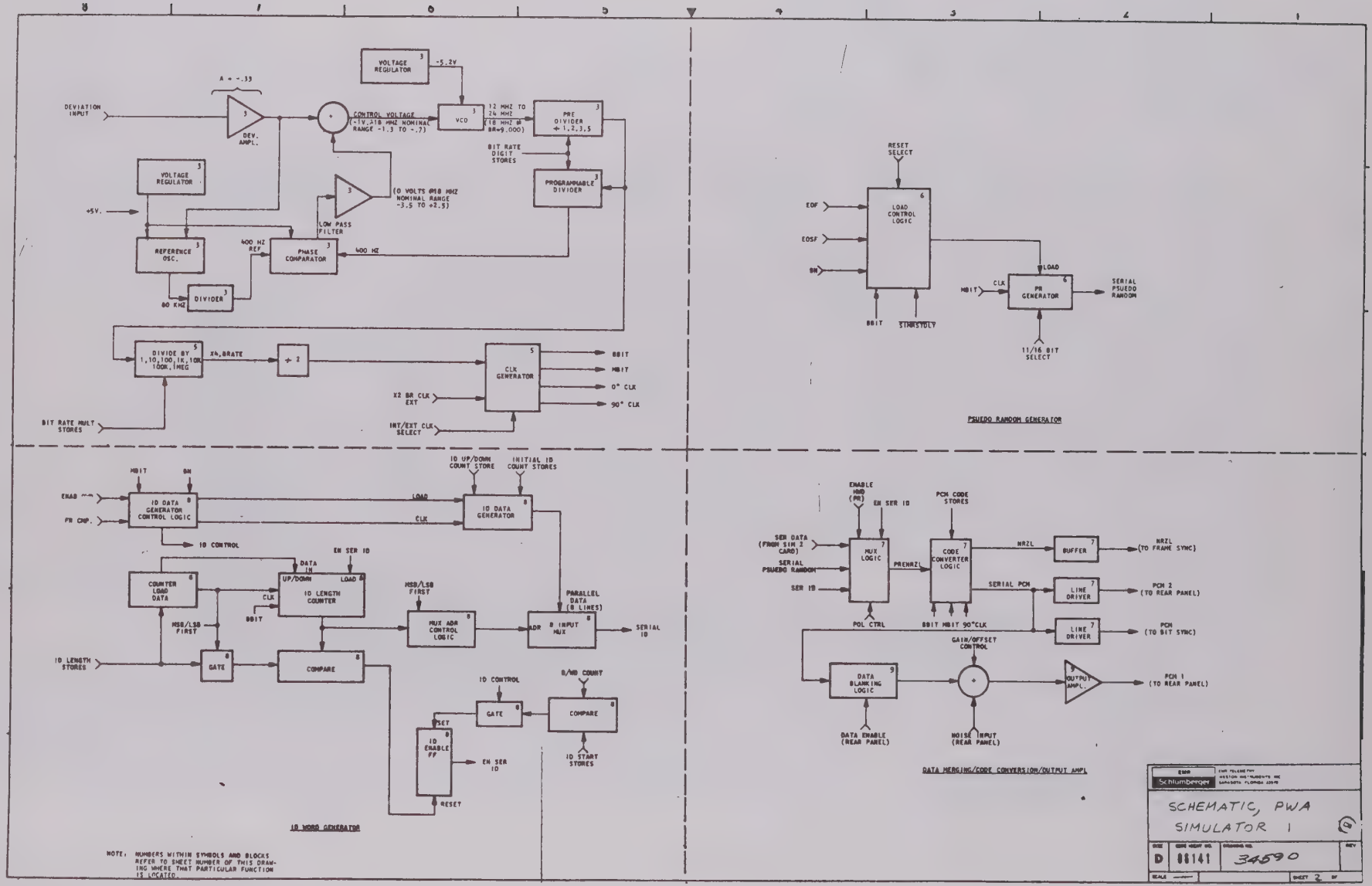
Schlumberger

SCHEMATIC, PWA,
SUBFRAME SYNC 2
FUNCTION -5

D	06141	34599	C

SH 28

6-107



NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

Schlumberger

SCHEMATIC, PWA
SIMULATOR I

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	88141	34590	

SCALE — SHEET 2 OF

COMPONENT CHART	
REF DES	PART NUMBER
C71	
CR 8	
E4	
R 75	
TP 10	TP4-9
U50	
27	
F2	

UNUSED CKTS REF DES	TYPE	CKT UNITS
U17	7400	D
U40	7400	C
U5		C
U13	74107	B
U15	7420	B
U19	74107	A
U20	7400	A
U22	7402	A,B
U23	7437	C
U27	7404	B,D
U30	7400	A,B
U32	7400	A,D
U34	7400	B
U35	74S74	B
U37	74S112	A
U36	74H00	A,D
U40	74S04	A,[illegible],D
U41	74S00	A,C,D
U53	74S112	B
U56	7400	A
U61	74S04	A,B,C,[illegible]
U63	7486	C,D
U64	74H00	D
U74	7400	B
U75	7404	B,C,D,E
U76	7486	A,B,D
U80	MC4044	C
U85	74H00	A,B,C
U90	7437	A,B,D

POWER PINS REF DES	+5V	GND
U1	5	10
U2	5	10
U3	5	10
U4	5	10
U5	14	7
U6	14	7
U7	14	7
U8	14	7
U9	16	8
U10	14	7
U11	14	7
U12	14	7
U13	14	7
U14	14	7
U15	14	7
U16	14	7
U17	14	7

POWER PINS REF DES	+5V	GND
U18	5	10
U19	14	7
U20	13	7
U21	16	8
U22	14	7
U23	14	7
U24	14	7
U25	16	8
U26	16	8
U27	14	7
U28	5	12
U29	14	7
U30	14	7
U31	14	7
U32	14	7
U33	14	7
U34	14	7

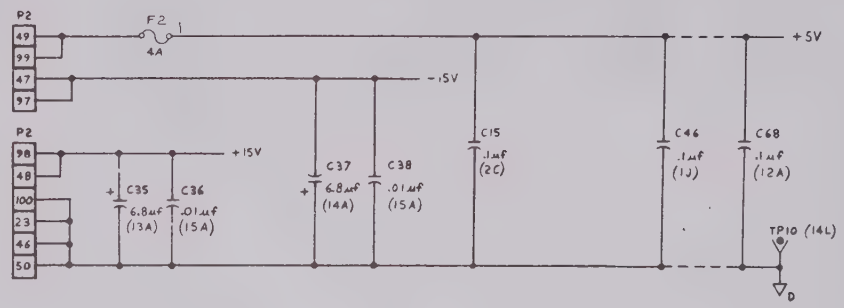
POWER PINS REF DES	+5V	GND
U35	14	7
U36	14	7
U37	16	8
U38	5	12
U39	14	7
U40	14	7
U41	4	7
U42	14	7
U43	4	7
U44	14	7
U45	14	7
U46	16	8
U47	16	8
U48	14	7
U49	14	7
U50	4	7
U51	14	7

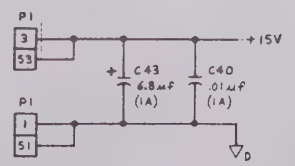
POWER PINS REF DES	+5V	GND
U52	14	7
U53	16	8
U54	16	8
U55	16	8
U56	14	7
U57	14	7
U58	16	8
U59	14	7
U60	14	7
U61	14	7
U62	14	7
U63	14	7
U64	14	7
U65	16	8
U66	16	8
U67	16	8
U68	14	7

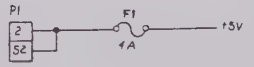
POWER PINS REF DES	+5V	GND
U69	14	7
U70	16	8
U71	16	8
U72	14	7
U74	14	7
U75	14	7
U76	14	7
U77	5	10
U78	5	10
U79	14	7
U82	14	7
U82	14	7
U83	14	7
U84	8	11,5
U85	14	7
U87	SEE SHT 9	7
U89	16	8

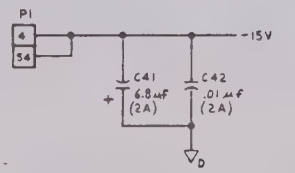
POWER PINS REF DES	+5V	GND
U90	14	7

REVISION				
B	ECO-5233B ALL IO 73 PINS!			









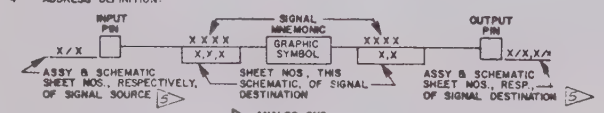
7 SEE WIRING DIAGRAM 32945

6 REMOVE JUMPER FOR TEST PURPOSES

5 ABBREVIATIONS USED FOR SIGNAL SOURCE AND/OR SIGNAL DESTINATION ADDRESSING & RELATED REF. DOCUMENTS ARE AS FOLLOWS:

FP = FRONT PANEL (DWG. 28079)
PS = POWER SUPPLY (DWG. 32945)
4 = CARD 4 (DWG. 34595)
5 = CARD 5 (DWG 34599)
RP = REAR PANEL (DWG ——— ; REF I/O LIST DWG 32938) CONNECTIONS ARE INDICATED BY CONNECTOR "J" NO. & PIN NO.
7 = CARD 7 (DWG 34593)

4 ADDRESS DEFINITION:



3. CIRCUIT RETURN SYMBOLS: ANALOG GND. (A); DIGITAL GND. (D)

2 FOR TOLERANCES AND RATINGS SEE PARTS LIST.

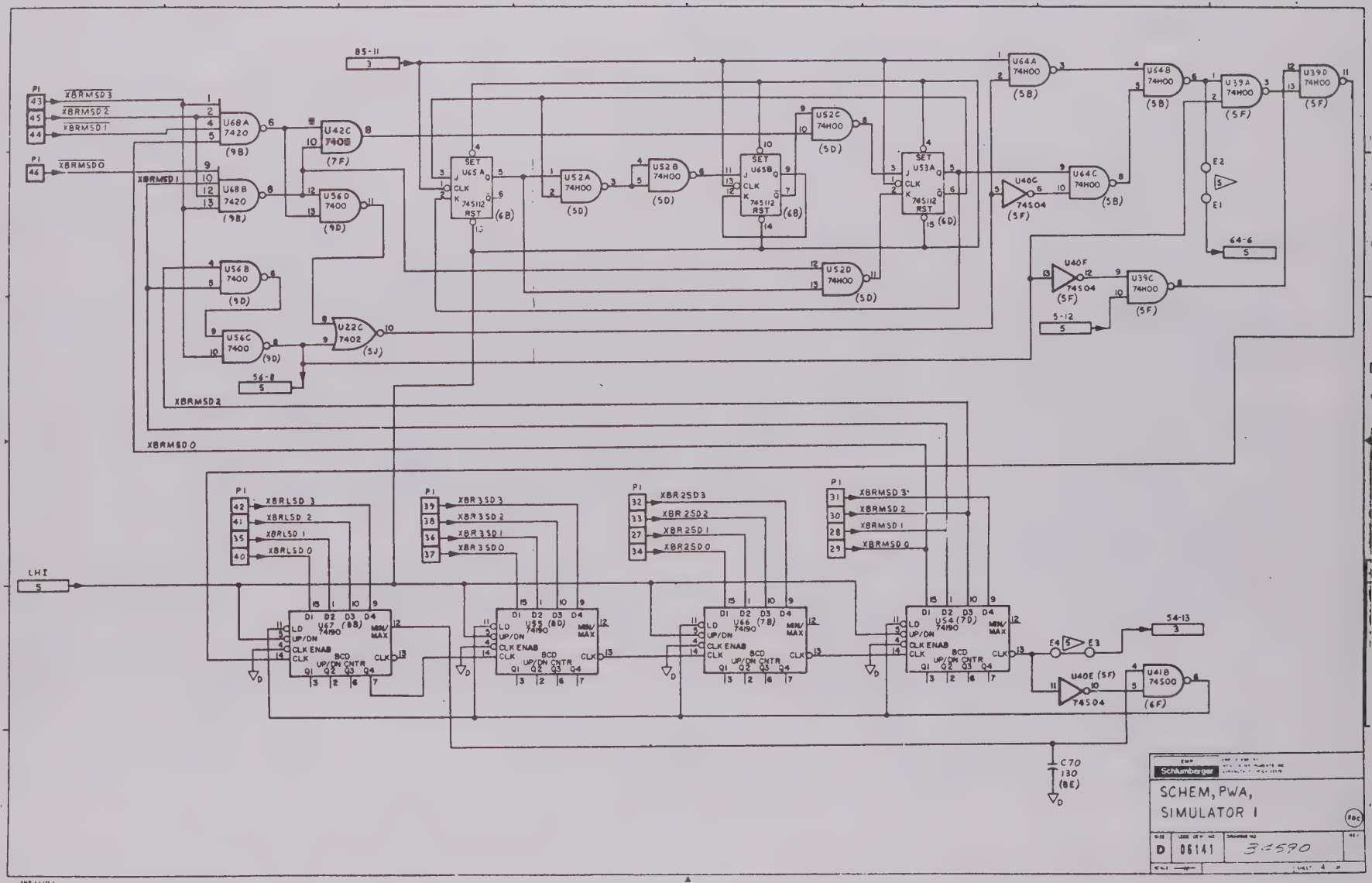
1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

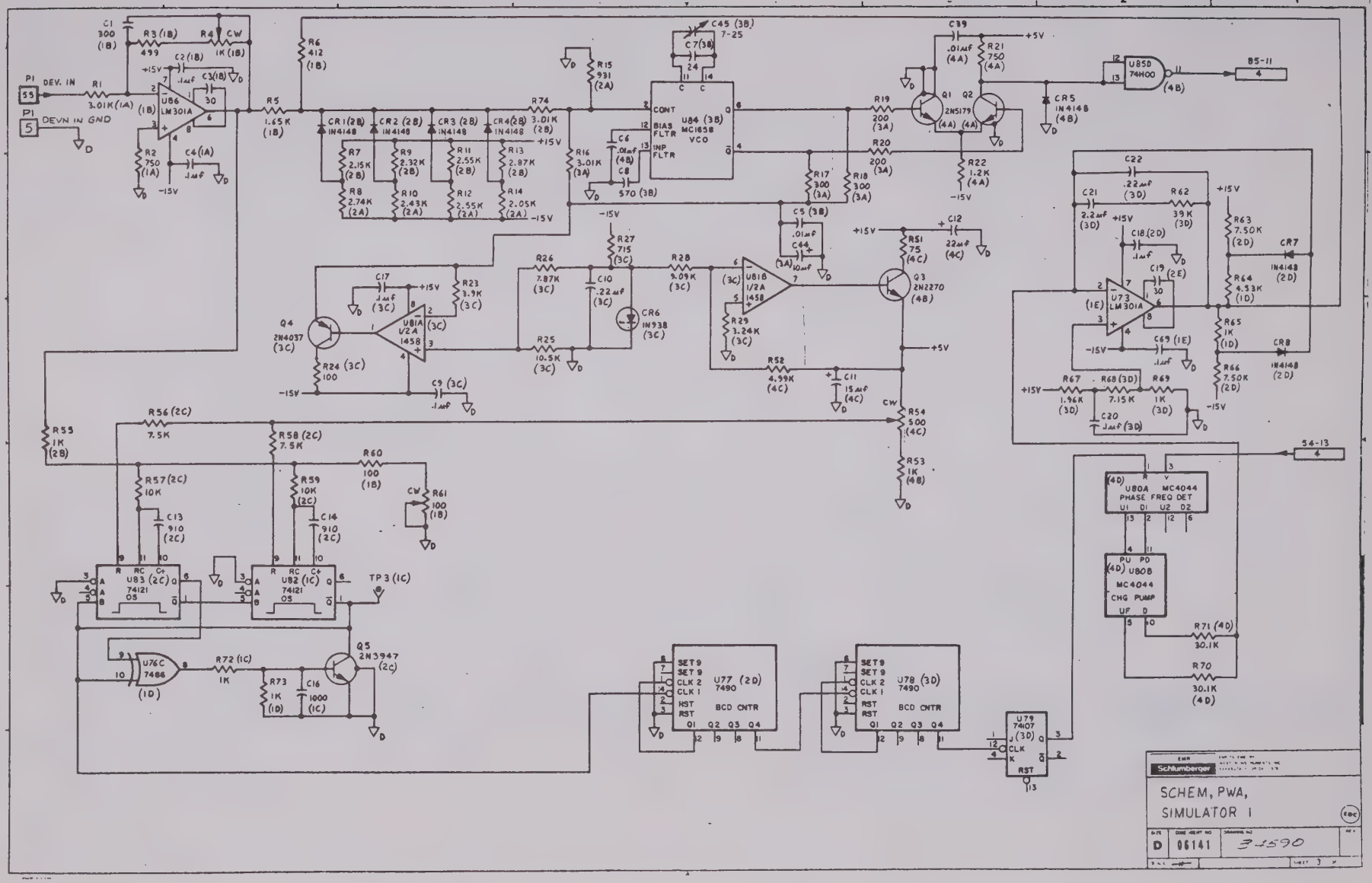
UNLESS OTHERWISE SPECIFIED:

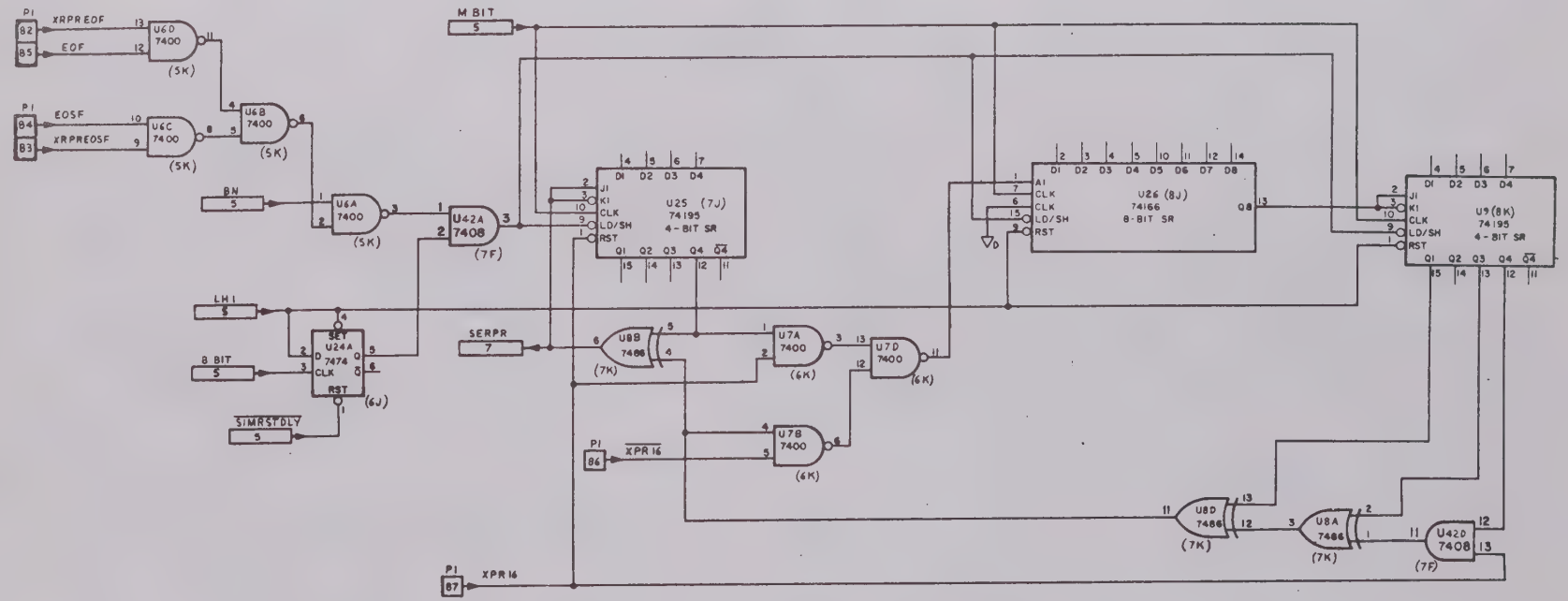
NOTES:

PARTS LIST

SCHEM, PWA, SIMULATOR I FUNCTION 6			
	D	05141	32590 B

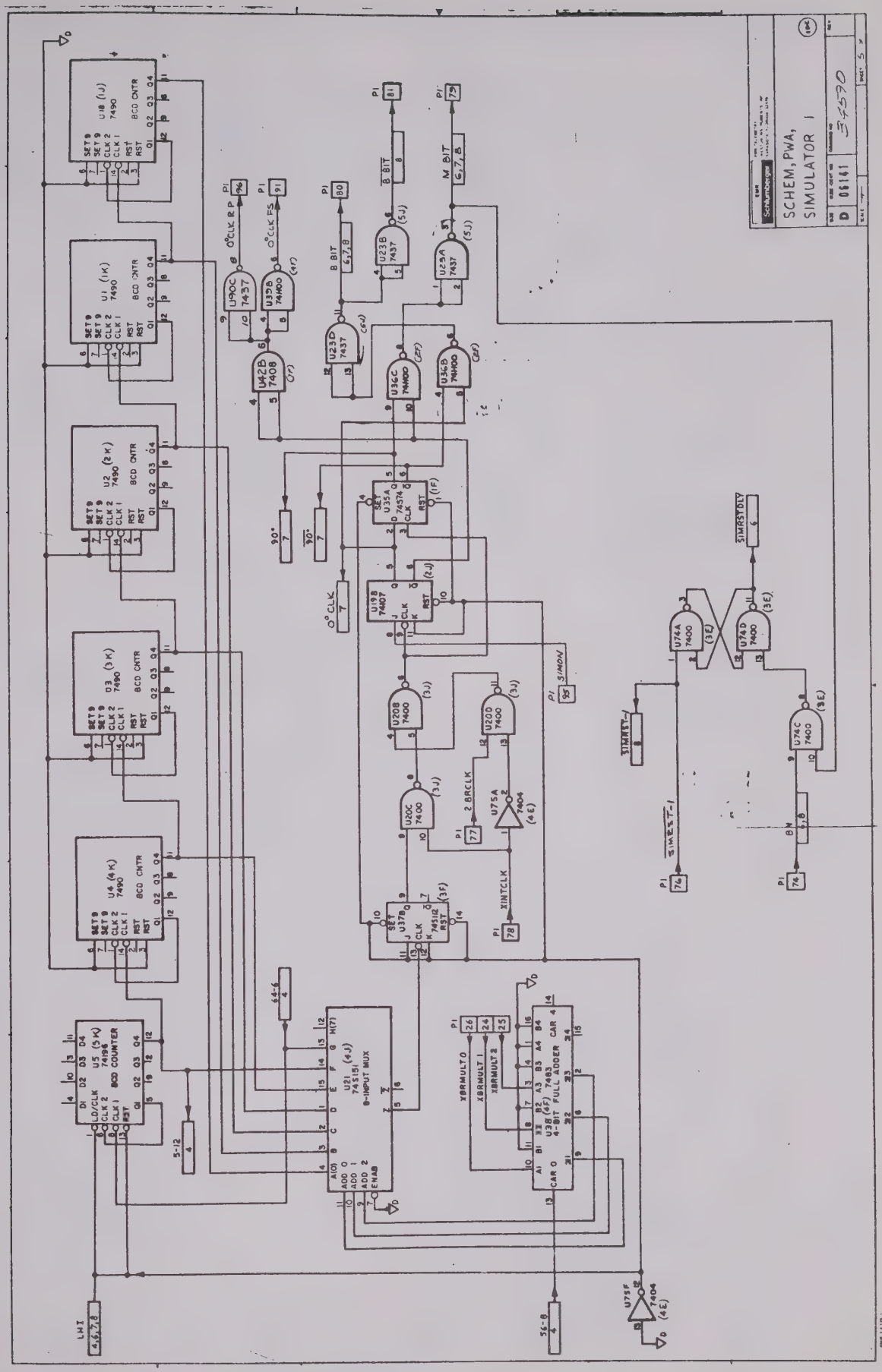

XBRMSD3
XBRMSD2
XBRMSD1
XBRMSD0
XBRMSD1
XBRMSD2
XBRMSD0
XBRLSD3
XBRLSD2
XBRLSD1
XBRLSD0
XBR3SD3
XBR3SD2
XBR3SD1
XBR3SD0
XBR2SD3
XBR2SD2
XBR2SD1
XBR2SD0
XBRMSD3
XBRMSD2
XBRMSD1
XBRMSD0
LHI
BS-11
U68A 7420
U68B 7420
U42C 7408
U56D 7400
U56B 7400
U56C 7400
U22C 7402
U65A 74S112
U65B 74S112
U52A 74H00
U52B 74H00
U52C 74H00
U52D 74H00
U53A 74S112
U64A 74H00
U64B 74H00
U64C 74H00
U39A 74H00
U39C 74H00
U39D 74H00
U40C 74S04
U40F 74S04
U40E 74S04
U41B 74S00
U47 74190
U33 74190
U66 74190
U54 74190
C70 130
SCHEM, PWA, SIMULATOR I
Schlumberger
D 06141
3-590

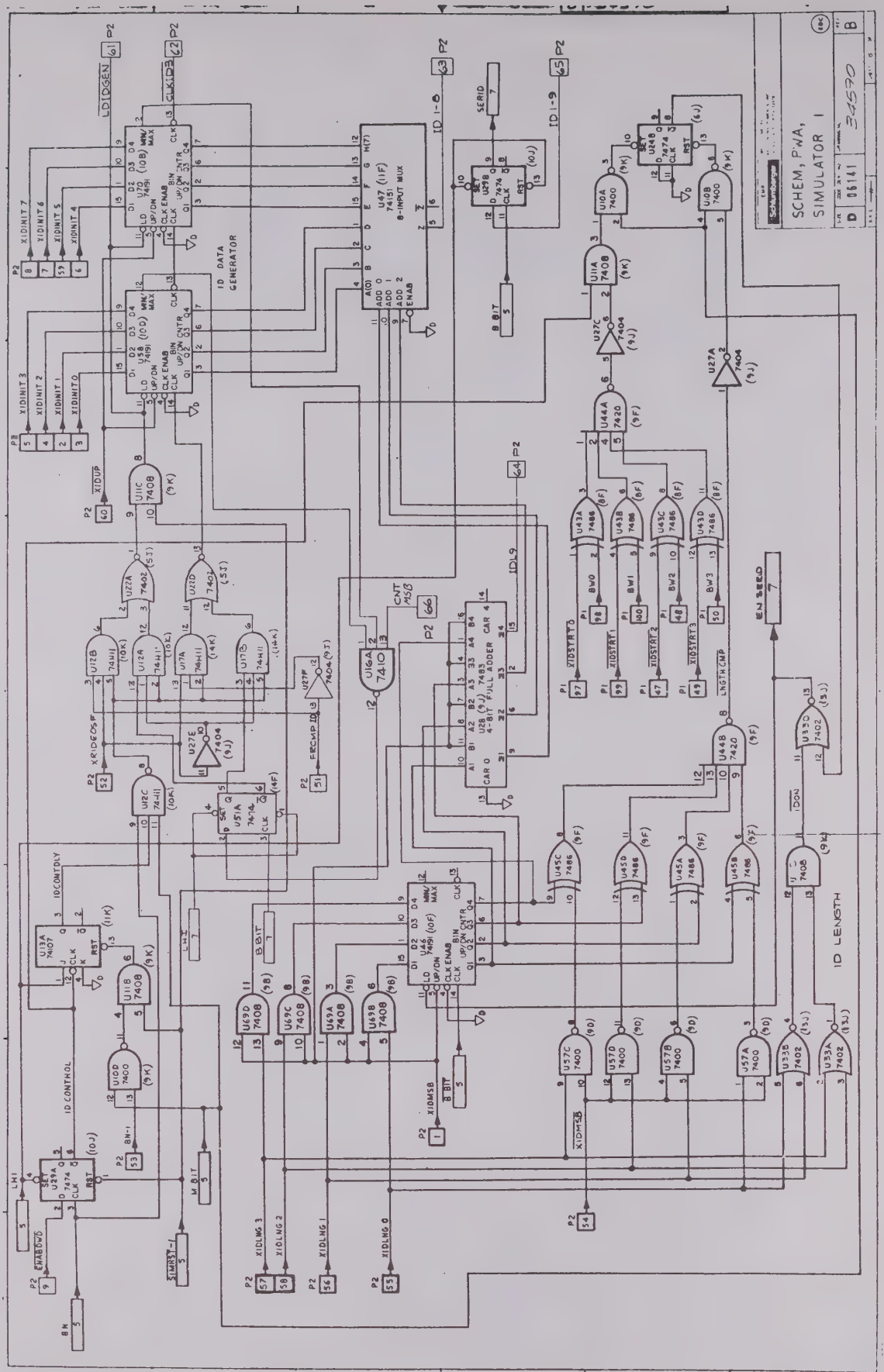

P1 55 DEV. IN
P1 5 DEVN IN GND
U86 LM301A (1B)
U84 (3B) MC1658 VCO
U81A 1/2A 1458 (3C)
U81B 1/2A 1458 (3C)
U73 LM301A (1E)
U80A MC4044 PHASE FREQ DET
U80B MC4044 CHG PUMP
U82 (1C) 74121 OS
U83 (2C) 74121 OS
U76C 7486 (1D)
U77 (2D) 7490 BCD CNTR
U78 (3D) 7490 BCD CNTR
U79 7407 (3D)
U85D 74H00 (4B)
Q1 Q2 2N5179 (4A) (4A)
Q3 2N2270 (4B)
Q4 2N4037 (3C)
Q5 2N3947 (2C)
CR1 (2B) IN4148
CR2 (2B) IN4148
CR3 (2B) IN4148
CR4 (2B) IN4148
CR5 IN4148 (4B)
CR6 IN938 (3C)
CR7 IN4148 (2D)
CR8 IN4148 (2D)
C45 (3B) 7-25
TP3 (1C)
BS-11 4
54-13 4
SCHEM, PWA, SIMULATOR I
D 06141 3-1590

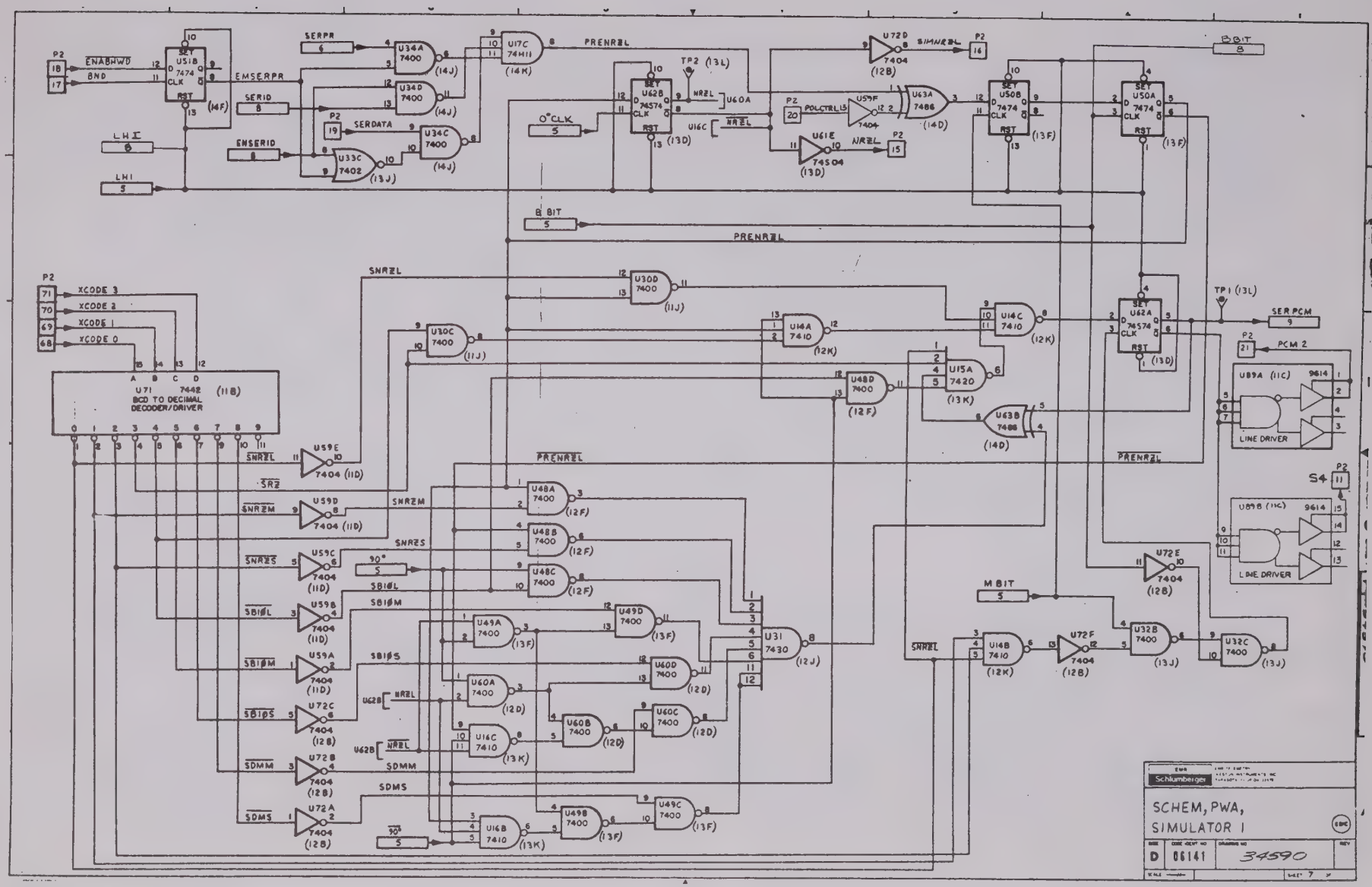


SCHEM, PWA,
SIMULATOR 1

D | 06141 | 34590


SCHEM, PWA,
SIMULATOR I
D 06141
34590
U18 (1J) 7490
U1 (1K) 7490
U2 (2K) 7490
U3 (3K) 7490
U4 (4K) 7490
U5 (5K) 74196
U21 (4J) 74S151
U38 (4F) 7483
U35A 74S74
U19B 74107
U37B 74S112
U90C 7437
U39B 74H00
U42B 7408
U23B 7437
U23A 7437
U23D 7437
U36C 74H00
U36B 74H00
U20B 7400
U20D 7400
U20C 7400
U75A 7404
U74A 7400
U74D 7400
U74C 7400
U75F 7404
LHI
XBRMULT 0
XBRMULT 1
XBRMULT 2
XINTCLK
2 BRCLK
SIMRST-1
SIMRSTDLY
SIMON
B BIT
M BIT
0° CLK
0° CLK RP
0° CLK FS
BCD CNTR
BCD COUNTER
8-INPUT MUX
4-BIT FULL ADDER


SCHEM, PWA,
SIMULATOR I
D 06141
B
ID DATA GENERATOR
ID CONTROL
ID LENGTH
LDIDGEN
CLKID3
ID 1-0
ID 1-9
SERID
8 BIT
XIDINIT7
XIDINIT6
XIDINIT5
XIDINIT4
XIDINIT3
XIDINIT2
XIDINIT1
XIDINIT0
XIDUP
XRIDEOSF
FRCMP ID
CNT 15B
XIDSTRT0
XIDSTRT1
XIDSTRT2
XIDSTRT3
LNGTH CMP
ENJ SEED
IDON
XIDMSB
XIDLNG 3
XIDLNG 2
XIDLNG 1
XIDLNG 0
EXABDWD
8N
BN-1
M BIT
LNGTH-1
IDCONTDLY
LNI
B BIT
L BIT


P2
ENABHWD
BND
U51B 7474
EMSERPR
SERPR
SERID
SERDATA
ENSERID
LHI
U34A 7400
U34D 7400
U34C 7400
U33C 7402
U17C 74H11
PRENRZL
TP2 (13L)
U62B 74S74
U60A
U61C
0°CLK
U59F 7404
U63A 7486
U61E 74S04
U72D 7404
SIMNRZL
BBIT
U50B 7474
U50A 7474
8 BIT
PRENRZL
SNRZL
XCODE 3
XCODE 2
XCODE 1
XCODE 0
U71 7442
BCD TO DECIMAL DECODER/DRIVER
U30D 7400
U30C 7400
U14A 7410
U14C 7410
U15A 7420
U48D 7400
U63B 7486
U62A 74S74
TP1 (13L)
SER PCM
PCM 2
U89A (11C)
9614
LINE DRIVER
S4
U89B (11C)
U59E 7404
SRZ
SNRZM
U59D 7404
SNRZS
U59C 7404
90°
SBIØL
U59B 7404
SBIØM
U59A 7404
SBIØS
U72C 7404
SDMM
U72B 7404
SDMS
U72A 7404
U48A 7400
U48B 7400
U48C 7400
U49D 7400
U49A 7400
U60D 7400
U60A 7400
U60B 7400
U60C 7400
U16C 7410
U16B 7410
U49B 7400
U49C 7400
U31 7430
MBIT
U72E 7404
U14B 7410
U72F 7404
U32B 7400
U32C 7400
Schlumberger
SCHEM, PWA,
SIMULATOR I
D
06141
34590

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO
1	DGND	1	7
2	+5V	1	7
3	+15V	1	7
4	-15V	1	7
5	DEV IN GND	3	RP/J5
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23	DGND	1	7
24	XBRMULT 1	5	7/14
25	XBRMULT 2	5	7/14
26	XBRMULT 0	5	7/14
27	XBR2SD1	4	7/14
28	XBRMSD1	4	7/14
29	XBRMSD0	4	7/14
30	XBRMSD2	4	7/14
31	XBRMSD3	4	7/14
32	XBR2SD3	4	7/14
33	XBR2SD2	4	7/14
34	XBR2SD0	4	7/14
35	XBRL3D1	4	7/15
36	XBR3SD1	4	7/15
37	XBR3SD0	4	7/15
38	XBR3SD2	4	7/15
39	XBR3SD3	4	7/15
40	XBRL3D0	4	7/15
41	XBRL3D2	4	7/15
42	XBRL3D3	4	7/15
43	/XBRMSD3	4	7/14
44	/XBRMSD1	4	7/14
45	/XBRMSD2	4	7/14
46	/XBRMSD0	4	7/14
47	/XIDSTRT2	8	7/17
48	BW2	8	7/4
49	/XIDSTRT3	8	7/17
50	BW3	8	7/4

P1

PIN NO	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO. / SCHEM SHEET NO
51	DGND		7
52	+5V		7
53	+15V	1	7
54	-15V	1	7
55	DEV IN	3	RP/J5
56			
57			
58			
59			
60			
61			
62			
63			
64			
65			
66			
67			
68			
69			
70			
71			
72			
73			
74	BN	5	7/4
75			
76	/SIMRST-1	5	7/4
77	2BRCLK	5	RP/J2
78	XINTCLK	5	7/14
79	MBIT	5	7/4
80	BBIT	5	7/4
81	/BBIT	5	7/4
82	XRPREOF	6	7/18
83	XRPREOSF	6	7/18
84	EOSF	6	7/9
85	EOF	6	7/6
86	/XPRI6	6	7/18
87	XPRI6	6	7/18
88			
89			
90			
91	0°CLK F3	5	4/7, 7/5
92			
93			
94			
95	SIMON	5	7/14
96	0°CLK RP	5	RP/J7
97	/XIDSTRTO	8	7/17
98	BWO	8	7/4
99	/XIDSTRT1	8	7/17
100	BW1	8	7/4

P2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO
1	XIDMSB	8	7/18
2	XIDINIT1	8	7/17
3	XIDINIT0	8	7/17
4	XIDINIT2	8	7/17
5	XIDINIT3	8	7/17
6	XIDINIT4	8	7/17
7	XIDINIT6	8	7/17
8	XIDINIT7	8	7/17
9	/ENABDWD	8	7/4
10			
11	S4	7	INT/3, 9/1
12			
13			
14			
15	NRZL	7	RP/J6
16	SIMNRZL	7	4/7
17	BND	7	7/4
18	/ENABWD	7	7/4
19	SERDATA	7	7/10
20	POLCTRL	7	7/12
21	PCM2	7	RP/J9
22	DGND	1	RP/J3
23	DGND	1	RP/J4
24			
25			
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46	DGND	1	RP/J8
47	-15V	1	7
48	+15V	1	7
49	+5V	1	7
50	DGND	1	7

P2

PIN NO.	MNEMONIC	PAGE	SIGNAL SOURCE OR DESTINATION ASSY NO / SCHEM SHEET NO.
51	FRCMP ID	8	7/9
52	XRIDEOSF	8	7/18
53	BN-1	8	7/4
54	/XIDMSB	8	7/18
55	XIDLNG0	8	7/17
56	XIDLNG1	8	7/17
57	XIDLNG3	8	7/17
58	XIDLNG2	8	7/17
59	XIDINIT5	8	7/17
60	/XIDUP	8	7/18
61	/LDIOGEN	8	7/12
62	/CLKIO3	8	7/12
63	IO1-8	8	7/12
64	IOL-9	8	7/12
65	IO1-9	8	7/12
66	CNTMSB	8	7/12
67			
68	XCODE0	7	7/15
69	XCODE1	7	7/15
70	XCODE2	7	7/15
71	XCODE3	7	7/15
72	DATA ENABLE	9	RP/J3
73	NOISE	9	RP/J4
74			
75			
76			
77			
78			
79			
80			
81			
82			
83			
84			
85			
86			
87			
88			
89			
90			
91			
92			
93			
94			
95			
96	PCM1	9	RP/J8
97	-15V	1	7
98	+15V	1	7
99	+5V	1	7
100	DGND	1	7

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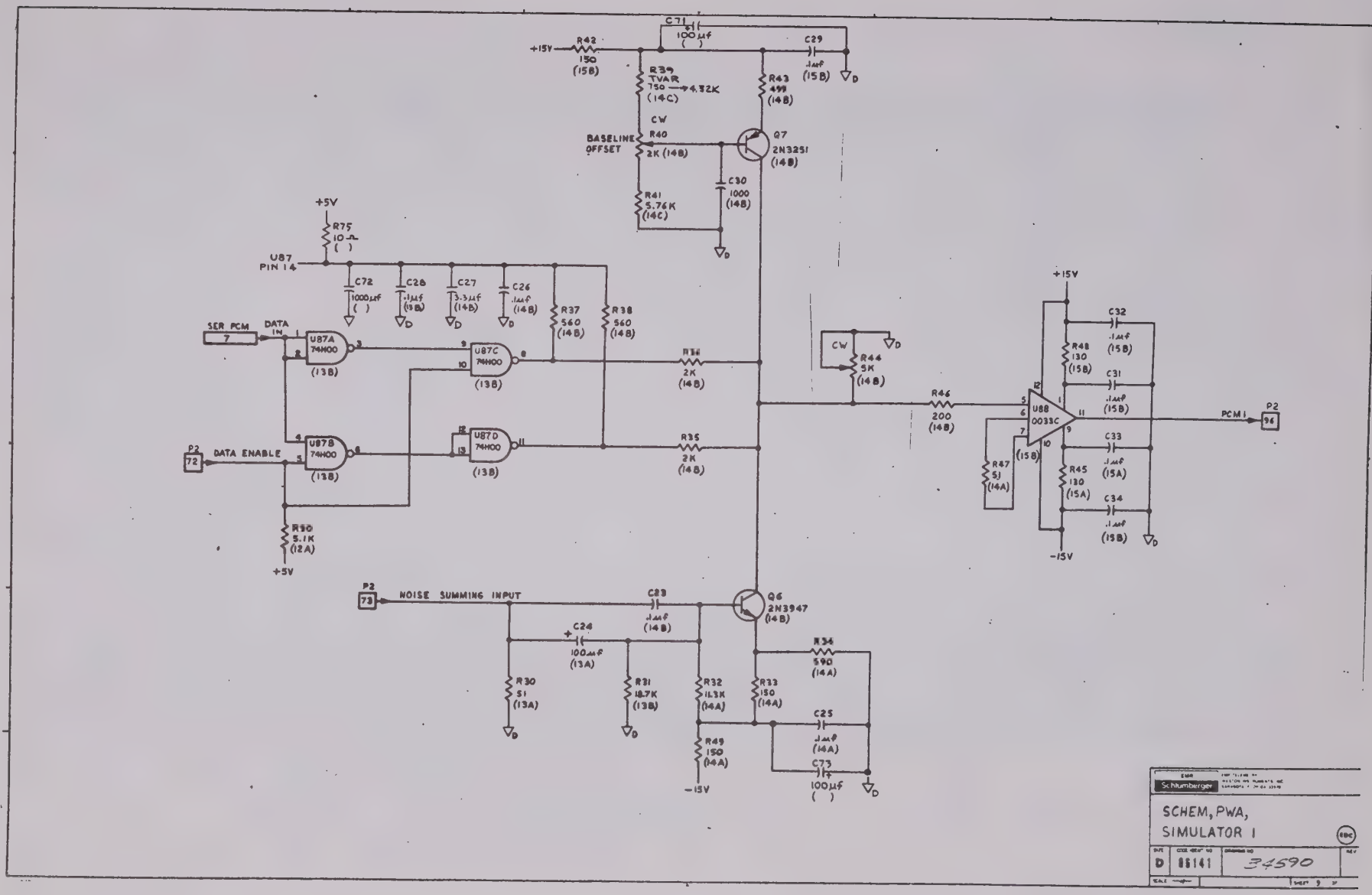
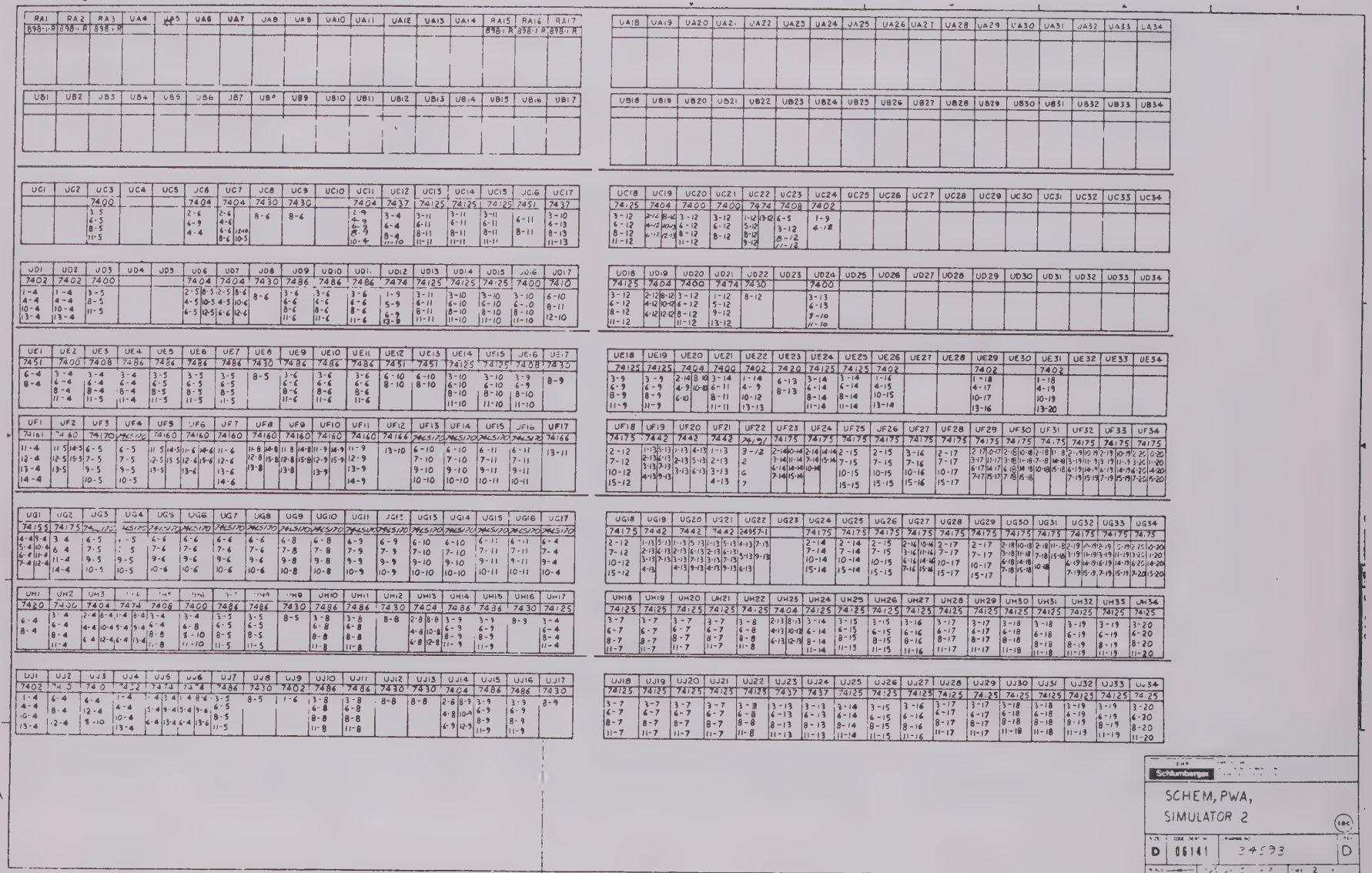
SCHEMATIC, PWA,
SIMULATOR I
FUNCTION #6

SIZE	CODE IDENT NO	DRAWING NO	REV
D	06141	34590	B

SHEET 10

6-118


+15V
R42 150 (15B)
C71 100µf ( )
C29 .1µf (15B)
R39 TVAR 750 → 4.32K (14C)
R43 499 (14B)
CW
BASELINE OFFSET
R40 2K (14B)
Q7 2N3251 (14B)
C30 1000 (14B)
R41 5.76K (14C)
+5V
R75 10Ω ( )
U87 PIN 14
C72 1000µf ( )
C28 .1µf (13B)
C27 3.3µf (14B)
C26 .1µf (14B)
R37 560 (14B)
R38 560 (14B)
SER PCM DATA IN
7
U87A 74H00
U87C 74H00
U87B 74H00
U87D 74H00
(13B)
R36 2K (14B)
R35 2K (14B)
P2 72
DATA ENABLE
R50 5.1K (12A)
+5V
CW
R44 5K (14B)
R46 200 (14B)
U88 0033C (15B)
R47 5J (14A)
R48 130 (15B)
R45 130 (15A)
C32 .1µf (15B)
C31 .1µf (15B)
C33 .1µf (15A)
C34 .1µf (15B)
+15V
-15V
PCM1
P2 96
P2 73
NOISE SUMMING INPUT
C23 .1µf (14B)
Q6 2N3947 (14B)
C24 100µf (13A)
R30 51 (13A)
R31 18.7K (13B)
R32 11.3K (14A)
R33 150 (14A)
R34 590 (14A)
C25 .1µf (14A)
R49 150 (14A)
C73 100µf ( )
-15V
Schlumberger
SCHEM, PWA, SIMULATOR 1
D
88141
34590


RA1 RA2 RA3 UA4 UA5 UA6 UA7 UA8 UB9 UA10 UA11 UA12 UA13 UA14 RA15 RA16 RA17
898-1 R 898-1 R 898-1 R 898-1 R 898-1 R 898-1 R
UA18 UA19 UA20 UA21 UA22 UA23 UA24 UA25 UA26 UA27 UA28 UA29 UA30 UA31 UA32 UA33 UA34
UB1 UB2 UB3 UB4 UB5 UB6 JB7 UB8 UB9 UB10 UB11 UB12 UB13 UB14 UB15 UB16 UB17
UB18 UB19 UB20 UB21 UB22 UB23 UB24 UB25 UB26 UB27 UB28 UB29 UB30 UB31 UB32 UB33 UB34
UC1 UC2 UC3 UC4 UC5 UC6 UC7 UC8 UC9 UC10 UC11 UC12 UC13 UC14 UC15 JC6 UC17
7400 7404 7404 7430 7430 7404 7437 74125 74125 74125 7451 7437
UC18 UC19 UC20 UC21 UC22 UC23 UC24 UC25 UC26 UC27 UC28 UC29 UC30 UC31 UC32 UC33 UC34
74125 7404 7400 7400 7474 7408 7402
UD1 UD2 UD3 UD4 UD5 UD6 UD7 UD8 UD9 UD10 UD11 UD12 UD13 UD14 UD15 UD16 UD17
7402 7402 7400 7404 7404 7430 7486 7486 7486 7474 74125 74125 74125 7400 7410
UD18 UD19 UD20 UD21 UD22 UD23 UD24 UD25 UD26 UD27 UD28 UD29 UD30 UD31 UD32 UD33 UD34
74125 7404 7400 7474 7430 7400
UE1 UE2 UE3 UE4 UE5 UE6 UE7 UE8 UE9 UE10 UE11 UE12 UE13 UE14 UE15 UE16 UE17
7451 7400 7408 7486 7486 7486 7486 7430 7486 7486 7486 7451 7451 74125 74125 7408 7430
UE18 UE19 UE20 UE21 UE22 UE23 UE24 UE25 UE26 UE27 UE28 UE29 UE30 UE31 UE32 UE33 UE34
74125 74125 7404 7400 7402 7420 74125 74125 7402 7402 7402
UF1 UF2 UF3 UF4 UF5 UF6 UF7 UF8 UF9 UF10 UF11 UF12 UF13 UF14 UF15 UF16 UF17
74181 74 60 74170 74S170 74160 74160 74160 74160 74160 74160 74166 74S170 74S170 74S170 74S32 74166
UF18 UF19 UF20 UF21 UF22 UF23 UF24 UF25 UF26 UF27 UF28 UF29 UF30 UF31 UF32 UF33 UF34
74175 7442 7442 7442 74S9/ 74175 74175 74175 74175 74175 74175 74175 74175 74175 74175 74175 74175
UG1 UG2 UG3 UG4 UG5 UG6 UG7 UG8 UG9 UG10 UG11 UG12 UG13 UG14 UG15 UG16 UG17
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UG18 UG19 UG20 UG21 UG22 UG23 UG24 UG25 UG26 UG27 UG28 UG29 UG30 UG31 UG32 UG33 UG34
74175 7442 7442 7442 24957-1 74175 74175 74175 74175 74175 74175 74175 74175 74175 74175 74175 74175
UH1 UH2 UH3 UH4 UH5 UH6 UH7 UH8 UH9 UH10 UH11 UH12 UH13 UH14 UH15 UH16 UH17
7420 7430 7404 7474 7408 7400 7486 7486 7430 7486 7486 7430 7404 7486 7436 7430 74125
UH18 UH19 UH20 UH21 UH22 UH23 UH24 UH25 UH26 UH27 UH28 UH29 UH30 UH31 UH32 UH33 UH34
74125 74125 74125 74125 74125 7404 74125 74125 74125 74125 74125 74125 74125 74125 74125 74125 74125
UJ1 UJ2 UJ3 UJ4 UJ5 UJ6 UJ7 UJ8 UJ9 UJ10 UJ11 UJ12 UJ13 UJ14 UJ15 UJ16 UJ17
7403 74 0 74 0 7432 7474 74 4 7486 7430 7402 7486 7486 7430 7430 7404 7486 7486 7430
UJ18 UJ19 UJ20 UJ21 UJ22 UJ23 UJ24 UJ25 UJ26 UJ27 UJ28 UJ29 UJ30 UJ31 UJ32 UJ33 UJ34
74125 74125 74125 74125 74125 7437 7437 74125 74125 74125 74125 74.25 74125 74125 74125 74125 74.25
Schlumberger
SCHEM, PWA,
SIMULATOR 2
D 06141 34593 D

6-120

[illegible] COMPONENT CHART	
[illegible]	[illegible] NUMBER
TP 67	TP1 THRU TP3, TP5-TP49, TP59-TP66
RA17	RA4 THRU RA14
UC 24	UC 1,2,4,5,10.
UD 24	UD 4,5,23.
UE 31	UE 27,28,30.
UF 34	UF 22
UG 34	UG 23
UH 34	
UJ 34	
C136	
F2	

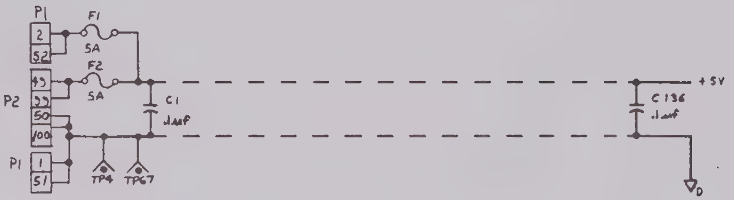
UNUSED CIRCUITS		
REF DES	TYPE	UNUSED CIRCUITS
RA2	898-1-R	H,J
RA3	898-1-R	H,J,N,P,R
RA15	898-1-R	G,H,J,R
RA16	898-1-R	H,J
RA17	898-1-R	H,J
UC6	7404	D,E,F
UC21	7400	D
UC24	7402	D
UD3	7400	B
UE20	7404	F
UJ9	7402	B,C,D
UC11	7404	F

POWER PINS			POWER PINS			POWER PINS			POWER PINS		
REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND
UC3	14	7	UD21	14	7	UF7	16	8	UG11	16	8
UC6	14	7	UD22	14	7	UF8	16	8	UG12	16	8
UC7	14	7	UD24	14	7	UF9	16	8	UG13	16	8
UC8	14	7	UE1	14	7	UF10	16	8	UG14	16	8
UC9	14	7	UE2	14	7	UF11	16	8	UG15	16	8
UC11	14	7	UE3	14	7	UF12	16	8	UG16	16	8
UC12	14	7	UE4	14	7	UF13	16	8	UG17	16	8
UC13	14	7	UE5	14	7	UF14	16	8	UG18	16	8
UC14	14	7	UE6	14	7	UF15	16	8	UG19	16	8
UC15	14	7	UE7	14	7	UF16	16	8	UG20	16	8
UC16	14	7	UE8	14	7	UF17	16	8	UG21	16	8
UC17	14	7	UE9	14	7	UF18	16	8	UG22	16	8
UC18	14	7	UE10	14	7	UF19	16	8	UG24	16	8
UC19	14	7	UE11	14	7	UF20	16	8	UG25	16	8
UC20	14	7	UE12	14	7	UF21	16	8	UG26	16	8
UC21	14	7	UE13	14	7	UF23	16	8	UG27	16	8
UC22	14	7	UE14	14	7	UF24	16	8	UG28	16	8
UC23	14	7	UE15	14	7	UF25	16	8	UG29	16	8
UC24	14	7	UE16	14	7	UF26	16	8	UG30	16	8
UD1	14	7	UE17	14	7	UF27	16	8	UG31	16	8
UD2	14	7	UE18	14	7	UF28	16	8	UG32	16	8
UD3	14	7	UE19	14	7	UF29	16	8	UG34	16	8
UD6	14	7	UE20	14	7	UF30	16	8	UH1	14	7
UD7	14	7	UE21	14	7	UF31	16	8	UH2	14	7
UD8	14	7	UE22	14	7	UF32	16	8	UH3	14	7
UD9	14	7	UE23	14	7	UF33	16	8	UH4	14	7
UD10	14	7	UE24	14	7	UF34	16	8	UH5	14	7
UD11	14	7	UE25	14	7	UG1	16	8	UH6	14	7
UD12	14	7	UE26	14	7	UG2	16	8	UH7	14	7
UD13	14	7	UE29	14	7	UG3	16	8	UH8	14	7
UD14	14	7	UE31	14	7	UG4	16	8	UH9	4	7
UD15	14	7	UF1	16	8	UG5	16	8	UH10	14	7
UD16	14	7	UF2	16	8	UG6	16	8	UH11	14	7
UD17	14	7	UF3	16	8	UG7	16	8	UH12	14	7
UD18	14	7	UF4	16	8	UG8	16	8	UH13	14	7
UD19	14	7	UF5	16	8	UG9	16	8	UH14	14	7
UD20	14	7	UF6	16	8	UG10	16	8	UH15	14	7

POWER PINS			POWER PINS			POWER PINS			POWER PINS		
REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND	REF DES	+5V	GND
UH16	14	7	UJ19	14	7						
UH17	14	7	UJ20	14	7						
UH18	14	7	UJ21	14	7						
UH19	14	7	UJ22	14	7						
UH20	14	7	UJ23	14	7						
UH21	14	7	UJ24	14	7						
UH22	14	7	UJ25	14	7						
UH23	14	7	UJ26	14	7						
UH24	4	7	UJ27	14	7						
UH25	14	7	UJ28	14	7						
UH26	14	7	UJ29	14	7						
UH27	14	7	UJ30	14	7						
UH28	14	7	UJ31	14	7						
UH29	14	7	UJ32	14	7						
UH30	14	7	UJ33	14	7						
UH31	14	7	UJ34	14	7						
UH32	14	7	UF22	16	8						
UH33	14	7									
UH34	14	7									
UJ1	14	7									
UJ2	14	7									
UJ3	14	7									
UJ4	14	7									
UJ5	14	7									
UJ6	14	7									
UJ7	14	7									
UJ8	14	7									
UJ9	14	7									
UJ10	4	7									
UJ11	14	7									
UJ12	14	7									
UJ13	14	7									
UJ14	14	7									
UJ15	14	7									
UJ16	14	7									
UJ17	14	7									
UJ18	14	7									

ARTWORK REVISION INDEX

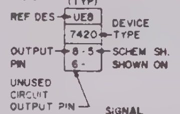
REVISIONS				
LTR	DESCRIPTION	[illegible]	DATE	[illegible]
A	UPDATE [illegible] SHTS [illegible] 21	[illegible]	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]	[illegible]
C	ECO 57[illegible]	[illegible]	8-29-78	[illegible]
D	ECO 57398 UPDATED SHTS [illegible] ADDED	[illegible]	9-19-78	[illegible]
E	ECO 57708 ADD UC24C SHT 9 [illegible]	[illegible]	12-14-78	[illegible]



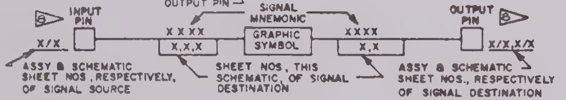
8 NOTES CONTINUED ON SHEET 21.

7 THIS DWG IS COMPLETE WITH SHEETS 1 THRU 21 & 3A & 3B.

6. ON SHEET 2



8. ADDRESS DEFINITION:



4. CHARACTERS IN PARENTHESES NEAR REFERENCE DESIGNATORS IDENTIFY THE SECTION OF THE ASSEMBLY WHERE THE PART IS LOCATED.

3 CIRCUIT RETURN SYMBOLS: —▷A ANALOG GND, —▷D DIGITAL GND.

2 FOR TOLERANCES AND RATINGS, SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS.

UNLESS OTHERWISE SPECIFIED:

NOTES

[illegible]	BASIC	CONTROL NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	ITEM OR SYMBOL
CONFIGURATION					
QTY REQUIRED	PARTS LIST				

BSC 34594 7/C-02

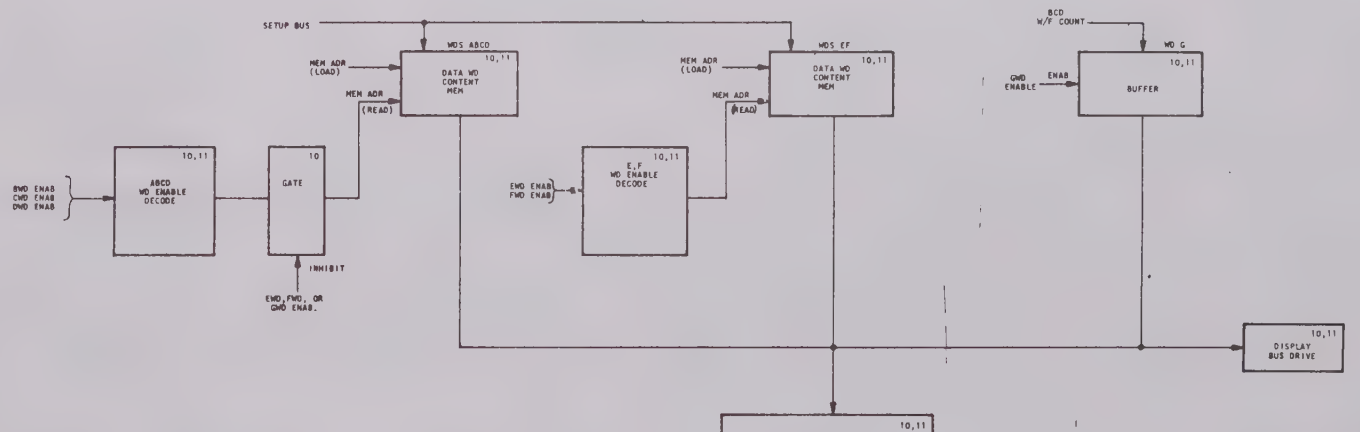
UNLESS OTHERWISE SPECIFIED

DRAWN BY C FASO 6-24-77

Schlumberger

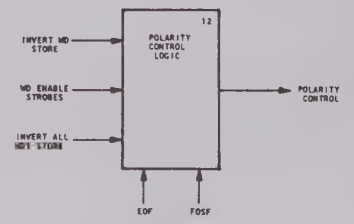
SCHEM, PWA, SIMULATOR 2 (FUNCTION # 7)

D 06141 34593 E



DATA STORE AND PARALLEL/SERIAL CONVERSION

EOF AND EOSF GENERATION



POLARITY CONTROL GENERATION

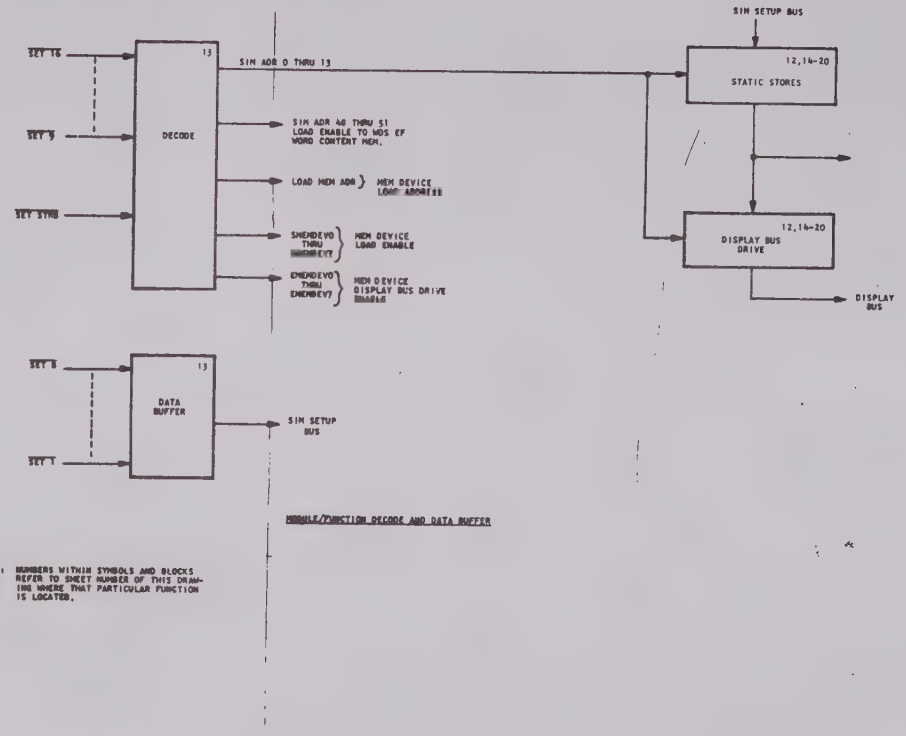
NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

Schlumberger

SCHEMATIC, PWA
SIMULATOR 2

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	06141	34593	

SCALE — SHEET 2 OF



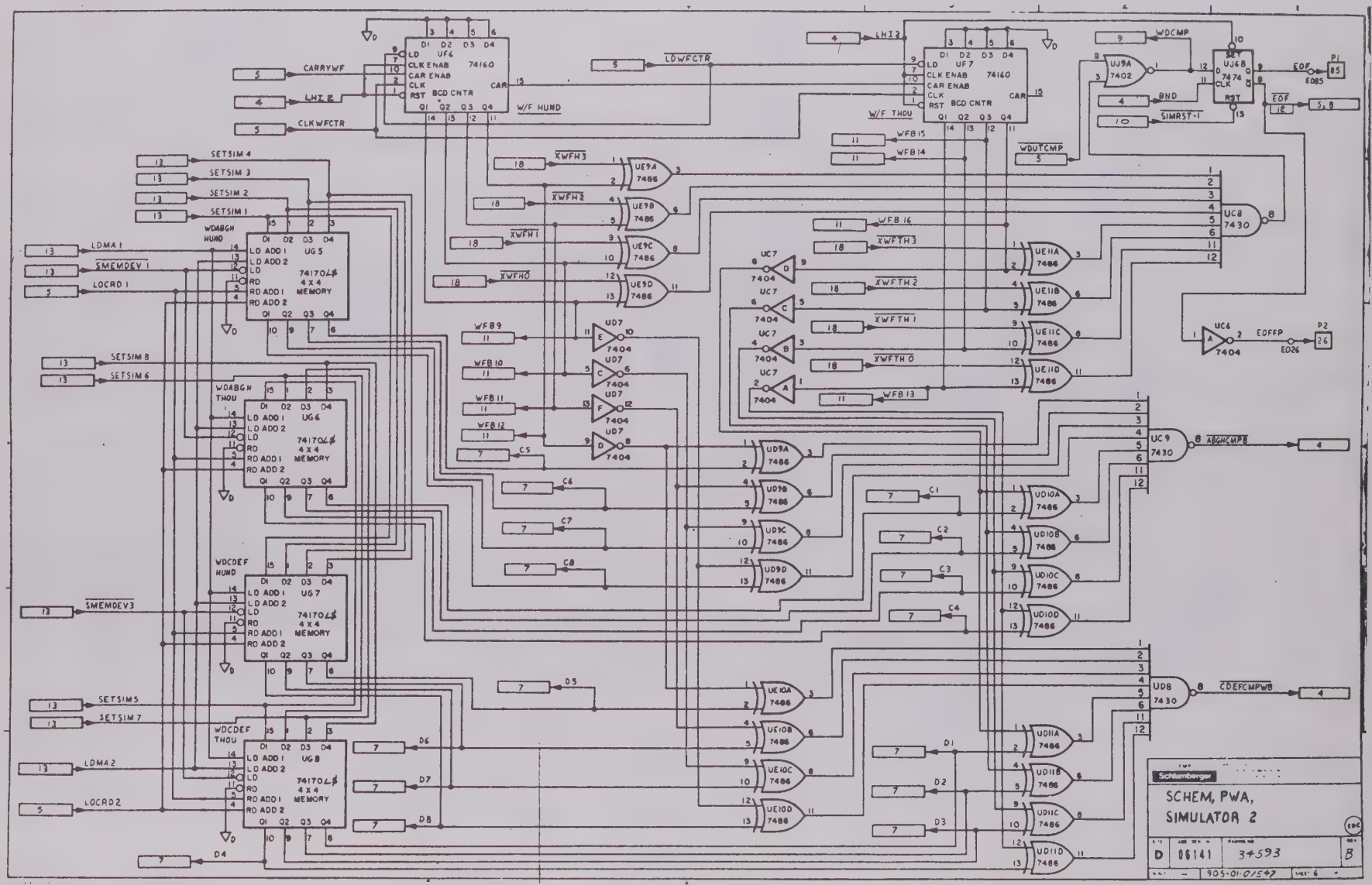
MODULE/FUNCTION DECODE AND DATA BUFFER

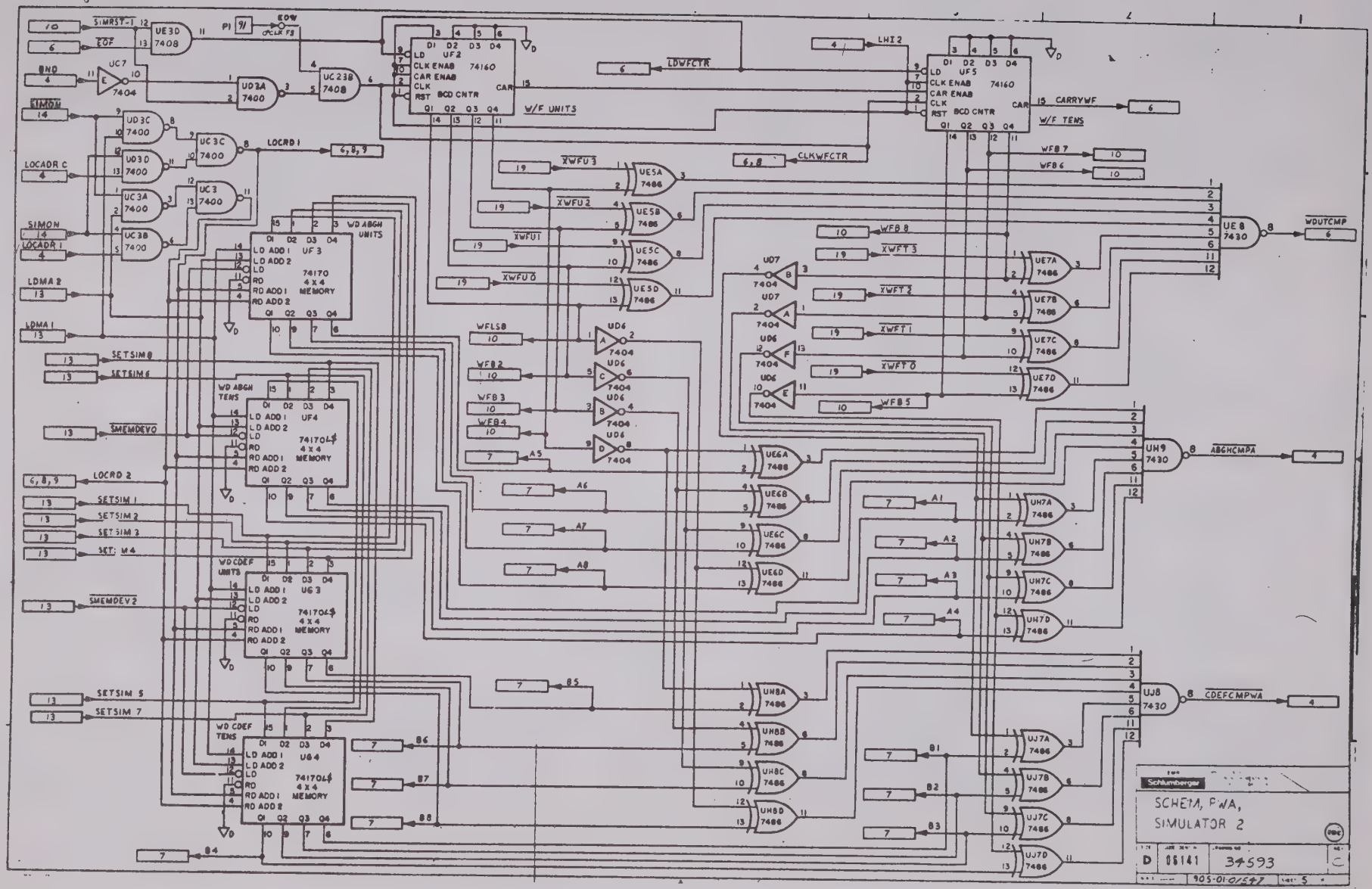
NOTE: NUMBERS WITHIN SYMBOLS AND BLOCKS REFER TO SHEET NUMBER OF THIS DRAWING WHERE THAT PARTICULAR FUNCTION IS LOCATED.

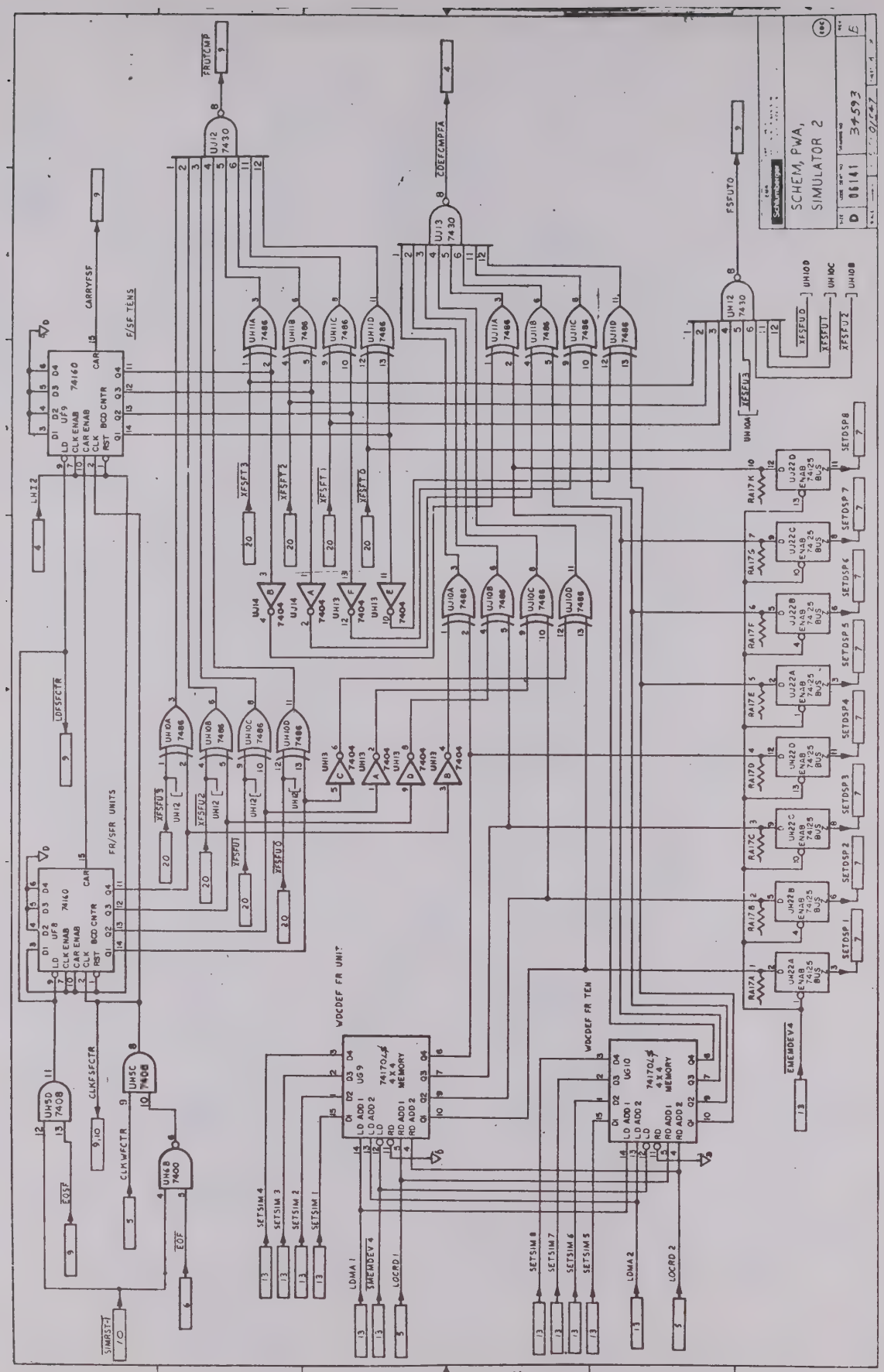
SCHEMATIC, PWA
SIMULATOR 2

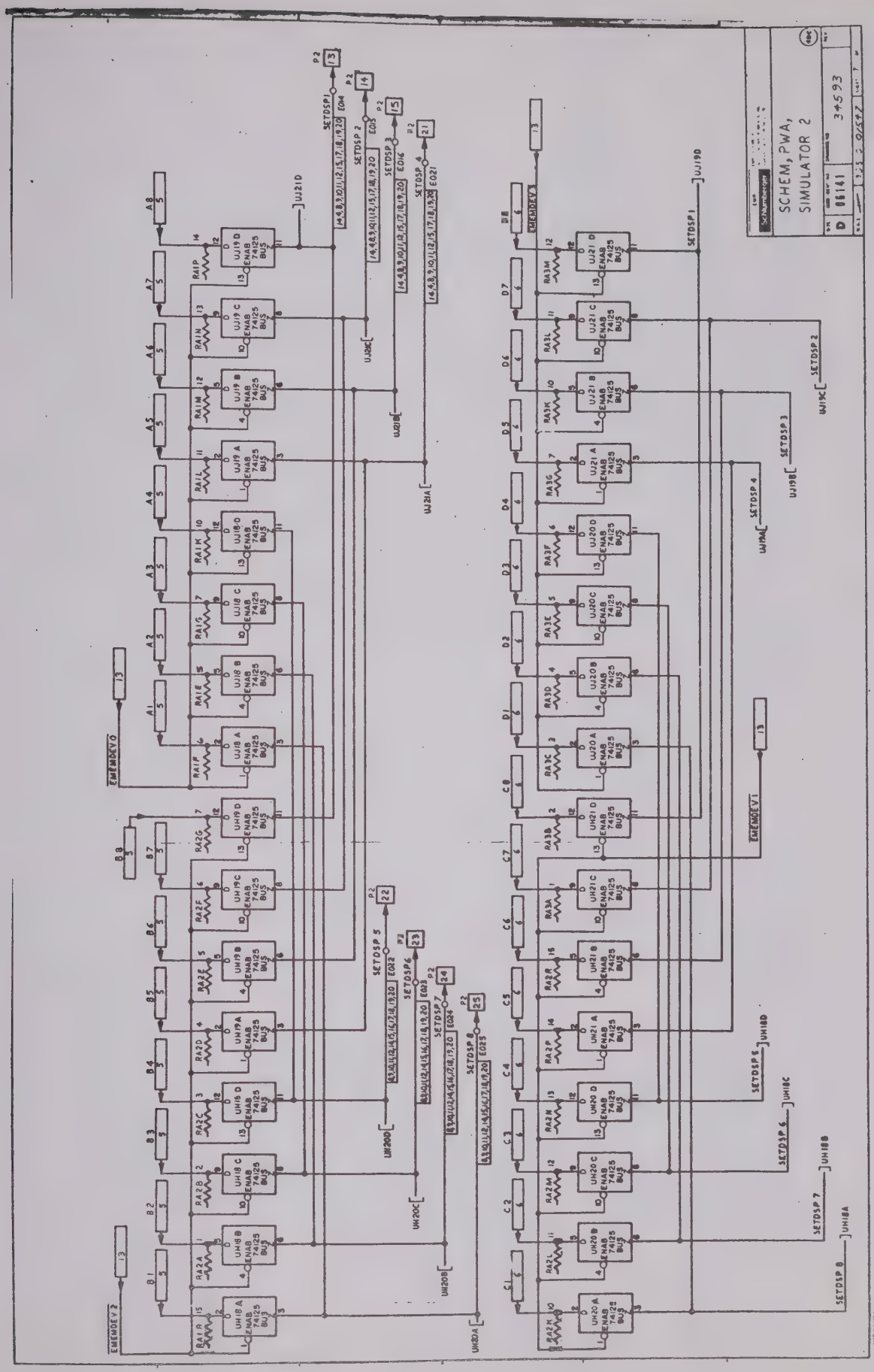
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	88141	34593	

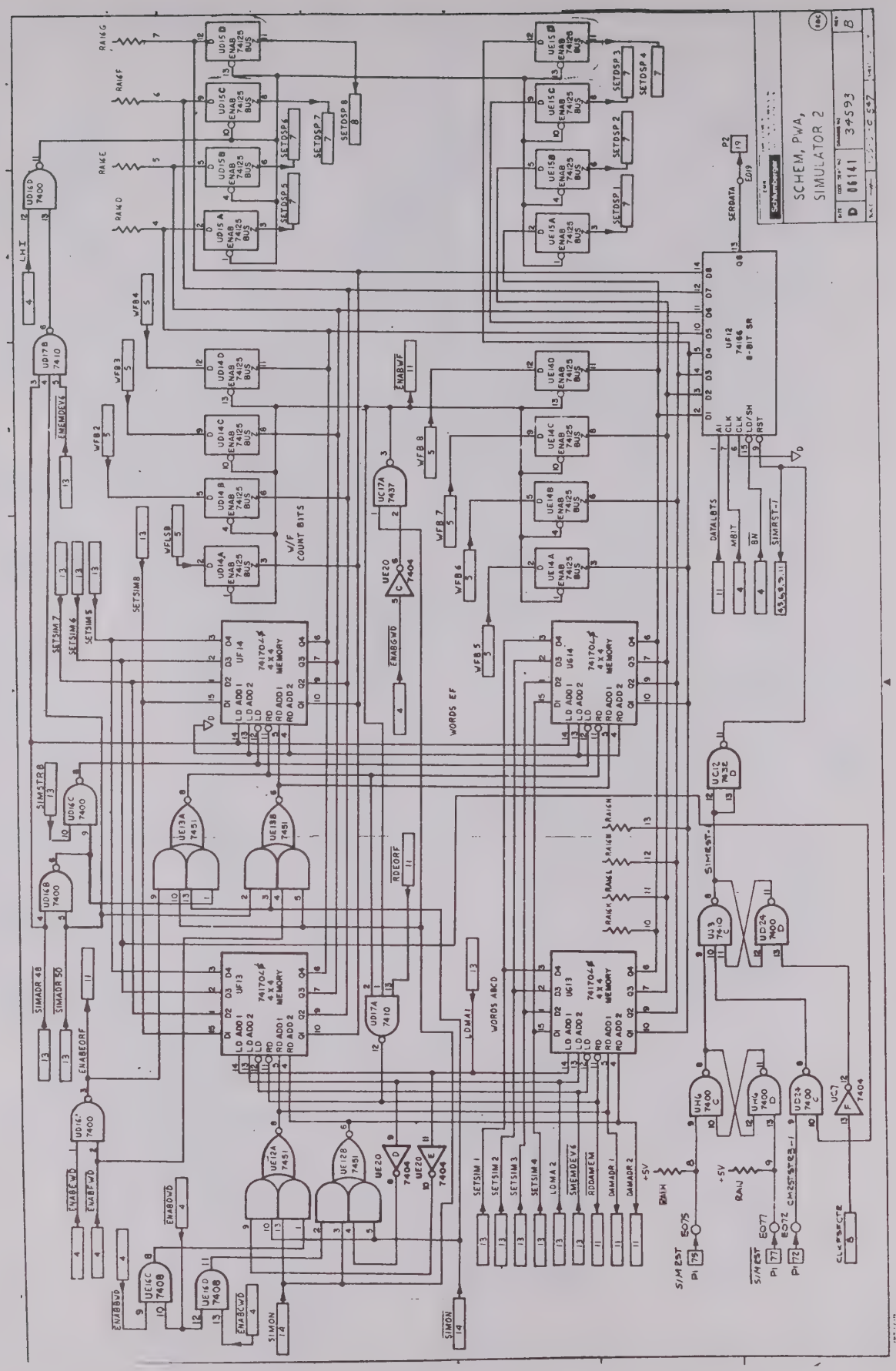
SCALE —/— SHEET 36 OF

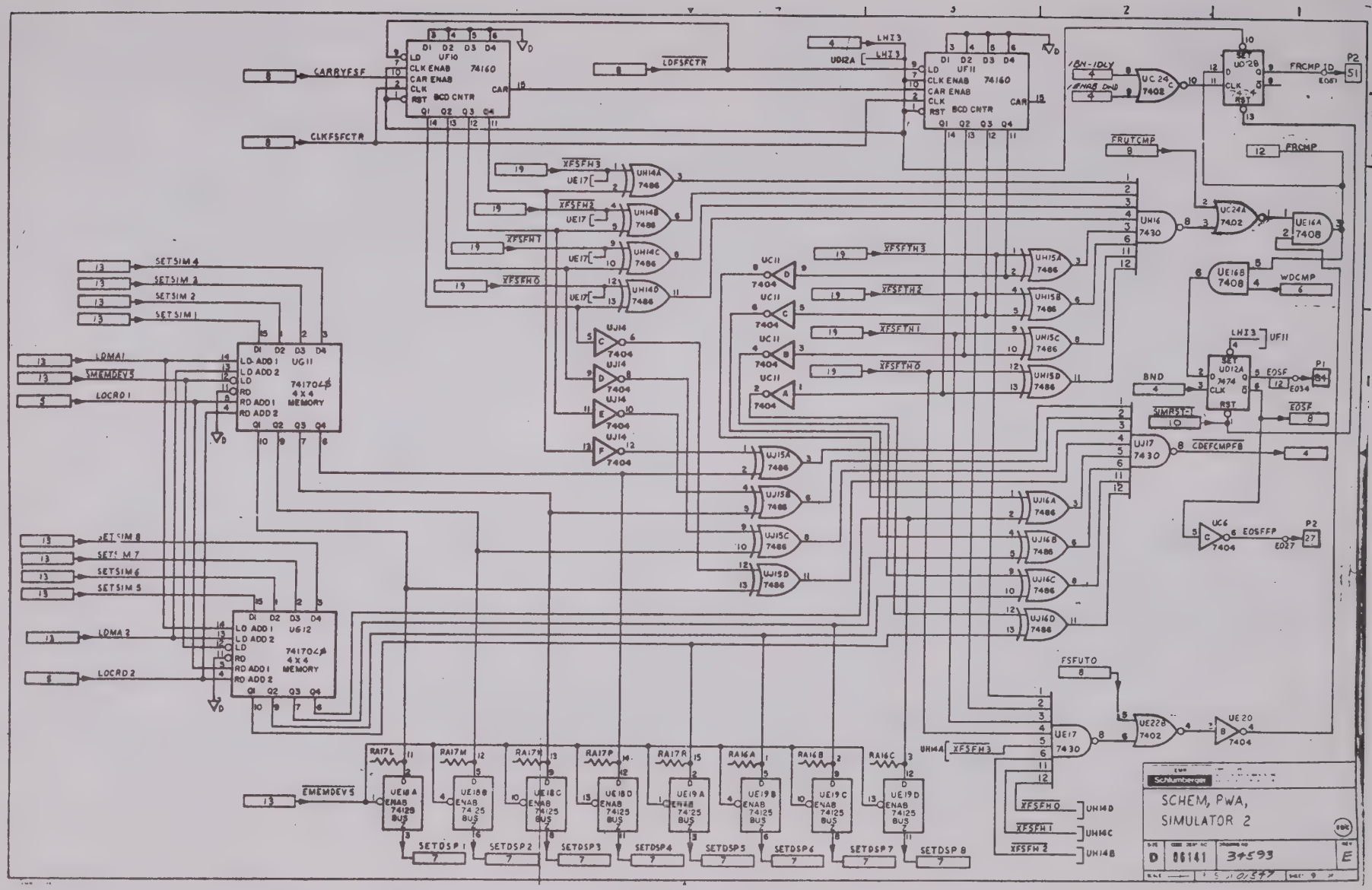

UF6 74160
UF7 74160
CLK ENAB
CAR ENAB
RST BCD CNTR
CARRYWF
LHI2
CLKWFCTR
LDWFCTR
W/F HUND
W/F THOU
WDCMP
WDOUTCMP
EOF
EOB5
SIMRST-1
SETSIM 4
SETSIM 3
SETSIM 2
SETSIM 1
WDABGH HUND
UG5
LDMA1
SMEMDEV1
LOCRD1
74170L$ 4X4 MEMORY
SETSIM 8
SETSIM 6
WDABGH THOU
UG6
WDCDEF HUND
UG7
SMEMDEV3
SETSIM5
SETSIM 7
WDCDEF THOU
UG8
LDMA2
LOCRD2
XWFH3
XWFH2
XWFH1
XWFH0
XWFTH3
XWFTH2
XWFTH1
XWFTH0
WFB15
WFB14
WFB16
WFB13
WFB9
WFB10
WFB11
WFB12
UC8 7430
UC6 7404
EOFFP
EOB6
UC9 7430
ABGHCMPWB
UD8 7430
CDEFCMPWB
C1
C2
C3
C4
C5
C6
C7
C8
D1
D2
D3
D4
D5
D6
D7
D8
Schlumberger
SCHEM, PWA, SIMULATOR 2
D
06141
34593
B
905-01-01547

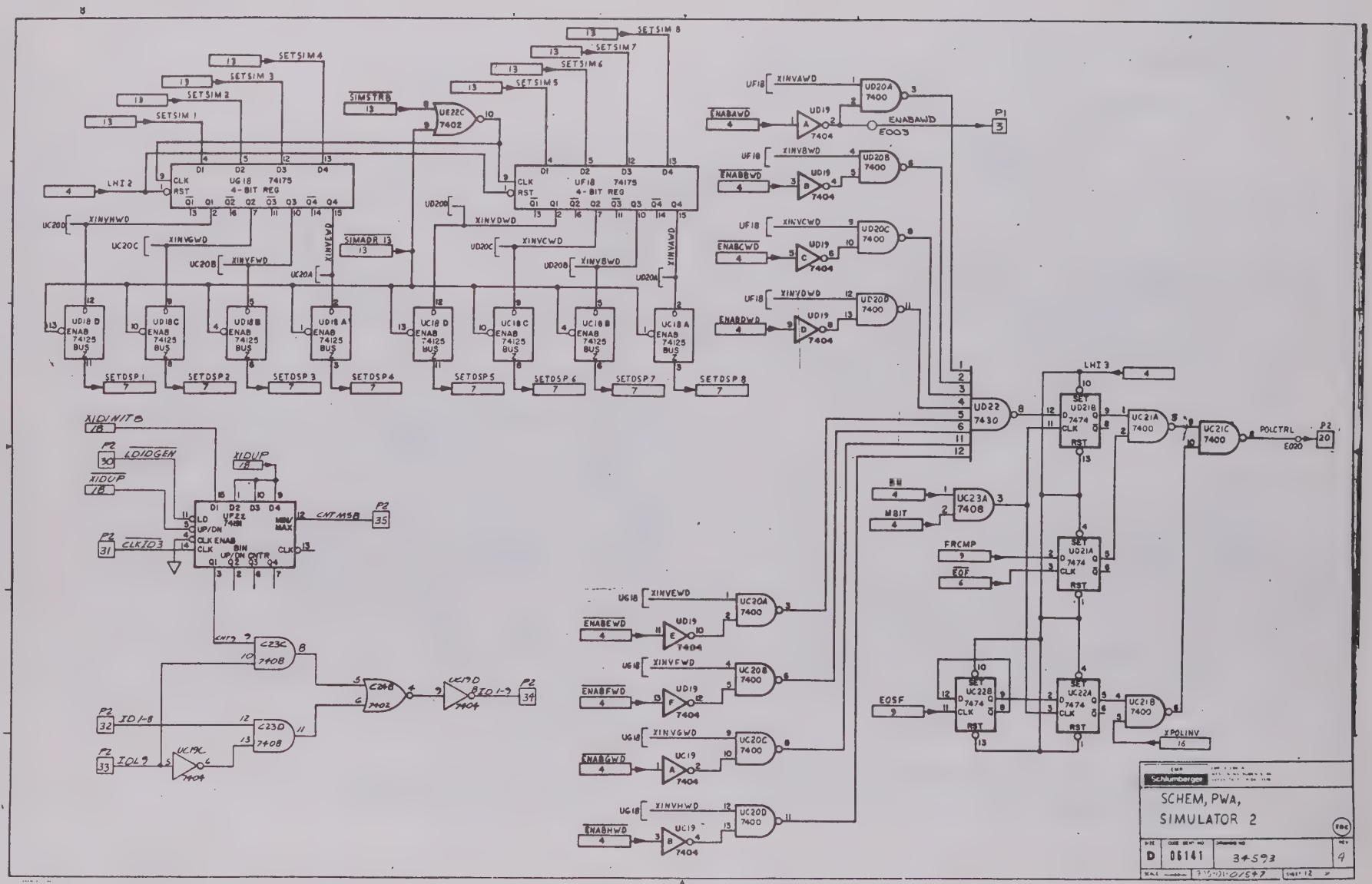

SIMRST-1
EOF
BND
SIMON
LOCADR C
LOCADR I
LDMA 2
LDMA 1
SETSIM 8
SETSIM 6
SMEMDEV0
LOCRD 2
SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
SMEMDEV2
SETSIM 5
SETSIM 7
EOW
W/F UNITS
W/F TENS
LDWFCTR
CLKWFCTR
LWI2
CARRYWF
LOCRD 1
WD ABGH UNITS
WD ABGH TENS
WD CDEF UNITS
WD CDEF TENS
WDUTCMP
ABGHCMPA
CDEFCMPWA
SCHEMA, PWA, SIMULATOR 2
D
06141
34593
905-01-0547

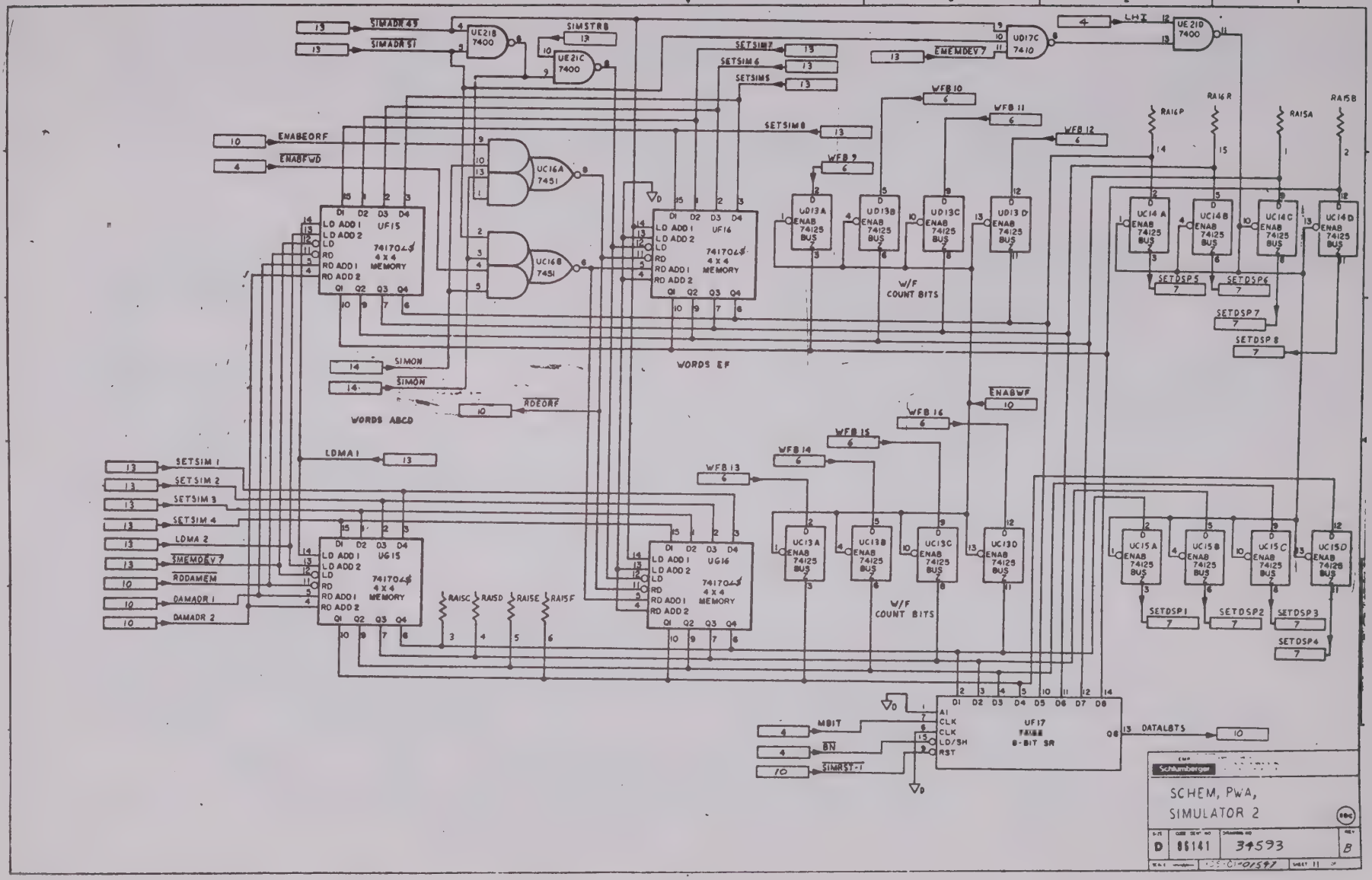

SCHEM, PWA,
SIMULATOR 2
D 06141 34593
E
F/SF TENS
FR/SFR UNITS
WDCDEF FR UNIT
WDCDEF FR TEN
CARRYFSF
FRUTCMP
CDEFCMPFA
FSFUTO
LDFSFCTR
CLKFSFCTR
CLKWFCTR
EOSF
EOF
SIMRST-1
SETSIM 4
SETSIM 3
SETSIM 2
SETSIM 1
SETSIM 8
SETSIM 7
SETSIM 6
SETSIM 5
LDMA 1
SMEMDEV 4
LOCRD 1
LDMA 2
LOCRD 2
EMEMDEV4
SETDSP 1
SETDSP 2
SETDSP 3
SETDSP 4
SETDSP 5
SETDSP 6
SETDSP 7
SETDSP 8

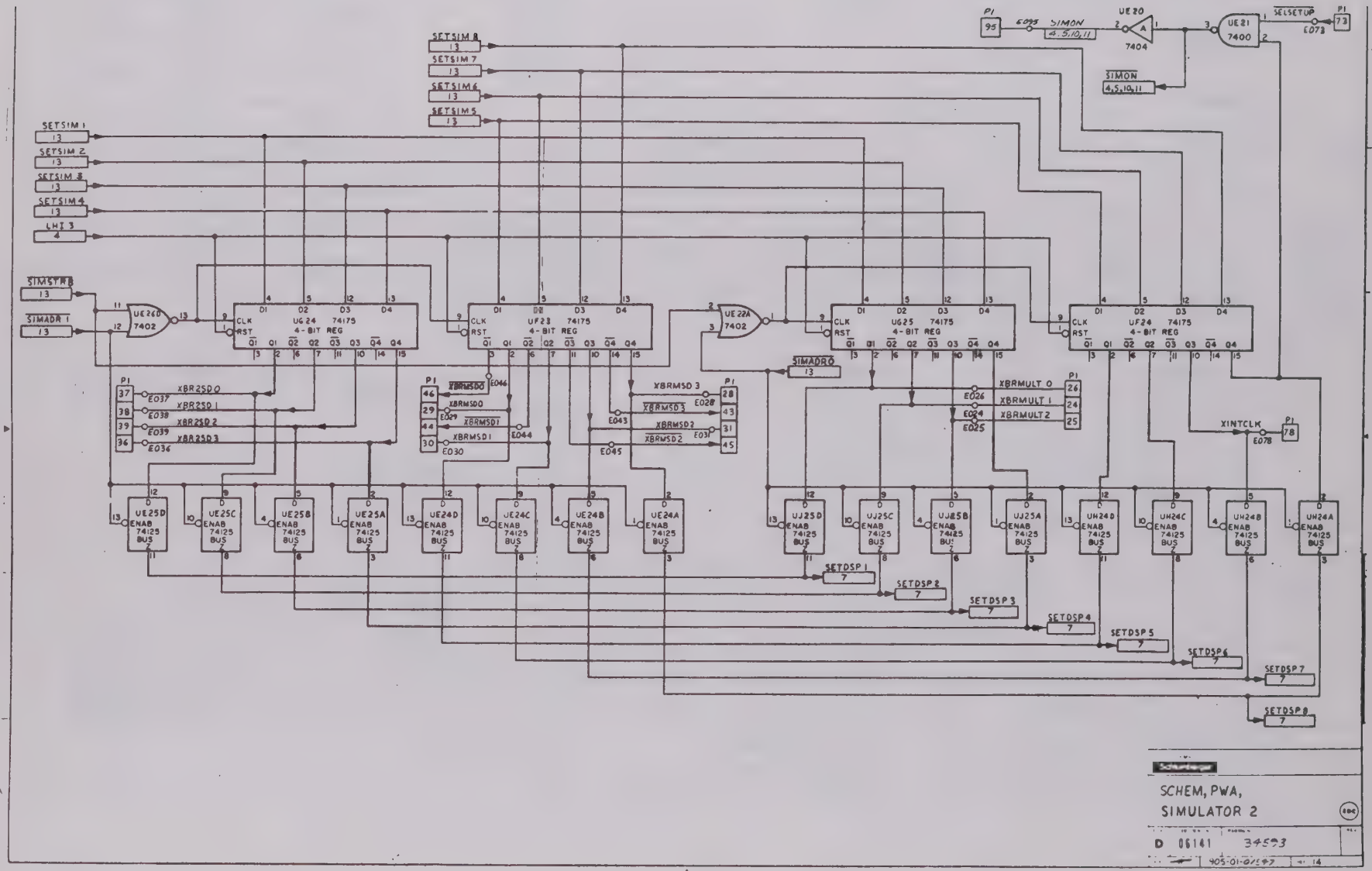

SCHEM, PWA,
SIMULATOR 2
34593
D 06141

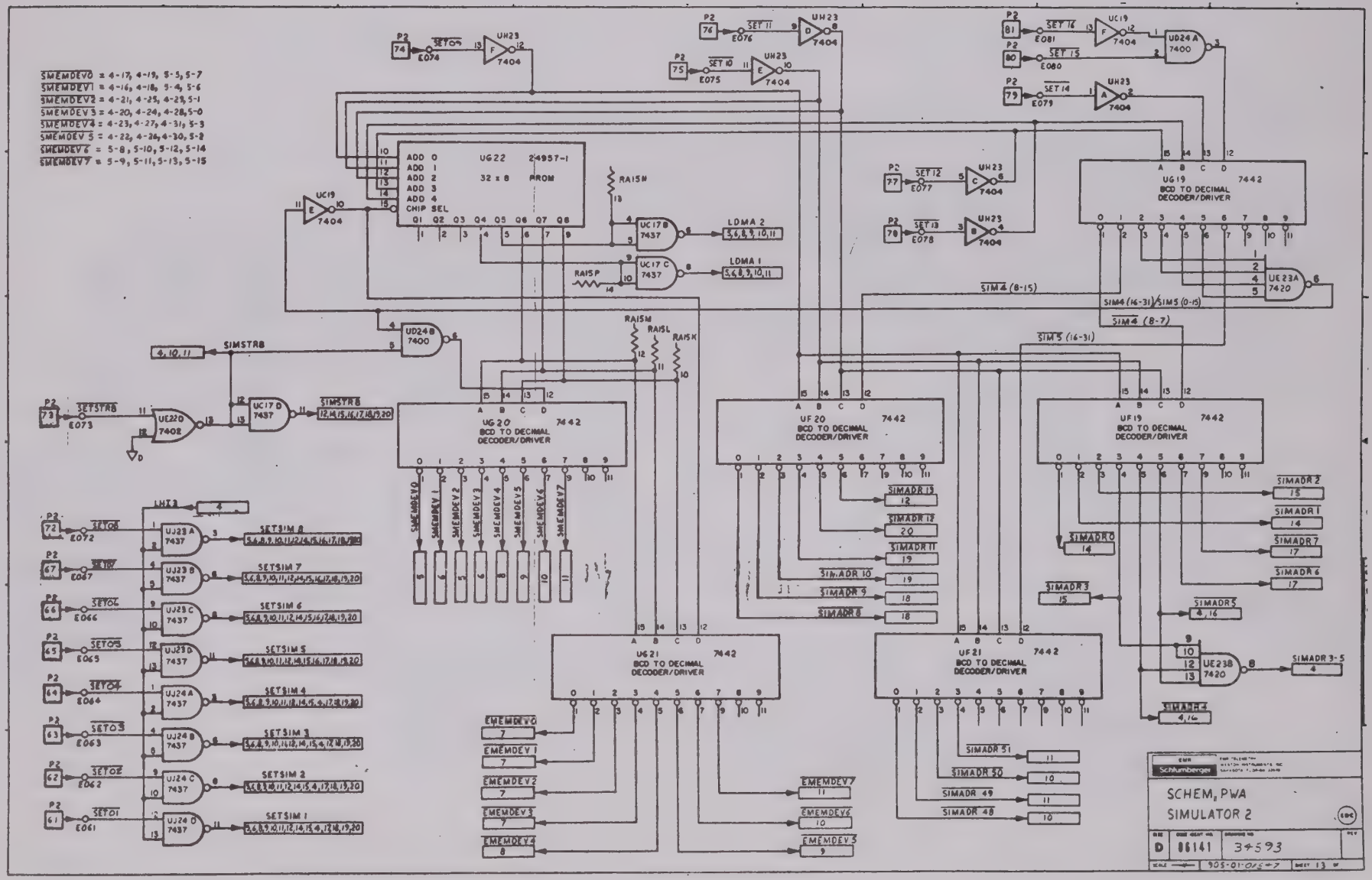

SCHEM, PWA,
SIMULATOR 2
D 06141 34593 B
UF12 74166 8-BIT SR
UF14 74170 4 X 4 MEMORY
UF13 74170 4 X 4 MEMORY
UG14 74170 4 X 4 MEMORY
UG13 74170 4 X 4 MEMORY
UE15A ENAB 74125 BUS
UE15B ENAB 74125 BUS
UE15C ENAB 74125 BUS
UE15D ENAB 74125 BUS
UE14A ENAB 74125 BUS
UE14B ENAB 74125 BUS
UE14C ENAB 74125 BUS
UE14D ENAB 74125 BUS
UE13A 7451
UE13B 7451
UE12A 7451
UE12B 7451
UE16C 7408
UE16D 7408
UD16A 7400
UD16B 7400
UD16C 7400
UD16D 7400
UD17A 7410
UD17B 7410
UC17A 7437
UC12 7432
UJ3 7410
UD24 7400
UH6 7400
UC7 7404
UE20 7404
W/F COUNT BITS
WORDS EF
WORDS ABCD
SERDATA
DATALBTS
MBIT
BN
SIMRST-1
SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
LDMA 2
SMEMDEV6
RDDAMEM
DAMADR 1
DAMADR 2
SIMON
SIMSTR8
SIMADR 48
SIMADR 50
ENABEORF
ENABFWD
ENABDWD
ENABCWD
ENABBWD
ENABGWD
ENABWF
RDEORF
LDMA1
SETDSP 1
SETDSP 2
SETDSP 3
SETDSP 4
SETDSP 5
SETDSP 6
SETDSP 7
SETDSP 8
SETSIM 5
SETSIM 6
SETSIM 7
SETSIM 8
ENAB 74125 BUS
RA16 A
RA16 B
RA16 C
RA16 D
RA16 E
RA16 F
RA16 G
RA16 H
RA16 J
RA16 K
RA16 L
RA16 M
RA16 N
+5V
RAIN
S/MRST
CLKFSFCTR
CM2STSTR3-1
P1
P2
E075
E077
E072
E019

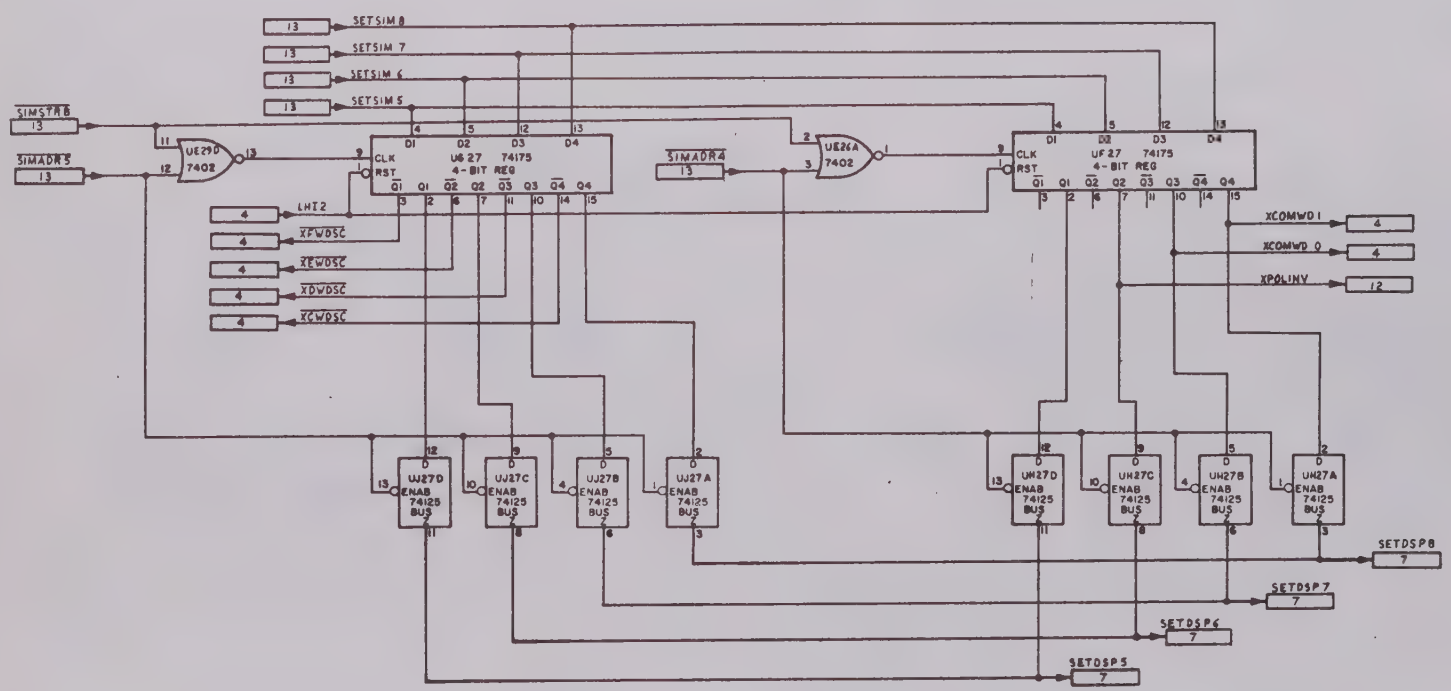

CARRYFSF
CLKFSFCTR
LDFSFCTR
SETSIM4
SETSIM3
SETSIM2
SETSIM1
LDMA1
SMEMDEV5
LOCAD1
SETSIM8
SETSIM7
SETSIM6
SETSIM5
LDMA2
LOCAD2
EMEMDEV5
XFSFH3
XFSFH2
XFSFH1
XFSFH0
XFSFTH3
XFSFTH2
XFSFTH1
XFSFTH0
FRUTCMP
FRCMP
WDCMP
BND
SYNRST
CDEFCMPFB
EOSF
EOSFFP
FSFUTO
SETDSP1
SETDSP2
SETDSP3
SETDSP4
SETDSP5
SETDSP6
SETDSP7
SETDSP8
SCHEM, PWA,
SIMULATOR 2
D
86141
34593
E


SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
SETSIM 5
SETSIM 6
SETSIM 7
SETSIM 8
SIMSTRB
UE22C 7402
LHI 2
UG18 74175 4-BIT REG
UF18 74175 4-BIT REG
XINVHWD
XINVGWD
XINVFWD
XINVEWD
XINVDWD
XINVCWD
XINVBWD
XINVAWD
SIMADR 13
UC20D
UC20C
UC20B
UC20A
UD18 D ENAB 74125 BUS
UD18C ENAB 74125 BUS
UD18B ENAB 74125 BUS
UD18A ENAB 74125 BUS
UC18 D ENAB 74125 BUS
UC18C ENAB 74125 BUS
UC18B ENAB 74125 BUS
UC18A ENAB 74125 BUS
SETDSP1
SETDSP2
SETDSP3
SETDSP4
SETDSP5
SETDSP6
SETDSP7
SETDSP8
UF18
ENABAWD
ENABBWD
ENABCWD
ENABDWD
UD19 7404
UD20A 7400
UD20B 7400
UD20C 7400
UD20D 7400
ENABAWD
E003
P1
3
UD22 7430
LHI 3
UD21B 7474
UC21A 7400
UC21C 7400
POLCTRL
E020
P2
20
BIT
MBIT
UC23A 7408
FRCMP
EOF
UD21A 7474
EOSF
UC22B 7474
UC22A 7474
UC21B 7400
XPOLINV
16
XIDINIT8
XIDUP
LDIDGEN
CLKID3
UF22 7469
CNTMSB
P2
35
UC23C 7408
UC23D 7408
UC24B 7402
UC19D 7404
ID1-3
34
ID1-8
32
ID4
33
UC19C 7404
UG18
ENABEWD
ENABFWD
ENABGWD
ENABHWD
UC19 7404
Schlumberger
SCHEM, PWA,
SIMULATOR 2
D
06141
34593
4


SIMADR 45
SIMADR 51
UE21B 7400
SIMSTRB
UE21C 7400
SETSIM7
SETSIM6
SETSIM5
SETSIM8
EMEMDEV7
UD17C 7410
LHI
UE21D 7400
WFB 10
WFB 11
WFB 12
WFB 9
RA16P
RA16R
RA15A
RA15B
ENABEORF
ENABFWD
UC16A 7451
UC16B 7451
UF15
UF16
7417045 4 X 4 MEMORY
UD13A ENAB 74125 BUS
UD13B ENAB 74125 BUS
UD13C ENAB 74125 BUS
UD13D ENAB 74125 BUS
W/F COUNT BITS
UC14A ENAB 74125 BUS
UC14B ENAB 74125 BUS
UC14C ENAB 74125 BUS
UC14D ENAB 74125 BUS
SETDSP5
SETDSP6
SETDSP7
SETDSP8
WORDS EF
SIMON
SIMON
WORDS ABCD
RDEORF
ENABWF
WFB 16
WFB 15
WFB 14
WFB 13
LDMA 1
SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
LDMA 2
SMEMDEV7
RDDAMEM
DAMADR 1
DAMADR 2
UG15
UG16
RAISC
RAISD
RAISE
RAISF
UC13A ENAB 74125 BUS
UC13B ENAB 74125 BUS
UC13C ENAB 74125 BUS
UC13D ENAB 74125 BUS
W/F COUNT BITS
UC15A ENAB 74125 BUS
UC15B ENAB 74125 BUS
UC15C ENAB 74125 BUS
UC15D ENAB 74125 BUS
SETDSP1
SETDSP2
SETDSP3
SETDSP4
UF17 74688 8-BIT SR
MBIT
BN
SIMRST-1
DATALBTS
SCHEM, PWA, SIMULATOR 2
D
86141
34593
B


SETSIM 8
SETSIM 7
SETSIM 6
SETSIM 5
SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
LHI 3
SIMSTRB
SIMADR 1
SIMADR 0
SIMON
SELSETUP
XINTCLK
XBR2SD0
XBR2SD1
XBR2SD2
XBR2SD3
XBRMSD0
XBRMSD1
XBRMSD2
XBRMSD3
XBRMULT 0
XBRMULT 1
XBRMULT 2
SETDSP 1
SETDSP 2
SETDSP 3
SETDSP 4
SETDSP 5
SETDSP 6
SETDSP 7
SETDSP 8
UE26 7402
UE22A 7402
UE20 7404
UE21 7400
UG24 74175 4-BIT REG
UF23 74175 4-BIT REG
UG25 74175 4-BIT REG
UF24 74175 4-BIT REG
UE25D ENAB 74125 BUS
UE25C ENAB 74125 BUS
UE25B ENAB 74125 BUS
UE25A ENAB 74125 BUS
UE24D ENAB 74125 BUS
UE24C ENAB 74125 BUS
UE24B ENAB 74125 BUS
UE24A ENAB 74125 BUS
UJ25D ENAB 74125 BUS
UJ25C ENAB 74125 BUS
UJ25B ENAB 74125 BUS
UJ25A ENAB 74125 BUS
UH24D ENAB 74125 BUS
UH24C ENAB 74125 BUS
UH24B ENAB 74125 BUS
UH24A ENAB 74125 BUS
SCHEM, PWA,
SIMULATOR 2
D 06141 34593


SMEMDEV0 = 4-17, 4-19, 5-5, 5-7
SMEMDEV1 = 4-16, 4-18, 5-4, 5-6
SMEMDEV2 = 4-21, 4-25, 4-23, 5-1
SMEMDEV3 = 4-20, 4-24, 4-28, 5-0
SMEMDEV4 = 4-23, 4-27, 4-31, 5-3
SMEMDEV5 = 4-22, 4-26, 4-30, 5-2
SMEMDEV6 = 5-8, 5-10, 5-12, 5-14
SMEMDEV7 = 5-9, 5-11, 5-13, 5-15
UG22 24957-1 32 x 8 PROM
UG 20 BCD TO DECIMAL DECODER/DRIVER 7442
UF 20 BCD TO DECIMAL DECODER/DRIVER 7442
UF19 BCD TO DECIMAL DECODER/DRIVER 7442
UG19 BCD TO DECIMAL DECODER/DRIVER 7442
UG 21 BCD TO DECIMAL DECODER/DRIVER 7442
UF 21 BCD TO DECIMAL DECODER/DRIVER 7442
SIMSTRB
SETSTRB
SETSIM 8
SETSIM 7
SETSIM 6
SETSIM 5
SETSIM 4
SETSIM 3
SETSIM 2
SETSIM 1
LDMA 2
LDMA 1
SIM4 (8-15)
SIM4 (16-31)/SIM5 (0-15)
SIM4 (8-7)
SIM5 (16-31)
SIMADR 15
SIMADR 14
SIMADR 13
SIMADR 12
SIMADR 11
SIMADR 10
SIMADR 9
SIMADR 8
SIMADR 7
SIMADR 6
SIMADR 5
SIMADR 4
SIMADR 3
SIMADR 2
SIMADR 1
SIMADR 0
SIMADR 3-5
SIMADR 51
SIMADR 50
SIMADR 49
SIMADR 48
EMEMDEV0
EMEMDEV1
EMEMDEV2
EMEMDEV3
EMEMDEV4
EMEMDEV5
EMEMDEV6
EMEMDEV7
SCHEM, PWA
SIMULATOR 2
86141
34593



Schlumberger

SCHEM, PWA,
SIMULATOR 2

SIZE	CODE IDENT NO	DRAWING NO	REV
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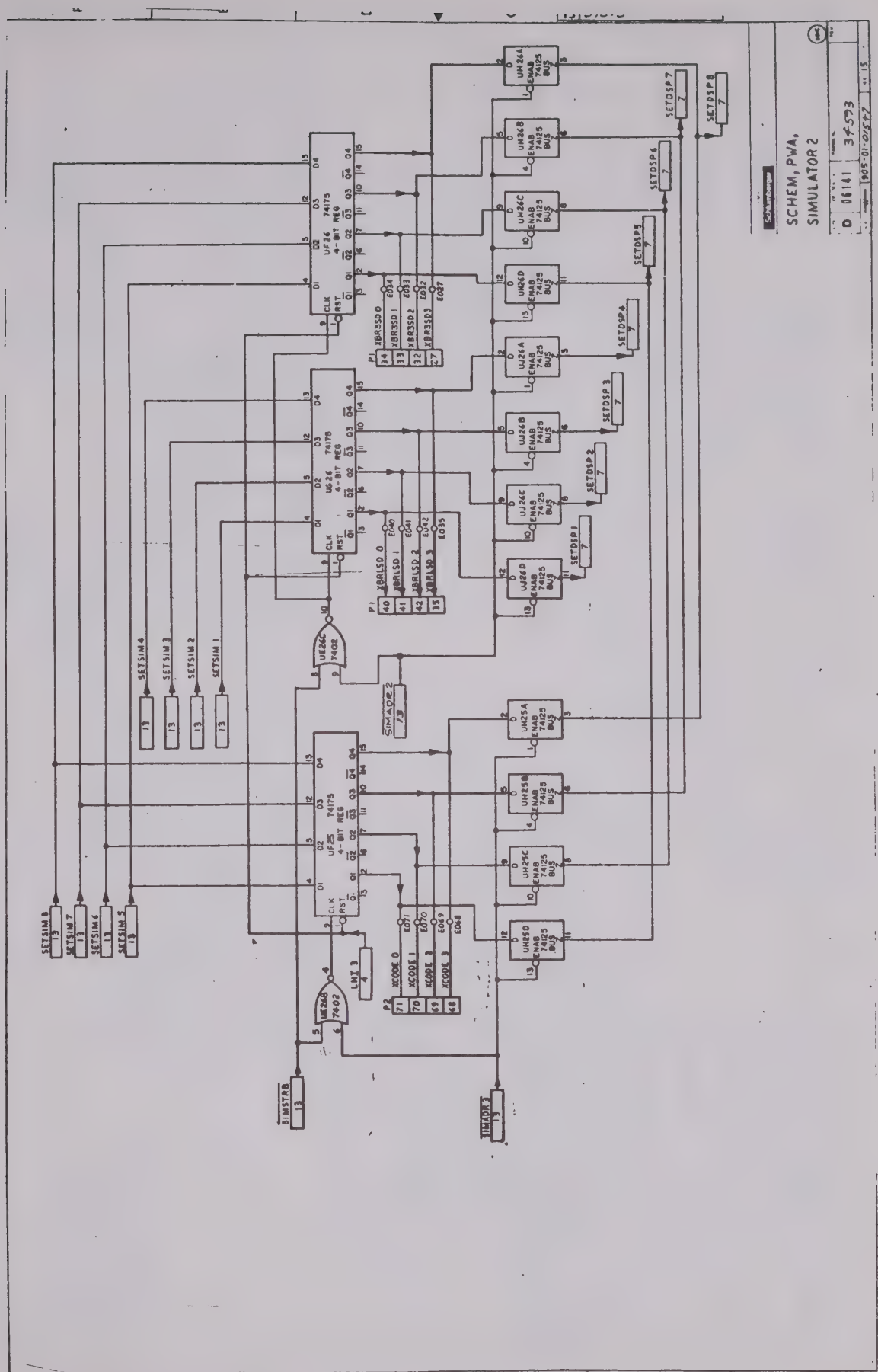
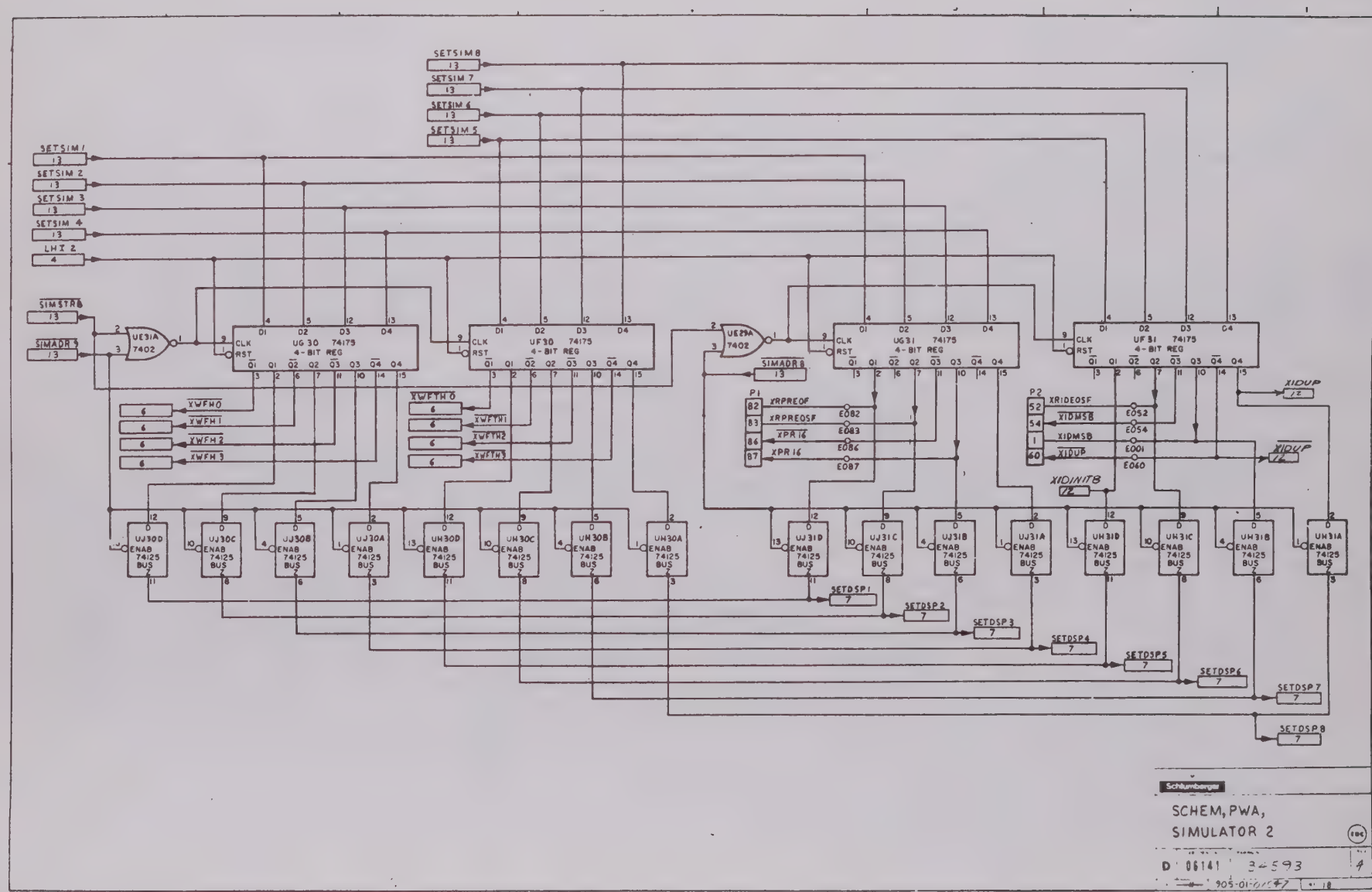
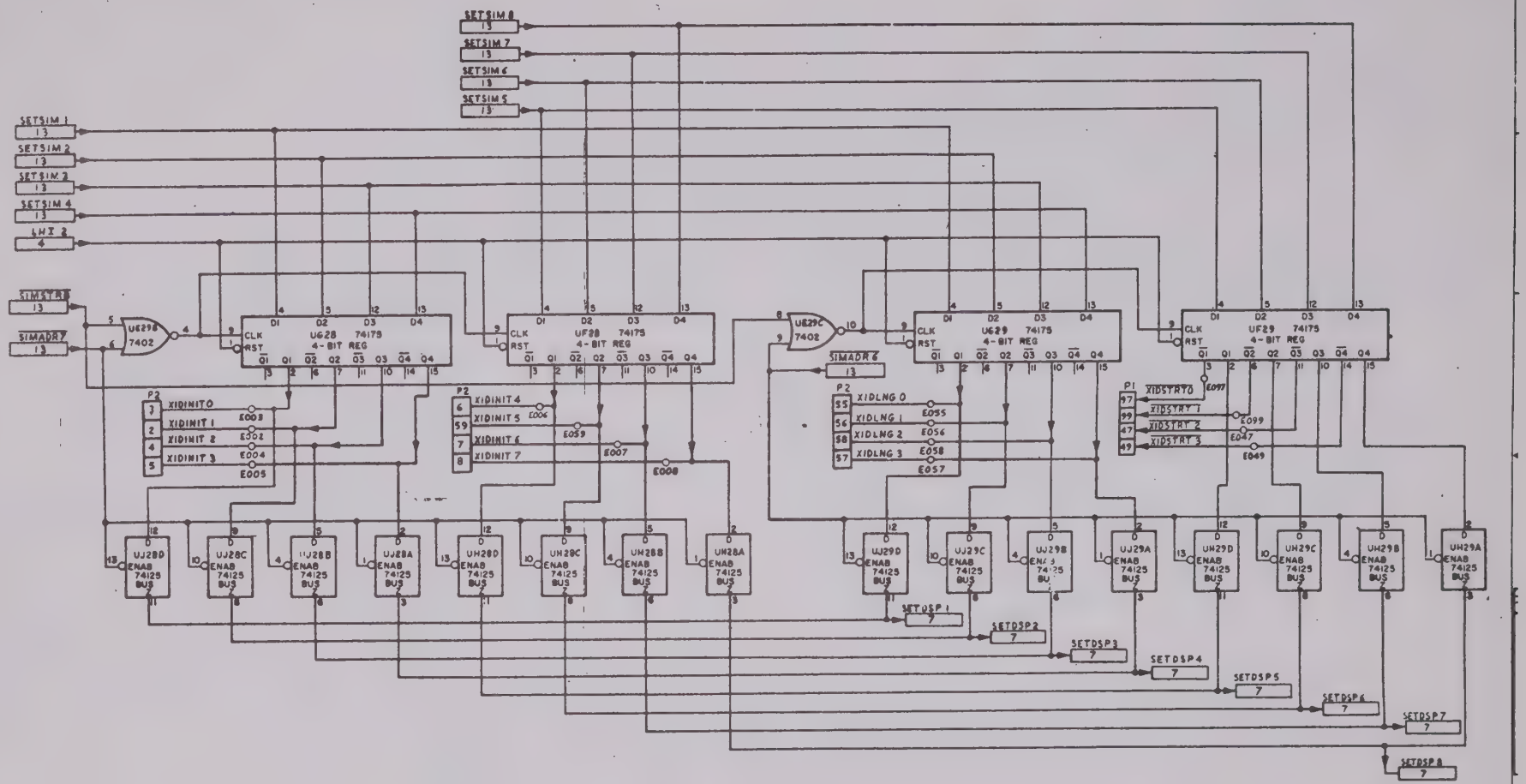
905-01-[illegible]


SCHEM, PWA,
SIMULATOR 2
D 06141 34593
905-01-01547
UF26 74175 4-BIT REG
UG26 74175 4-BIT REG
UF25 74175 4-BIT REG
UE26C 7402
UE26B 7402
UH26A ENAB 74125 BUS
UH26B ENAB 74125 BUS
UH26C ENAB 74125 BUS
UH26D ENAB 74125 BUS
UJ26A ENAB 74125 BUS
UJ26B ENAB 74125 BUS
UJ26C ENAB 74125 BUS
UJ26D ENAB 74125 BUS
UH25A ENAB 74125 BUS
UH25B ENAB 74125 BUS
UH25C ENAB 74125 BUS
UH25D ENAB 74125 BUS
SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
SETSIM 5
SETSIM 6
SETSIM 7
SETSIM 8
SETDSP 1
SETDSP 2
SETDSP 3
SETDSP 4
SETDSP 5
SETDSP 6
SETDSP 7
SETDSP 8
SIMADR 2
SIMADR 3
SIMSTRB
LHT 3
XCODE 0
XCODE 1
XCODE 2
XCODE 3
XBR3SD 0
XBR3SD 1
XBR3SD 2
XBR3SD 3
XBRLSD 0
XBRLSD 1
XBRLSD 2
XBRLSD 3


SETSIM 8
SETSIM 7
SETSIM 6
SETSIM 5
SETSIM 1
SETSIM 2
SETSIM 3
SETSIM 4
LHI 2
SIMSTRB
SIMADR 9
UE31A 7402
UG30 74175 4-BIT REG
UF30 74175 4-BIT REG
UE29A 7402
UG31 74175 4-BIT REG
UF31 74175 4-BIT REG
SIMADR 8
XWFH0
XWFH1
XWFH2
XWFH3
XWFTH0
XWFTH1
XWFTH2
XWFTH3
P1
XRPREOF
XRPREOSF
XPR16
XPR16
E082
E083
E086
E087
P2
XRIDEOSF
XIDMSB
XIDMSB
XIDUP
E052
E054
E001
E060
XIDUP
XIDUP
XIDINIT8
UJ30D
UJ30C
UJ30B
UJ30A
UH30D
UH30C
UH30B
UH30A
UJ31D
UJ31C
UJ31B
UJ31A
UH31D
UH31C
UH31B
UH31A
ENAB 74125 BUS
SETDSP1
SETDSP2
SETDSP3
SETDSP4
SETDSP5
SETDSP6
SETDSP7
SETDSP8
Schlumberger
SCHEM, PWA,
SIMULATOR 2
D 06141 34593
4
905-01-01-47



SCHEM, PWA,
SIMULATOR 2

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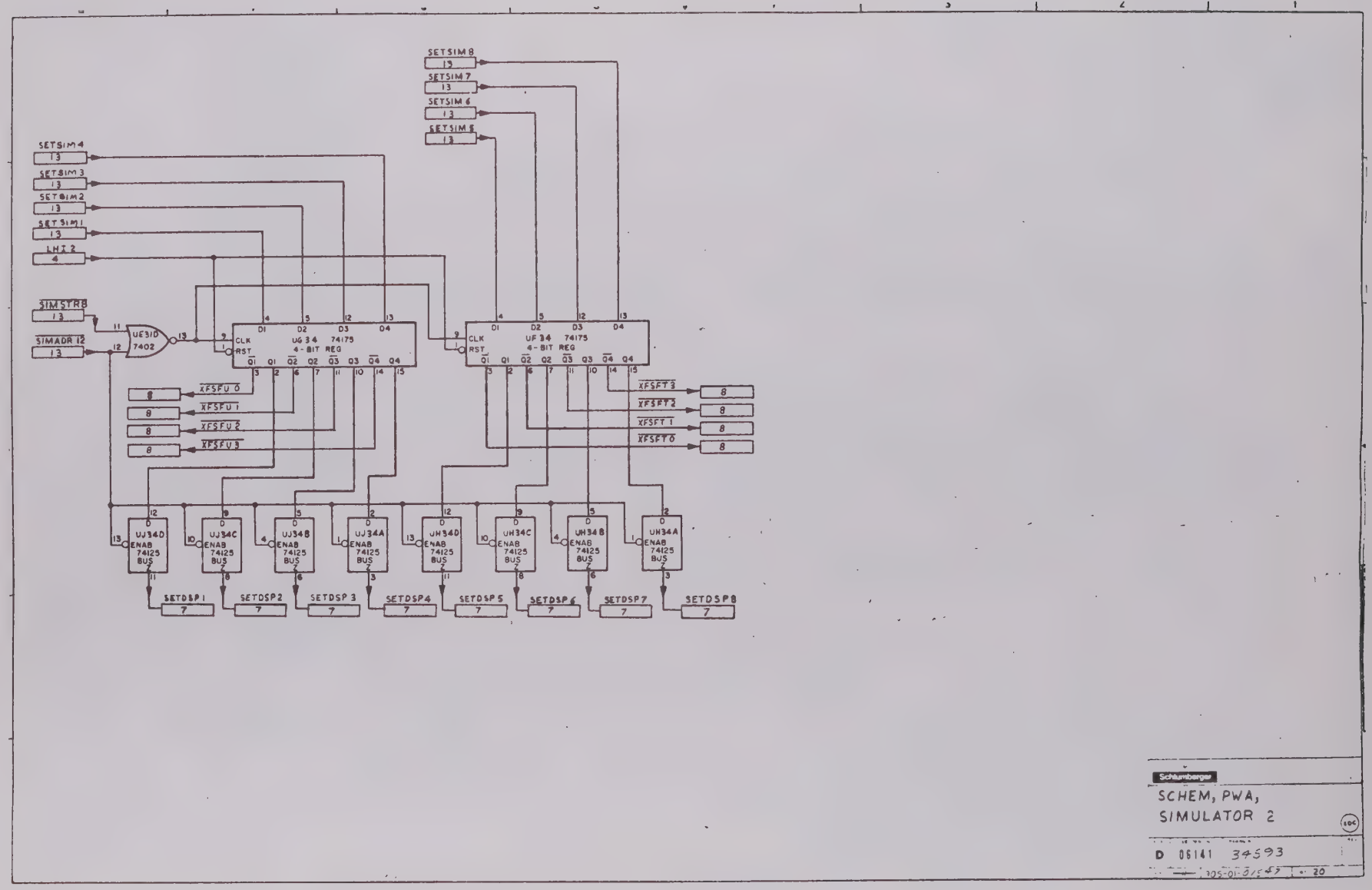
905-01-0597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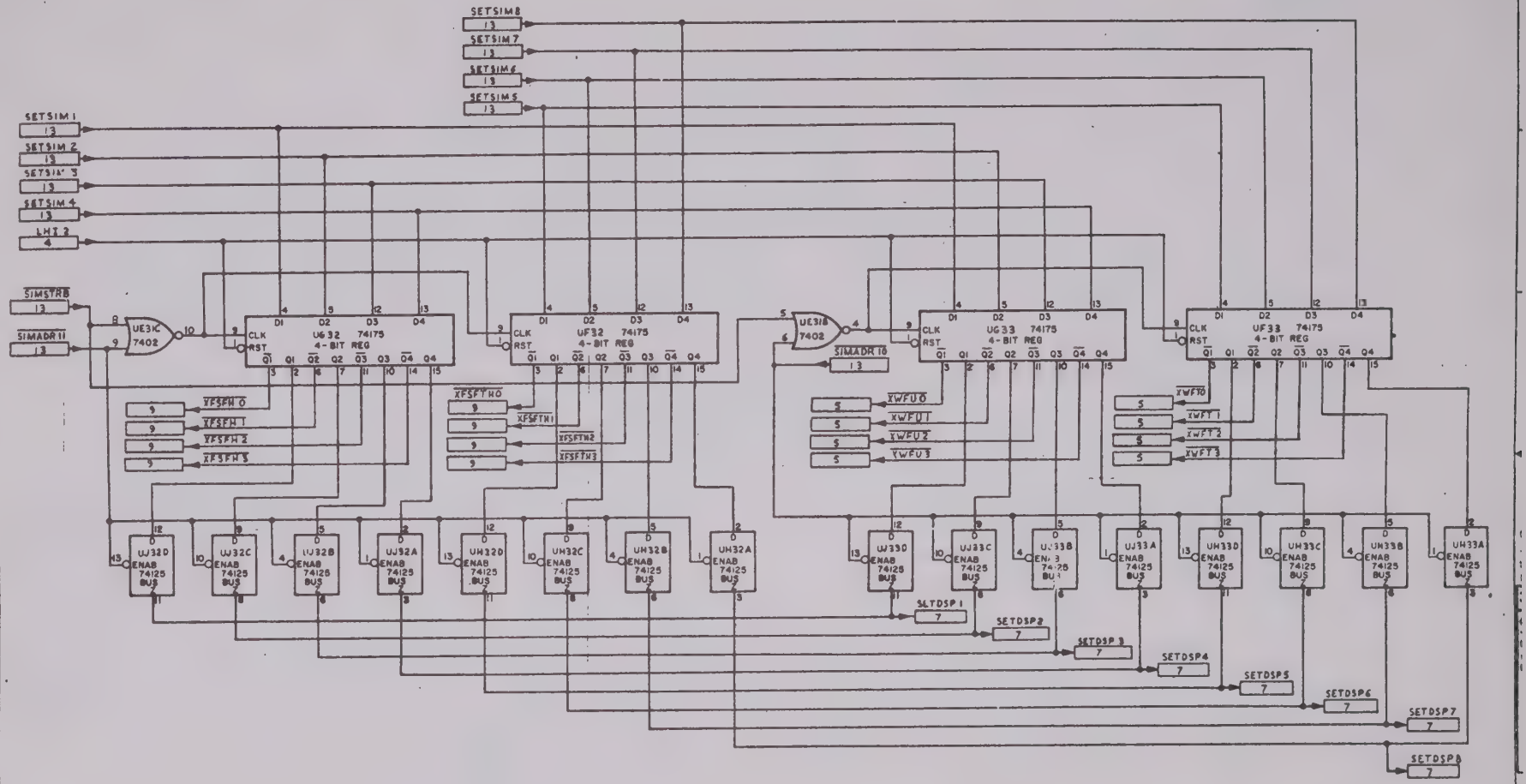
SETSIM 6
SETSIM 5
SETSIM 4
SETSIM 3
SETSIM 2
SETSIM 1
LHI 2
SIMSTRB
SIMADR 12
UE31D 7402
UG 34 74175 4-BIT REG
UF 34 74175 4-BIT REG
CLK
RST
XFSFU 0
XFSFU 1
XFSFU 2
XFSFU 3
XFSFT 3
XFSFT 2
XFSFT 1
XFSFT 0
UJ34D
UJ34C
UJ34B
UJ34A
UH34D
UH34C
UH34B
UH34A
ENAB 74125 BUS
SETDSP 1
SETDSP 2
SETDSP 3
SETDSP 4
SETDSP 5
SETDSP 6
SETDSP 7
SETDSP 8
Schlumberger
SCHEM, PWA,
SIMULATOR 2
D 06141 34593



Schlumberger

SCHEM, PWA,
SIMULATOR 2

D	06141	34593

HOLE/COMPONENT CHART		
LAST NO. USED HOLE	QTY	DESCRIPTION/UNUSED NUMBER

POWER PINS

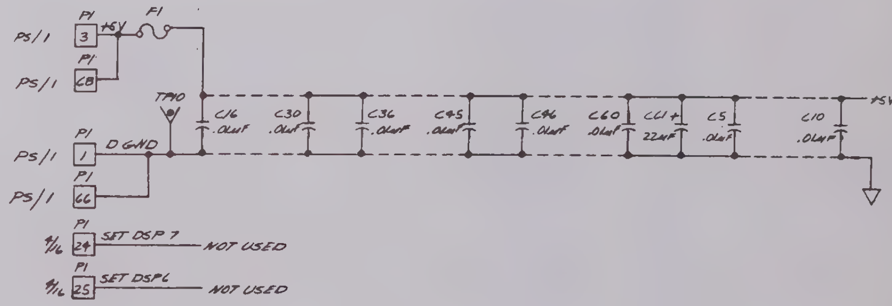
REF DES	+5V	GND	REF DES	+5V	GND
UA5	10	9	UF7	16	8
UA6	10	9	UF8	16	8
UA7	10	9	UF9	16	8
UA8	10	9	UF11	14	7
UA9	10	9	UF12	14	7
UA10	10	9	UF13	14	7
UB5	10	9	UF14	14	7
UB6	10	9	UH6	14	7
UB7	10	9	UH7	14	7
UB8	10	9	UH8	14	7
UB9	10	9	UH9	16	8
UB10	10	9	UH10	14	7
UC6	16	8	UH11	14	7
UC7	16	8	UH12	14	7
UC8	16	8	UH13	14	7
UC10	16	8	UH14	14	7
UD6	16	8	UJ2	14	7
UD7	16	8	UJ3	14	7
UD8	16	8	UJ4	14	7
UD9	16	8	UJ5	14	7
UD10	16	8	UJ6	14	7
UE6	16	8	UJ7	14	7
UE7	16	8	UJ8	14	7
UE8	16	8	UJ9	14	7
UE9	16	8	UJ10	14	7
UE10	16	8	UJ11	14	7
UE11	14	7	UJ12	14	7
UE12	16	8	UJ13	14	7
UE13	16	8	UJ14	14	7
UE14	16	8	UF10	14	7
UE15	14	7	UC1	14	7
UF15	14	7	UC2	14	7
			UC3	14	7
			UC4	16	8
			UC5	14	7
			UC11	14	7
			UC15	14	7
			UD1	14	7
			UD2	14	7
			UD3	14	7
			UD4	14	7
			UD5	14	7
			UD15	14	7

ARTWORK REVISION INDEX

SHEET NO.								
REVISION								

REVISIONS

SYM	DESCRIPTION	EFFECTIVITY	DATE	APPROVED
A	REC CHNG UPDATE ALL SHTS		7-22-77	
B	ECO 55654 CHNG [illegible] PRWDRNG SHTS 2		10-26-77	
C	ECO 55479 ADD CKT SHTS CHNG CKT SHT 6		11-2-77	
D	ECO 56370 ADD UH7 & JJG SHT 5		3-3-78	
E	ECO 57670 DELE UD10 [illegible]		12-12-78	
F	ECO 59059 ADDED UE15 & UF15 TO SHT 1 & 5	EDDT E3 [illegible]	8-[illegible]-79	



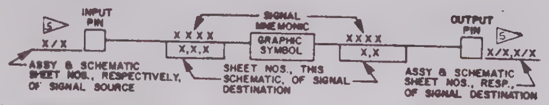
7 MAY BE CHANGED BY TEST.

6. TO TEST MEMORY
   A. GND TP1
   B. JUMPER TP3 TO TP4
   C. WRITE CLEAR (1:31 BIT 4="1")
   D. VERIFY LED (TP27) OFF
   E. MOVE JUMPER FROM TP4 TO TP5
   F. WRITE CLEAR
   G. VERIFY LED OFF
   H. [illegible] JUMPER BOARDS IN ZA1 & ZB1
   I. MOVE JUMPER FROM TP5 BLACK TO TP4
   J. REPEAT STEPS C THRU G

   GROUNDING TP2 JAMS DATA INVERTED FROM TP3 INTO MEMORY
   GROUNDING TP25 LETS READ CYCLE RUN CONTINUOUSLY.

5. ABBREVIATIONS USED FOR SIGNAL SOURCE AND/OR SIGNAL DESTINATION ADDRESSING & RELATED REF. DOCUMENTS ARE AS FOLLOWS:
   - FP = FRONT PANEL (DWG. 28070)
   - PS = POWER SUPPLY (DWG. 32945)
   - RP = REAR PANEL (DWG ——, REF I/O LIST DWG 32938) CONNECTIONS ARE INDICATED BY CONNECTOR "J" NO. & PIN NO.
   - 4 = CARD 4 (DWG. 34595)
   - 5 = CARD 5 (DWG. 34599)
   - 7 = CARD 7 (DWG. 34593)
   - 8 = CARD 8 (DWG. 34597)
   - 10 = CARD 10 (DWG 34309)

4. ADDRESS DEFINITION:



3. CIRCUIT RETURN SYMBOLS:
   —▷ DIGITAL GND.

2. FOR TOLERANCES AND RATINGS SEE PARTS LIST.

1. RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS.

UNLESS OTHERWISE SPECIFIED:
NOTES:

PARTS LIST

BSC	34305	710-02
DASH NO.	NEXT ASSY NO	USED ON

APPLICATION

DO NOT APPLY PART NO. IDENTIFY PER [illegible]

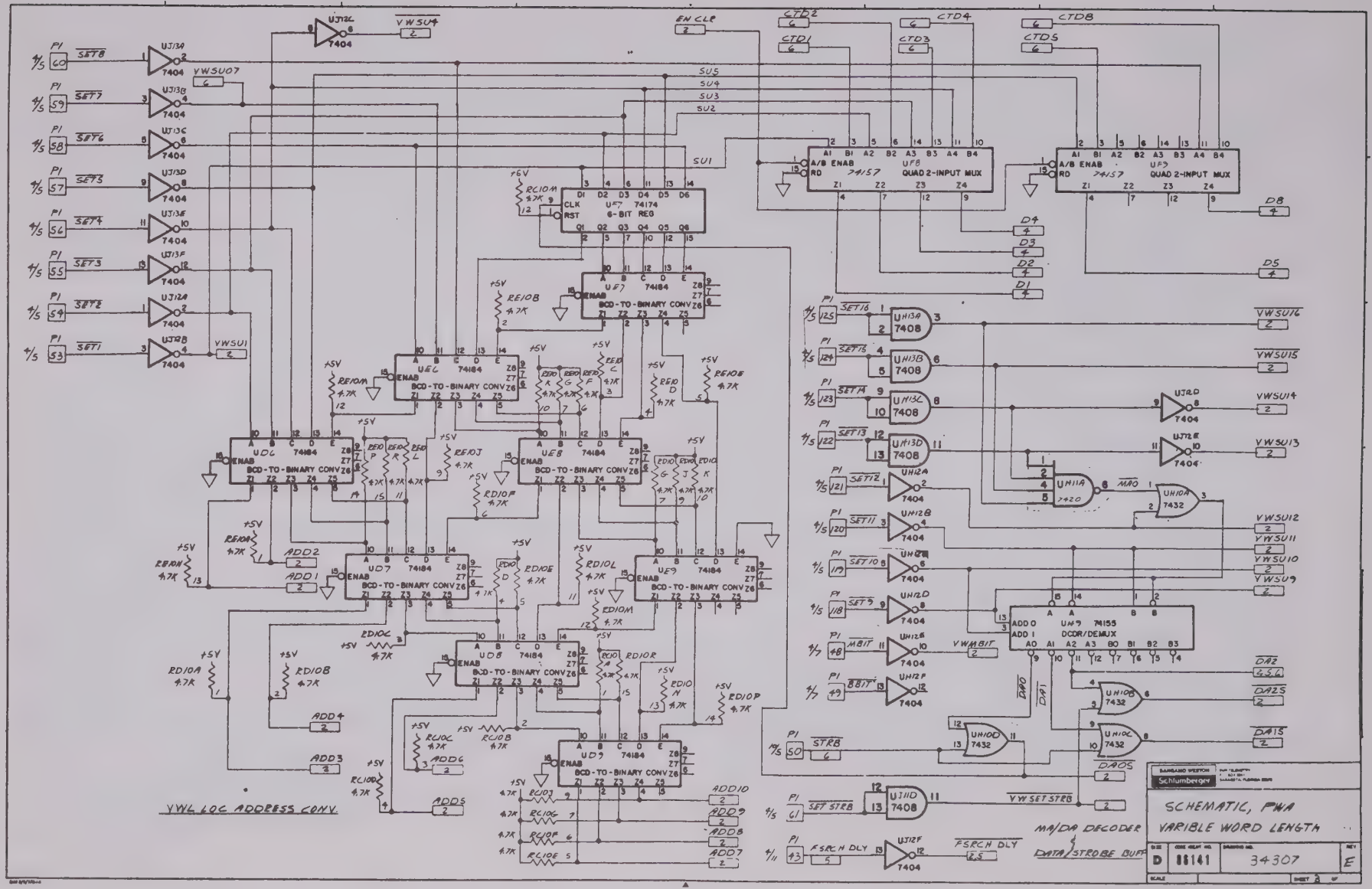
UNLESS OTHERWISE SPECIFIED — DO NOT SCALE DRAWING

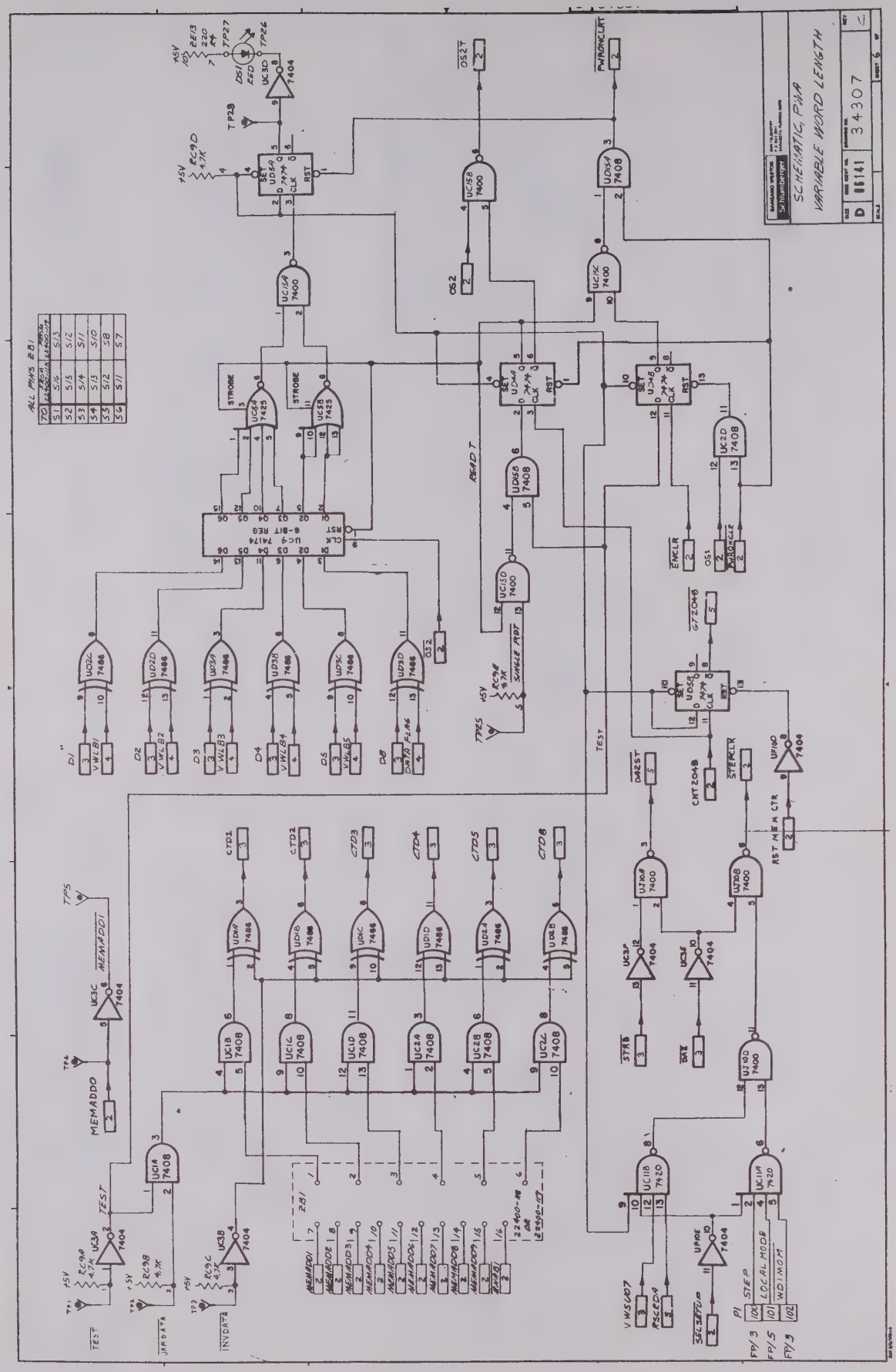
SANGAMO WESTON — Schlumberger

SCHEMATIC, PWA VARIABLE WORD LENGTH

SIZE D | CODE IDENT NO. 06141 | DRAWING NO. 34307 | REV F

SHEET 1 OF 7


SCHEMATIC, PWA
VARIBLE WORD LENGTH
MA/DA DECODER
DATA/STROBE BUFF
YWL LOC ADDRESS CONV.
Schlumberger
D
86141
34307
E


SCHEMATIC, PWA
VARIABLE WORD LENGTH
D 06141 34307
Schlumberger
UC9 74174 6-BIT REG
UC1A 7408
UC3A 7404
UC3C 7404
UC3B 7404
UC118 7420
UC11A 7420
UC4A 7474
UC4B 7474
UC5A 7425
UC5B 7425
UC15A 7400
UC15B 7400
UC15C 7400
UC15D 7400
UC3D 7404
UD15A 7408
UD15B 7408
UD15D 7408
UC2D 7408
UD2C 7408
UD2D 7408
UD3A 7408
UD3B 7408
UD3C 7408
UD3D 7408
UD4A 7408
UD4B 7408
UD4C 7408
UD4D 7408
UD2A 7408
UD2B 7408
UC1B 7408
UC1C 7408
UC1D 7408
UC2A 7408
UC2B 7408
UC2C 7408
UJ10A 7400
UJ10B 7400
UJ10D 7400
UF10D 7404
UP10E 7404
UC3F 7404
UC3E 7404
ALL PINS 281
TEST
JAMDATA
INVDATA
MEMADDO
MEMADD1
READ T
SINGLE RDT
STEP
LOCAL MODE
WDIMOM
PWRONCLRT
ENCLR
STEPCLR
RST MEM CTR
CNT2048
GT2048
DARST
STRB
DAT
SELSETUP
VWSUD7
RSCRDA
OS1
OS2
OS2T
STROBE
CTD1
CTD2
CTD3
CTD4
CTD5
CTD6
D1
D2
D3
D4
D5
D6
VWLB1
VWLB2
VWLB3
VWLB4
VWLB5
VWLB6
DATA FLAG
MEMADD1
MEMADD2
MEMADD3
MEMADD4
MEMADD5
MEMADD6
MEMADD7
MEMADD8
MEMADD9
ENABL
22400-18
22400-17
TP1
TP2
TP3
TP4
TP5
TP23
TP25
TP26
TP27
DS1 RED
+5V
RC9A 4.7K
RC9B 4.7K
RC9C 4.7K
RC9D 4.7K
RC9E 4.7K
RC9F 4.7K
RC9G 4.7K
RC9H 4.7K
RC9I 4.7K
RC9J 4.7K
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RC9MV 4.7K
RC9MW 4.7K
RC9MX 4.7K
RC9MY 4.7K
RC9MZ 4.7K
RC9NA 4.7K
RC9NB 4.7K
RC9NC 4.7K
RC9ND 4.7K
RC9NE 4.7K
RC9NF 4.7K
RC9NG 4.7K
RC9NH 4.7K
RC9NI 4.7K
RC9NJ 4.7K
RC9NK 4.7K
RC9NL 4.7K
RC9NM 4.7K
RC9NN 4.7K
RC9NO 4.7K
RC9NP 4.7K
RC9NQ 4.7K
RC9NR 4.7K
RC9NS 4.7K
RC9NT 4.7K
RC9NU 4.7K
RC9NV 4.7K
RC9NW 4.7K
RC9NX 4.7K
RC9NY 4.7K
RC9NZ 4.7K
RC9OA 4.7K
RC9OB 4.7K
RC9OC 4.7K
RC9OD 4.7K
RC9OE 4.7K
RC9OF 4.7K
RC9OG 4.7K
RC9OH 4.7K
RC9OI 4.7K
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RC9OL 4.7K
RC9OM 4.7K
RC9ON 4.7K
RC9OO 4.7K
RC9OP 4.7K
RC9OQ 4.7K
RC9OR 4.7K
RC9OS 4.7K
RC9OT 4.7K
RC9OU 4.7K
RC9OV 4.7K
RC9OW 4.7K
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RC9OY 4.7K
RC9OZ 4.7K
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RC9PS 4.7K
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RC9PU 4.7K
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RC9QC 4.7K
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RC9QG 4.7K
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RC9QJ 4.7K
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RC9RE 4.7K
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RC9RG 4.7K
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RC9RJ 4.7K
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RC9RY 4.7K
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RC9SD 4.7K
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RC9VK 4.7K
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RC9VO 4.7K
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RC9VQ 4.7K
RC9VR 4.7K
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RC9VU 4.7K
RC9VV 4.7K
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RC9WO 4.7K
RC9WP 4.7K
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RC9WS 4.7K
RC9WT 4.7K
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RC9WV 4.7K
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RC9WX 4.7K
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RC9XV 4.7K
RC9XW 4.7K
RC9XX 4.7K
RC9XY 4.7K
RC9XZ 4.7K
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RC9YD 4.7K
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RC9YF 4.7K
RC9YG 4.7K
RC9YH 4.7K
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RC9YK 4.7K
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RC9YO 4.7K
RC9YP 4.7K
RC9YQ 4.7K
RC9YR 4.7K
RC9YS 4.7K
RC9YT 4.7K
RC9YU 4.7K
RC9YV 4.7K
RC9YW 4.7K
RC9YX 4.7K
RC9YY 4.7K
RC9YZ 4.7K
RC9ZA 4.7K
RC9ZB 4.7K
RC9ZC 4.7K
RC9ZD 4.7K
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RC9ZN 4.7K
RC9ZO 4.7K
RC9ZP 4.7K
RC9ZQ 4.7K
RC9ZR 4.7K
RC9ZS 4.7K
RC9ZT 4.7K
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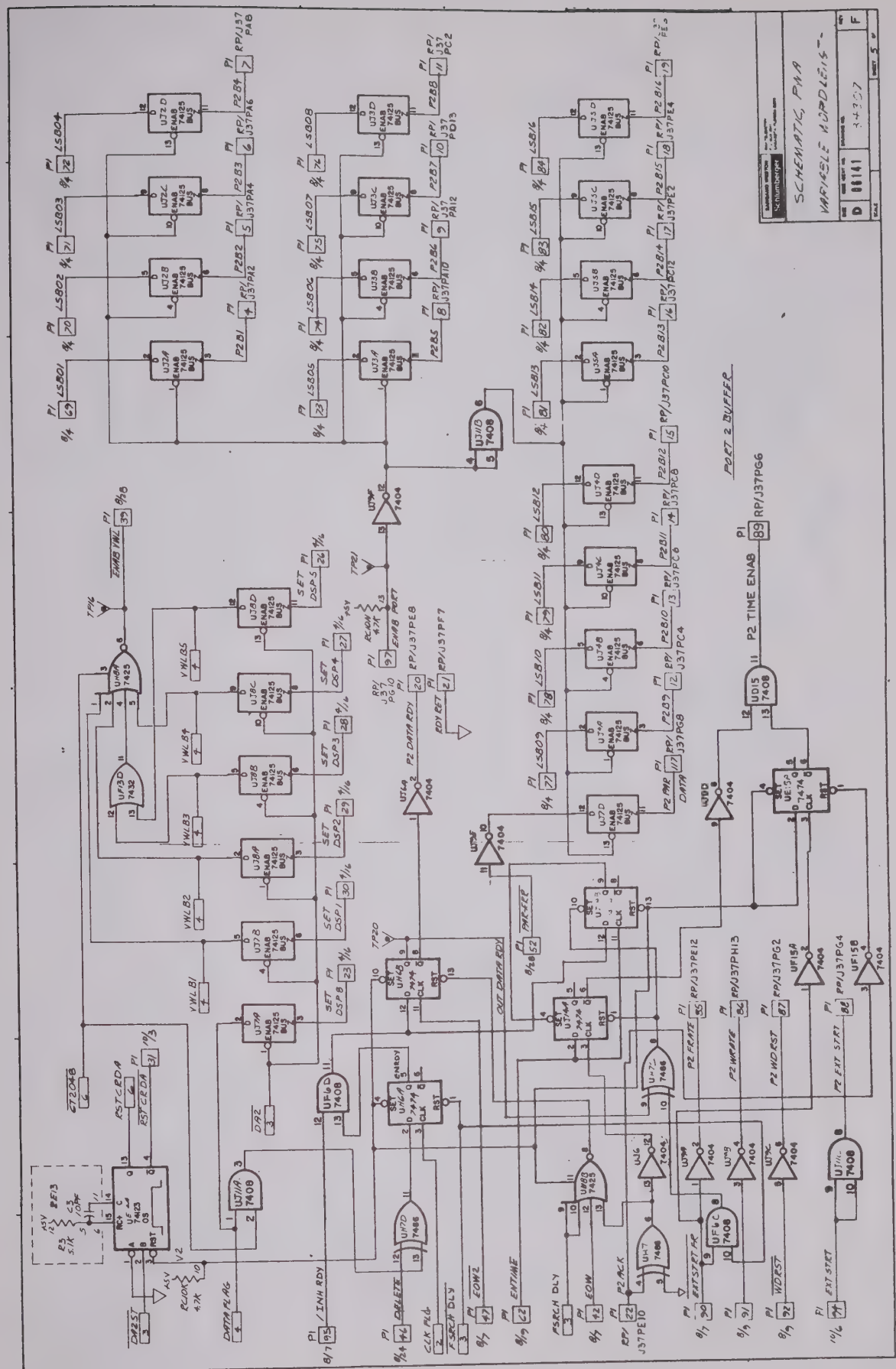
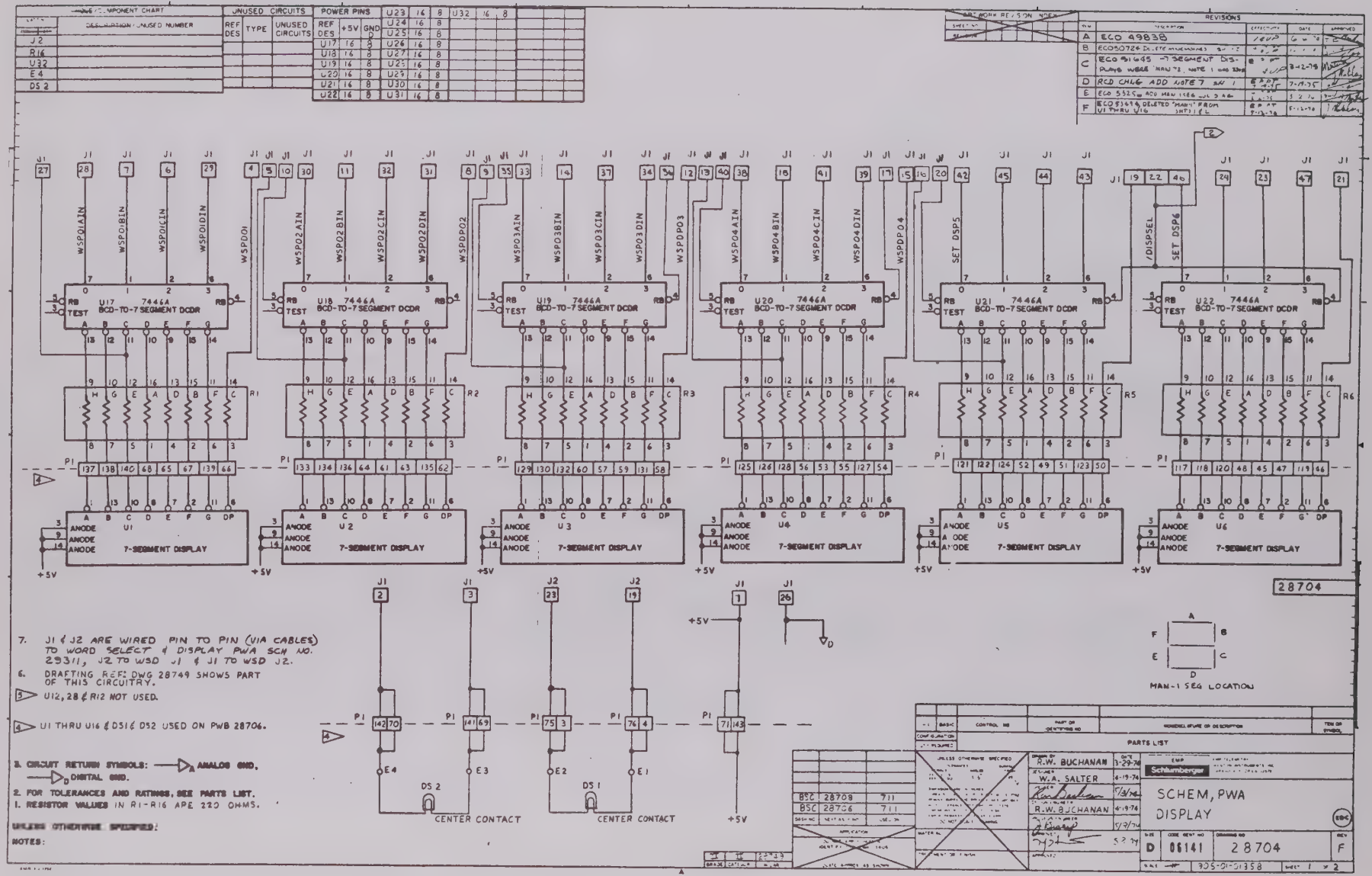
RC9ZX 4.7K
RC9ZY 4.7K
RC9ZZ 4.7K

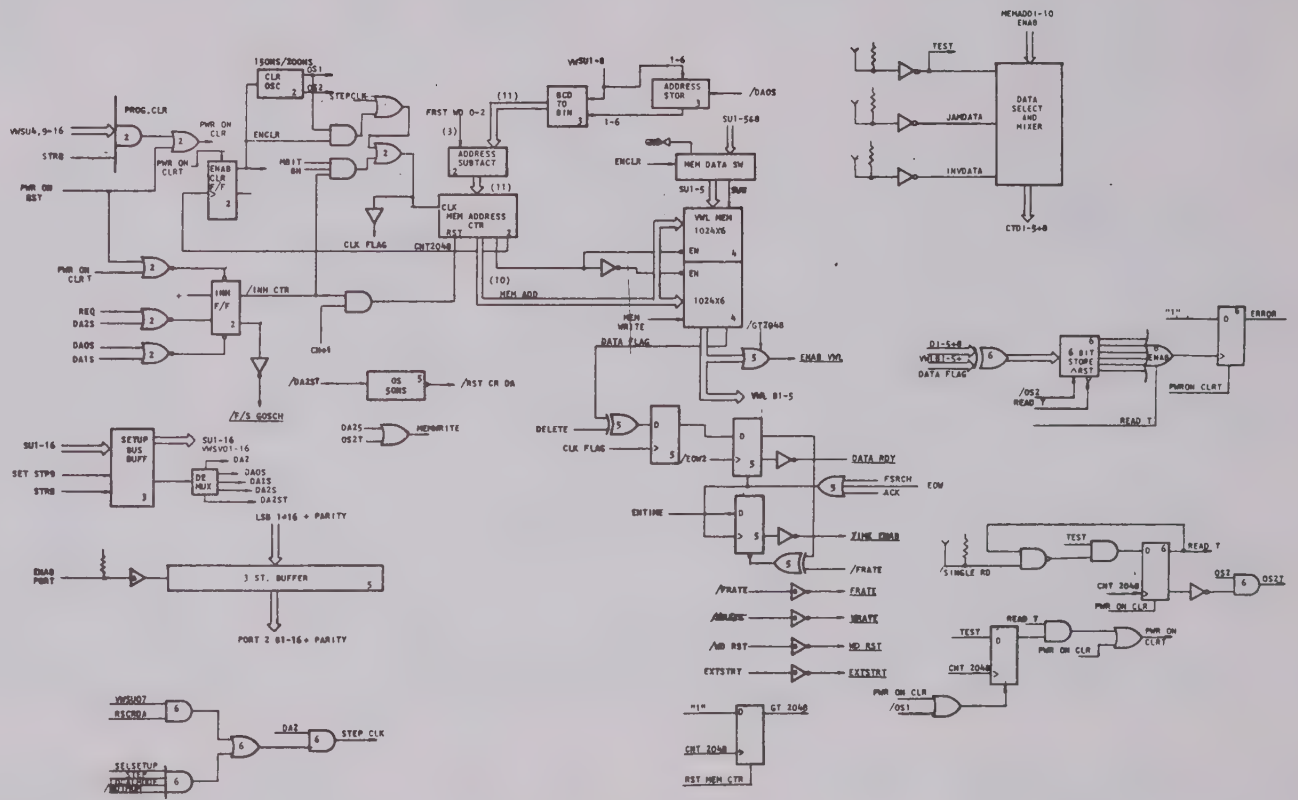

SCHEMATIC, PWA
VARIABLE WORD LENGTH
PORT 2 BUFFER
P2 TIME ENAB



7. J1 & J2 ARE WIRED PIN TO PIN (VIA CABLES) TO WORD SELECT & DISPLAY PWA SCH NO. 29311, J2 TO WSD J1 & J1 TO WSD J2.
6. DRAFTING REF: DWG 28749 SHOWS PART OF THIS CIRCUITRY.
5. U12, 28 & R12 NOT USED.
4. U1 THRU U16 & DS1 & DS2 USED ON PWB 28706.
3. CIRCUIT RETURN SYMBOLS: A ANALOG GND, D DIGITAL GND.
2. FOR TOLERANCES AND RATINGS, SEE PARTS LIST.
1. RESISTOR VALUES IN R1-R16 ARE 220 OHMS.

UNLESS OTHERWISE SPECIFIED:

NOTES:

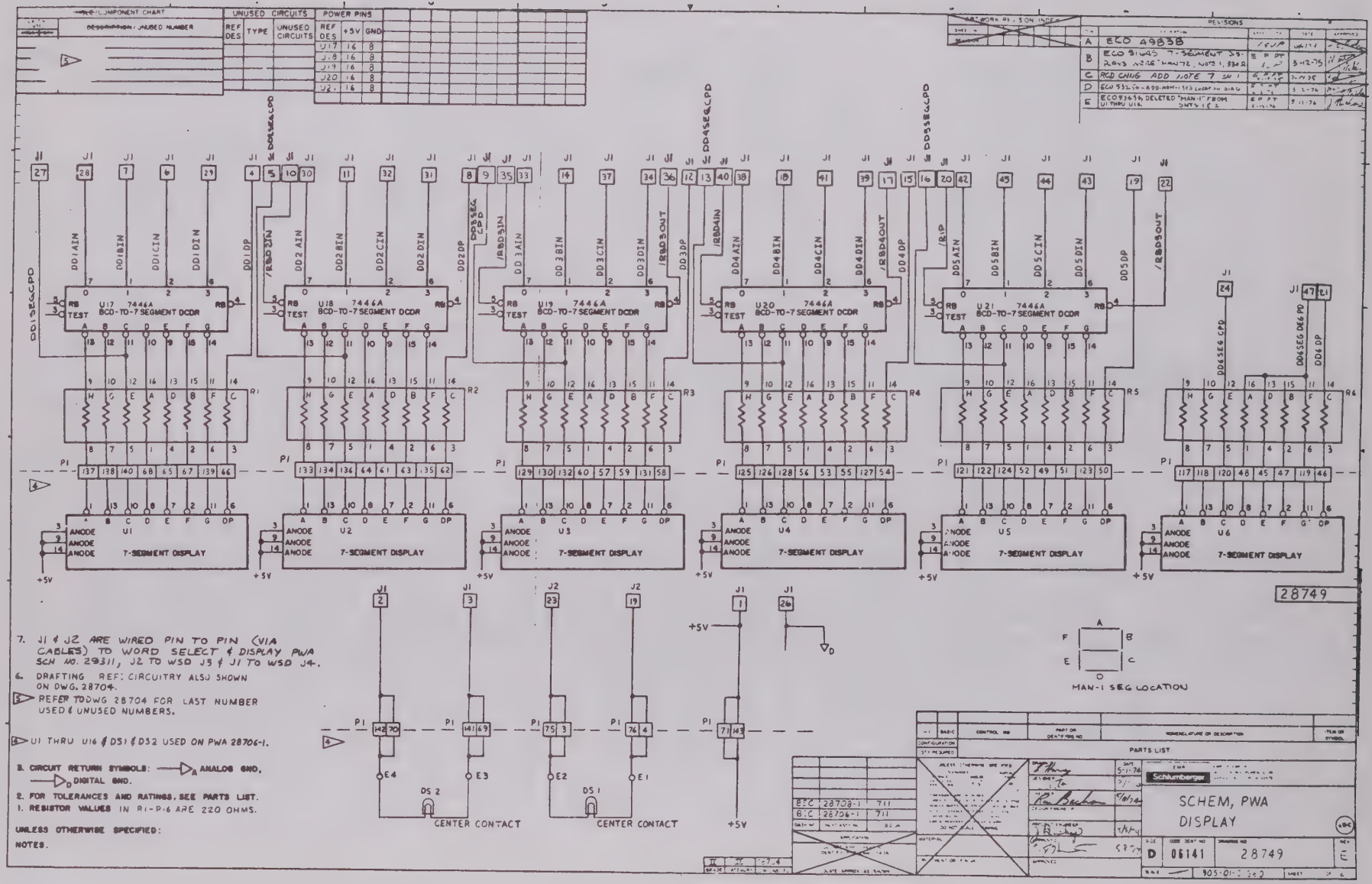


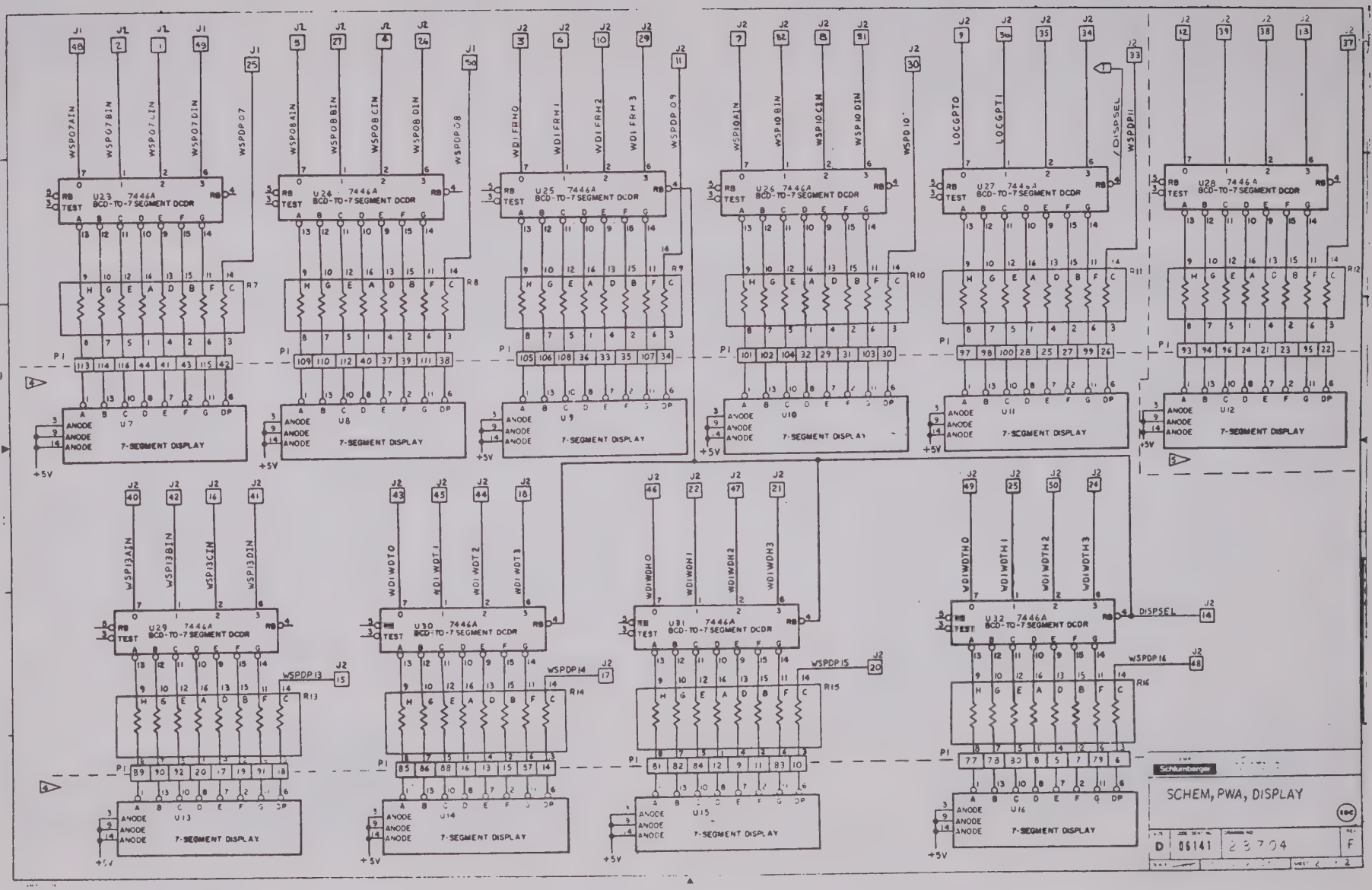
Schlumberger

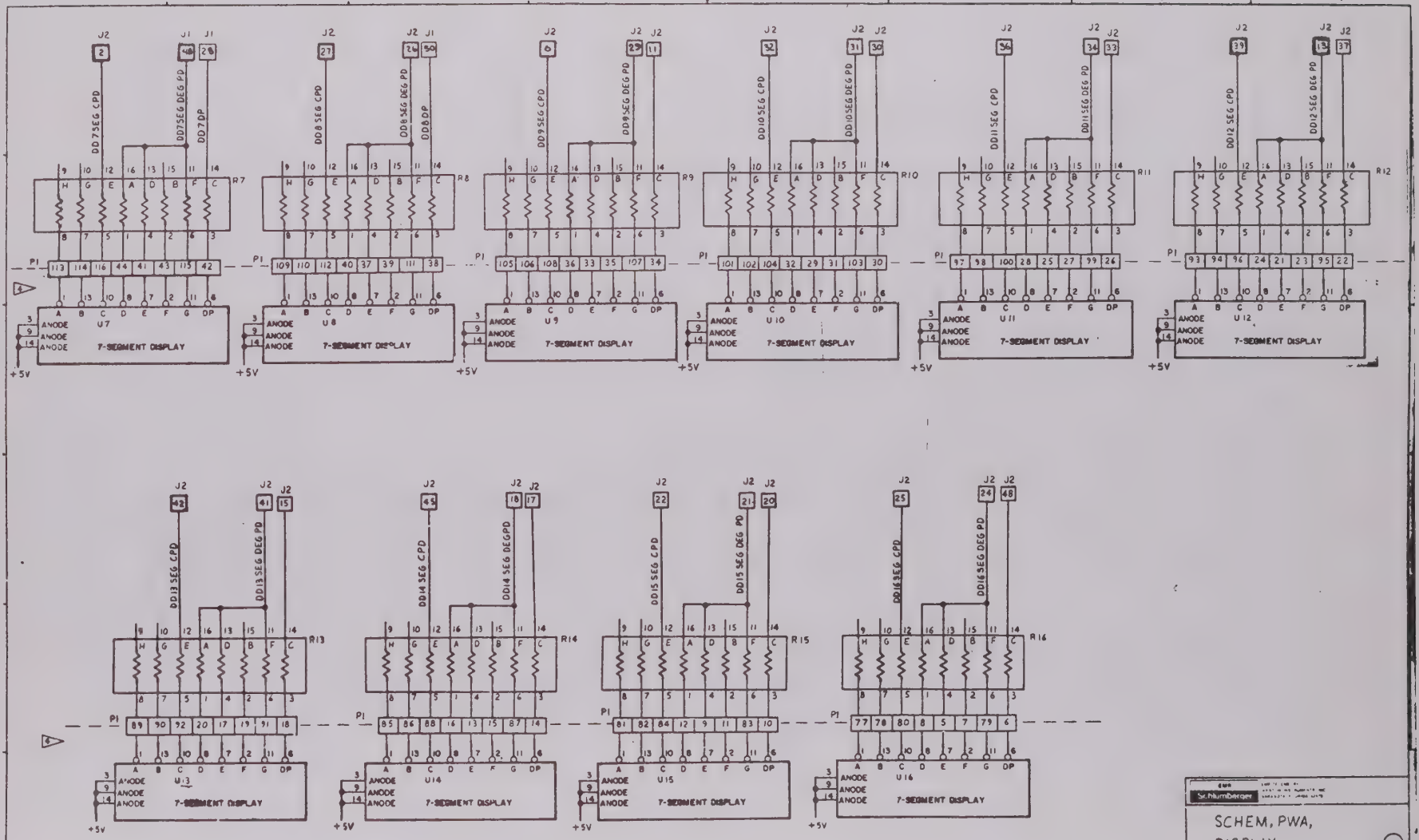
SCHEMATIC, PMA
VARIABLE WORD LENGTH

SIZE	CAGE IDENT NO.	DRAWING NO.	REV
D	86141	34307	B

SCALE — SHEET 7 OF


UNUSED CIRCUITS
POWER PINS
REVISIONS
U17 7446A BCD-TO-7 SEGMENT DCDR
U18 7446A BCD-TO-7 SEGMENT DCDR
U19 7446A BCD-TO-7 SEGMENT DCDR
U20 7446A BCD-TO-7 SEGMENT DCDR
U21 7446A BCD-TO-7 SEGMENT DCDR
7-SEGMENT DISPLAY
7. J1 & J2 ARE WIRED PIN TO PIN (VIA CABLES) TO WORD SELECT & DISPLAY PWA SCH NO. 29311, J2 TO WSD J3 & J1 TO WSD J4.
6. DRAFTING REF: CIRCUITRY ALSO SHOWN ON DWG. 28704.
5. REFER TO DWG 28704 FOR LAST NUMBER USED & UNUSED NUMBERS.
4. U1 THRU U16 & DS1 & DS2 USED ON PWA 28706-1.
3. CIRCUIT RETURN SYMBOLS: ANALOG GND, DIGITAL GND.
2. FOR TOLERANCES AND RATINGS, SEE PARTS LIST.
1. RESISTOR VALUES IN R1-R6 ARE 220 OHMS.
UNLESS OTHERWISE SPECIFIED:
NOTES.
MAN-1 SEG LOCATION
CENTER CONTACT
CENTER CONTACT
PARTS LIST
SCHEM, PWA
DISPLAY
28749


U23 7446A BCD-TO-7 SEGMENT DCDR
U24 7446A BCD-TO-7 SEGMENT DCDR
U25 7446A BCD-TO-7 SEGMENT DCDR
U26 7446A BCD-TO-7 SEGMENT DCDR
U27 7446A BCD-TO-7 SEGMENT DCDR
U28 7446A BCD-TO-7 SEGMENT DCDR
U29 7446A BCD-TO-7 SEGMENT DCDR
U30 7446A BCD-TO-7 SEGMENT DCDR
U31 7446A BCD-TO-7 SEGMENT DCDR
U32 7446A BCD-TO-7 SEGMENT DCDR
7-SEGMENT DISPLAY
WSP07AIN
WSP07BIN
WSP07CIN
WSP07DIN
WSP07DO7
WSP08AIN
WSP08BIN
WSP08CIN
WSP08DIN
WSP08DO8
WDIFRM0
WDIFRM1
WDIFRM2
WDIFRM3
WSPDP09
WSP10AIN
WSP10BIN
WSP10CIN
WSP10DIN
WSPD10
LOCGPT0
LOCGPT1
DISPSEL
WSPDP11
WSP13AIN
WSP13BIN
WSP13CIN
WSP13DIN
WSPDP13
WDIWDT0
WDIWDT1
WDIWDT2
WDIWDT3
WSPDP14
WSPDP15
WDIWDH0
WDIWDH1
WDIWDH2
WDIWDH3
WSPDP16
DISPSEL
SCHEM, PWA, DISPLAY
Schlumberger
D 06141 23704 F


DD7SEG CPD
DD7SEG DEG PD
DD7DP
DD8SEG CPD
DD8SEG DEG PD
DD8DP
DD9SEG CPD
DD9SEG DEG PD
DD10SEG CPD
DD10SEG DEG PD
DD11SEG CPD
DD11SEG DEG PD
DD12SEG CPD
DD12SEG DEG PD
DD13SEG CPD
DD13SEG DEG PD
DD14SEG CPD
DD14SEG DEGPD
DD15SEG CPD
DD15SEG DEG PD
DD16SEG CPD
DD16SEG DEG PD
7-SEGMENT DISPLAY
ANODE
+5V
SCHEM, PWA,
DISPLAY
D
88141
28749
E

SECTION 7

DRAWINGS AND PARTS LISTS

7.1 GENERAL

This section contains assembly diagrams and parts lists for the EMR Model 710 PCM Decommutator.

7.2 ASSEMBLY DRAWINGS AND PARTS LISTS

The following assembly diagrams and parts lists are included in this section:

DRAWING NO.	NAME
32890	PCM Decommutator Assembly
PL-32890-1	PCM Decommutator Assy. Parts List
28072	Front Subpanel PWA
PL-28072-1	Front Subpanel PWA Parts List
32940	Rear Panel Assembly
PL-32940-1	Rear Panel Assy. Parts list
28708	Display Drivers PWA
PL-28708	Display Drivers PWA Parts List (Basic Configuration)
PL-28708-1	Display Drivers PWA Parts List (-1 Configuration)
33052	Ground Terminator PWA
PL-33052	Ground Terminator PWA Parts List
32944	Paddle Board PWA
PL-32944	Paddle Board PWA Parts List
34596	Frame Synchronizer PWA
PL-34596	Frame Synchronizer PWA Parts List
34598	Word Select & Display PWA
PL-34598	Word Select & Display PWA Parts List
34311	Data Entry PWA
PL-34311	Data Entry PWA Parts List

34600	Subframe PWA
PL-34600-1	Subframe PWA Parts List (-1 Subframe Option)
PL-34600	Subframe PWA Parts List (-2 Subframe Option)
34592	Simulator Card 1 PWA
PL-34592	Simulator Card 1 PWA Parts List
34594	Simulator Card 2 PWA
PL-34594	Simulator Card 2 PWA Parts List
34308	Variable Word Length PWA
PL-34308	Variable Word Length PWA Parts List
33101	Power Supply PS2
PL-33101	Power Supply PS2 Parts List
33100	Card Reader Kit
PL-33100	Card reader Kit Parts List
22400	Special Network
PL-22400-73	Special Network Parts List
22400-74	
22400-75	
22400-76	
22400-77	
22400-78	
22400-116	
22400-117	
22400-118	
22400-119	
PL-22400-120	Special Networks Parts List

ASSEMBLY NOTES:

1. APPLY APPLICABLE INFORMATION PER EMR 13406.
2. ITEMS 5 (RACK MTG BRKTS), 55 (POWER CORD ASSY), 101 (MALE PINS), 103 (CABLE CLAMPS), A5P37, A5P38 & A5P30 THRU A5P34 (REAR PANEL MATING CONN) (NOT SHOWN) SHIPPED WITH UNIT UNINSTALLED, ALSO ITEMS 75 & 76 (EXTENDER PWA'S).
3. HDW USED ONLY IF PS2 IS USED.
4. ON ITEM 22, REMOVE THE 2 OUTSIDE SCREWS (DISCARD) ON THE LAMP HOLDING BRKTS & FASTEN ITEMS 24 & 25 TO ITEM 22 USING ITEM 50 WITH ITEM 60 BETWEEN ITEMS 22 & 24.
5. BOND ALL CARD GUIDES IN PLACE USING ITEM 59 AS REQD.
6. SECURE ITEM 26 IN FRONT PANEL USING ITEM 59 AS REQD.
7. CLIP WIRE WRAP PINS STICKING OUT FROM ITEM 20 (PADDLE PWA) ENOUGH TO CLEAR S1.
8. INSTALL ITEM 66, ON ITEM 12, ON EACH SIDE CENTERED BETWEEN CARD GUIDE BRKTS (ITEMS 28 & 29) JUST CLEARING THE CARD GUIDES (ITEM 62).
9. INSTALL ITEM 56 (CABLE CLAMP) UNDER SCREW HEAD AT FAR END OF ITEM 20 (PADDLE PWA).
10. INSTALL ITEM 78 (CONN MTG BRKT) & CONN A1J18 IN MIDDLE OF ITEM 20 (PADDLE PWA). WIRE A1J18 TO FRONT PANEL A3J3 USING A3P18 & ITEMS 79 THRU 86 PER WIRING DIAGRAM 30156. SEE DETAIL 'A' FOR ASSY OF A1J18, A3J3 & A3P18.
11. WIRE A5 (REAR PANEL) INTERNALLY & TO PS1 & TO A1 (BASE PLATE) PER WIRING DIAGRAM 32945 & I/O CONN LIST 32938 USING A5J2, A5J39 & ITEMS 85 THRU 91 & 102.
12. WIRE A1 (BASE PLATE) PER WIRING DIAGRAM 32945 & MFG WIRE LIST WL-32890 FOR BSC & WL-32890-1 FOR -1 USING A1P2 & A1P3, ITEMS 85, 86 & 92 THRU 100. CRIMP LUGS MUST ALSO BE SOLDERED TO THE BRAID INSTALL F1 BETWEEN E101 & E063 ON ITEM 20. INSTALL C1 AS SHOWN ON 32945.
13. INSTALL ITEM 104 (INSULATOR) BETWEEN CARD SLOTS 4 & 5. IF ADJACENT CARD IS NOT USED RETURN ITEM 104 TO STOCK
14.
15. INSTALL W1 THRU W4 (CABLES) FROM ITEM 74 TO ITEMS 22 & 23 (W1 & W2 GO TO ITEM 23). '*' INDICATES POSITION IN WHICH PIN 1 IS LOCATED TYP. (SEE DETAILS 'B' & 'C' FOR FOLDING CABLES).
16. ITEMS 107 PLACED IN CONVENIENT LOCATIONS TO SECURE CABLES TO J1 & J2.
17. BOND ITEM 112 (BUTTONS) TO SWITCH SHAFTS USING ITEM 113. OFFSET OF BUTTONS TO BE DOWN.
18. ITEM 115 (PRGM CARDS) SUPPLIED WITH UNIT ONLY IF ITEM 69 (CARD RDR) IS USED.

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PCM DECOM ASSEMBLY

SIZE	CODE IDENT NO	DRAWING NO	REV
D	06141	[illegible]	[illegible]

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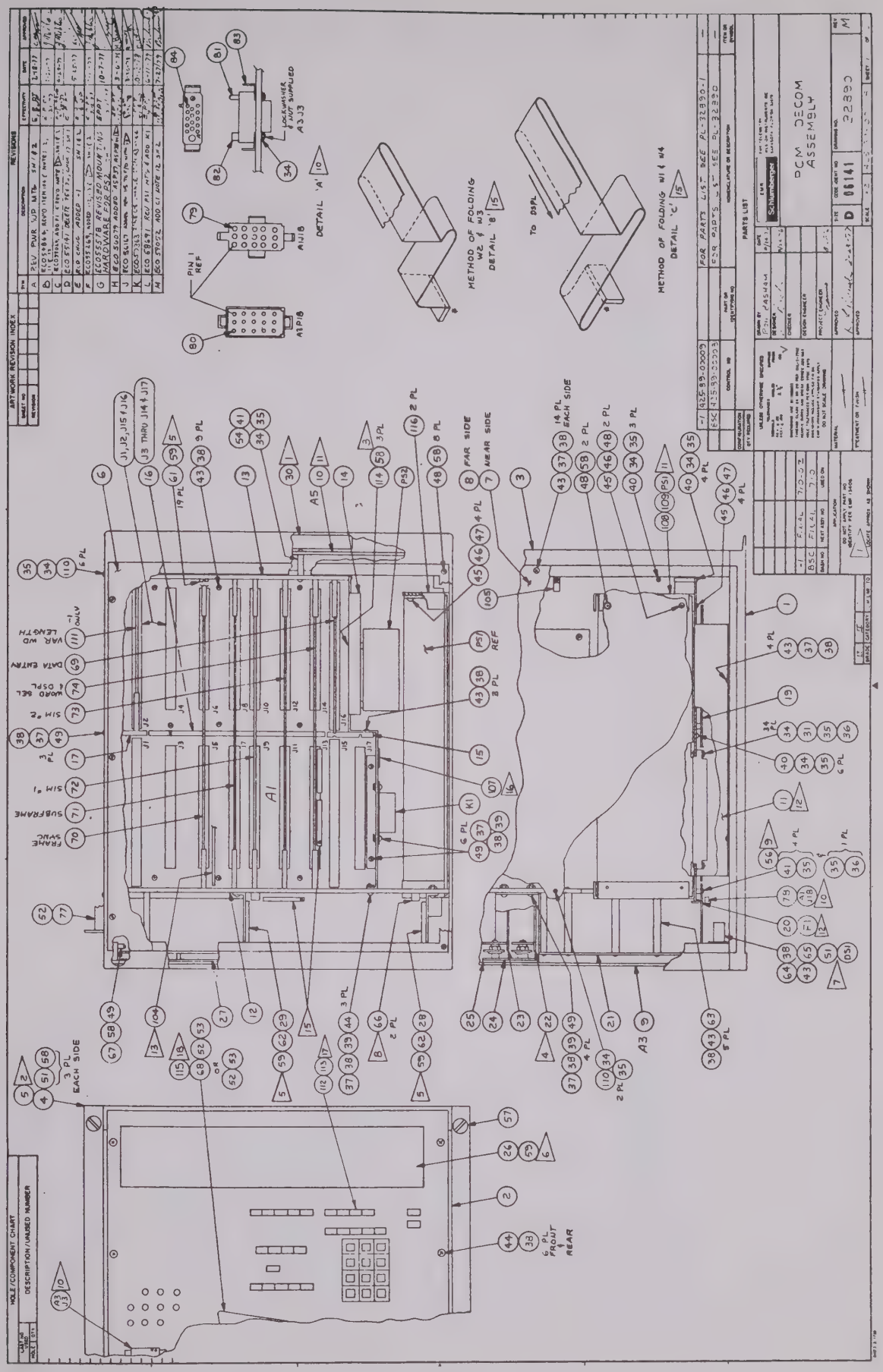


ARTWORK REVISION INDEX
REVISIONS
HOLE/COMPONENT CHART
DESCRIPTION/UNUSED NUMBER
PARTS LIST
DETAIL 'A'
METHOD OF FOLDING W2 & W3 DETAIL 'B'
METHOD OF FOLDING W1 & W4 DETAIL 'C'
LOCKWASHER & NUT SUPPLIED
PIN 1 REF
TO DSPL
FOR PARTS LIST SEE PL-32890-1
FOR PARTS LIST SEE PL-32890
DCM DECOM ASSEMBLY
Schlumberger
06141
32890
FAR SIDE
NEAR SIDE
14 PL EACH SIDE
3 PL EACH SIDE
6 PL FRONT & REAR

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 32890-1 REV DATE 08/16/79 REV LTR F
LIST TITLE - DECOM,PCM,ASSY,MOD 710-02 CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 425-89-00009 ECO 59053 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
58	AR	060-11-00030	GRADE C /#271 RED	CMPD,LOCKING,FINE THREAD	LOCTITE CORP
59	AR	060-11-00019	0151	CMPD,EPOXY,GENL PURPOSE	HYSOL
60	2	239-98-00017	BY DESCRIPTION	SPCR,RND,1/40DX1/8L,#4CL	TRI-TECH
61	17	401-98-00010	1650-F	GUIDE	KSTANFORD
62	4	401-98-00018	1250F	GUIDE,CARD,VERTICAL,NYLON	STANFORD APP
63	6	297-99-00021	33111	STDF,MODIFIED,6-32X3 LG	EMR
64	1	016-99-00329	28202	BRKT,PWR SWITCH MOUNTING	EMR
65	1	290-98-00010	C1560AWW	BUTTON,SWITCH,WHITE .50IN	CLARE-PENDAR
66	2	189-99-00027	21968-86	PAD,2.25X.50X.38THK,RBR	EMR
67	1	239-98-00030	9222-PH-140	SPACER,1/40X1/8L,#6	AMATOM
68	1	999-03-00253	34544	CARD,RDR,*POA/VAR*	EMR
69	1	205-89-01939	34311	PWA,DATA ENTRY	EMR
70	1	205-89-01942	34596	PWA,FRAME SYNC	EMR
71	1	999-02-00327	34544	PWA,SUBFRAME,*POA/VAR*	EMR
72	1	999-04-00161	34544	PWA,SIM,1,*POA/VAR*	EMR
73	1	999-04-00160	34544	PWA,SIM,2,*POA/VAR*	EMR
74	1	205-89-01943	34598	PWA,WD SEL & DSPL	EMR
75	1	205-89-01854	33118	PWA,EXTENDER,FULL WIDTH	EMR
76	1	205-89-01946	34617	PWA,EXTENDER,SINGLE WIDE	EMR
77	1	999-05-00133	34544	SLIDES,*POA/VAR*	EMR
78	1	196-89-00080	28817	PLATE,CONN MTG,SUBASSY	EMR
79	14	065-98-00028	61173-1	CONT,SKT,#30-22AWG TIN	AMP
80	14	065-98-00029	61174-1	CONT,PIN,#30-22AWG TIN	AMP
81	1	194-98-00067	200389-4	PIN,GUIDE,CENTER,MALE	AMP
82	1	194-98-00068	200390-4	PIN,GUIDE,CENTER,FEMALE	AMP
83	1	242-98-00009	201922-1	SPRING,LOCKING,FEMALE	AMP
84	14	065-98-00031	66309-3	CONT,SKT,#24-20AWG GOLD	AMP
85	AR	276-98-00107	NAS-703-26-U-C-9	WIRE,#26,STRD,WHT,600V	MML42
86	AR	276-98-00070	NAS-703-20-U-C-9	WIRE,#20,STRD,WHT,600V	MML42
87	AR	276-02-00097	MIL-W-16878/4*SIL CTD*	WIRE,#26,SOL, TW PR,600V	PRCMT OPTION
88	AR	276-98-00064	NAS-703-18-U-C-9	WIRE,#18,STRD,WHT,600V	MML42
89	AR	276-98-00081	NAS-703-22-U-C-9	WIRE,#22,STRD,WHT,600V	MML42
90	AR	276-98-00157	NAS-703-16-U-C-9	WIRE,#16,STRD,WHT,600V	MML42
91	10	065-98-00026	60619-1	CONT,SKT,#20-14AWG TIN	AMP
92	5	065-98-00027	60620-1	CONT,PIN,#20-14AWG TIN	AMP
93	3	065-98-00029	61174-1	CONT,PIN,#30-22AWG TIN	AMP
94	AR	276-02-00004	MIL-W-16878/4*SIL CTD*	WIRE,#28,SOL, WHT, 600V	PRCMT OPTION
95	AR	276-02-00005	MIL-W-16878/4*SIL CTD*	WIRE,#28,SOL, TW PR,600V	PRCMT OPTION
96	AR	232-98-00006	1233/2	SHIELD,1/2 IN FLAT BRAID	ALPHA WIRE
97	AR	268-98-00013	FIT-105-3/4*BLACK*	TUBING,.750ID,SHRINK	ALPHA WIRE
98	AR	268-02-00039	MIL-I-22129	TUBING,#22,EXTR TEF,CLEAR	PRCMT OPTION
99	10	255-98-00039	RA-1213	TERM,FORK ,22-16AWG	THOMAS BETTS
100	4	140-99-00227	21968-83	INSUL,RECTANGULAR	EMR
101	326	065-98-00005	220-P02	CONT, RELIA-TAC, MALE	AMPHENOL
102	326	065-98-00002	220-S02	CONT,RELIA-TAC,FEMALE	AMPHENOL
103	7	047-98-00001	220-5	CLAMP,CABLE	AMPHENOL
104	1	140-99-00230	21968-87	INSUL,PWA,10.31X15.12	EMR
105	1	047-98-00002	HP-3N	CLAMP,CABLE	BURNDY
107	3	047-98-00026	KKC-4	CLAMP,1/4DIA,KWIK-KLIP	RICHCO
108	2	255-02-00007	MS25036-157	TERM,RING TNG,12-10AWG	PRCMT OPTION
109	3	255-98-00171	YAV8C-L1	TERM,RING TNG, #8AWG	BURNDY
110	AR	229-02-00075	MS51957-15	SCREW,4-40X3/8 PAN HD	PRCMT OPTION
111	1	999-06-00126	34544	PWA,VAR,WD,LG,*POA/VAR*	EMR

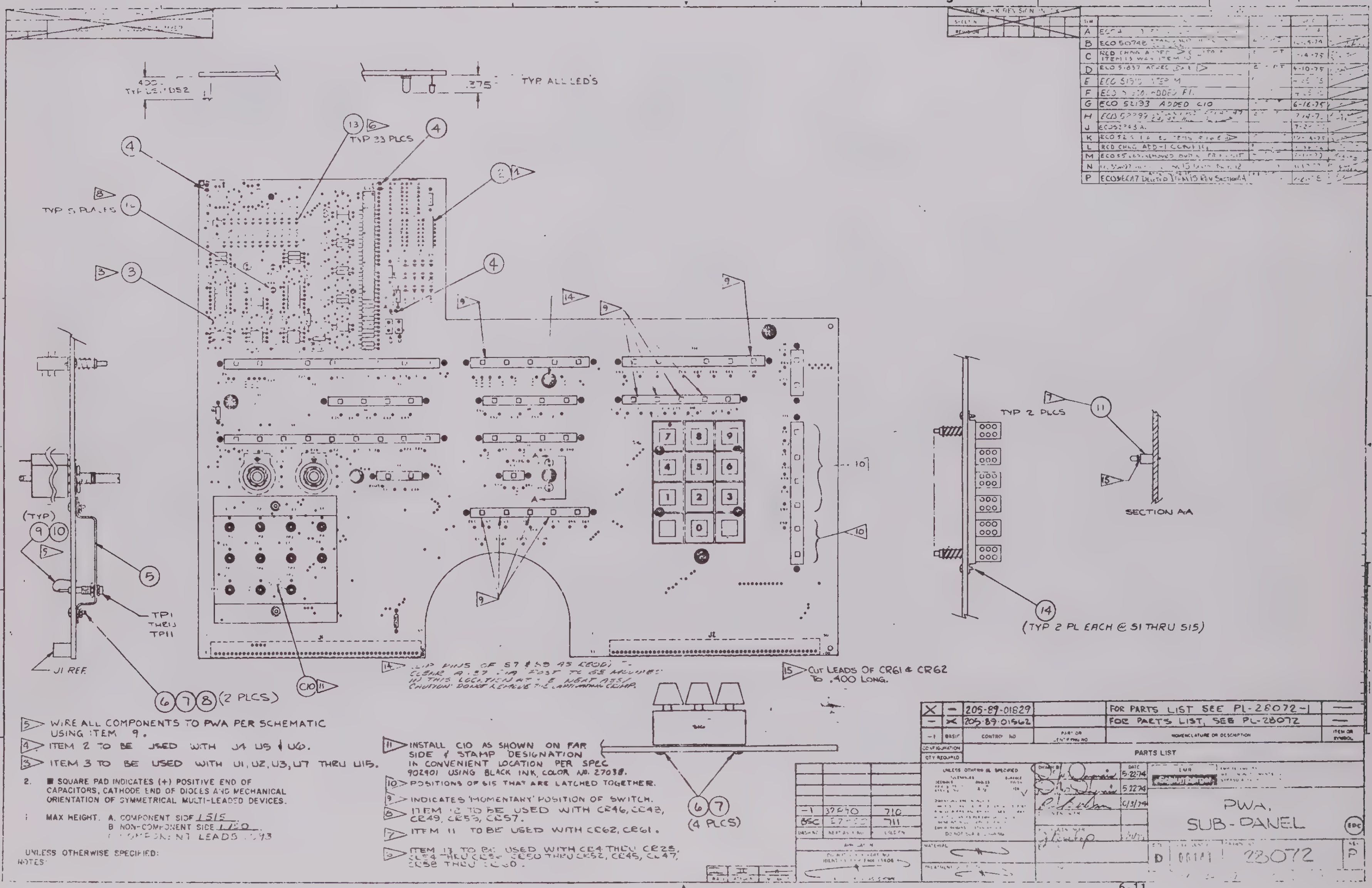
DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 32890-1 REV DATE 08/16/79 REV LTR F

LIST TITLE - DECOM,PCM,ASSY,MOD 710-02 CHGE CONT NO. CODE IDENT 06141 SHT 1 OF

PART NO. - 425-89-00009 ECO 59053 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	2	400-89-00007	25122-1	FRAME,ASSY,BEZEL	EMR
2	2	200-99-00015	25207-6	POST,CORNER,FRONT	EMR
3	2	200-99-00022	25208-6	POST,CORNER,REAR	EMR
4	2	016-89-00136	24569-9	BRKT,ASSY,RACK MT	EMR
5	2	016-89-00194	30556-9	BRKT,RACK MT ASSY,HDL	EMR
6	2	075-89-00081	24600	COVER,TOP/BOTTOM,ASSY	EMR
7	1	191-89-00721	32942	PANEL,SUBASSY,RIGHT SIDE	EMR
8	1	191-89-00720	32941	PANEL,SUBASSY,LEFT SIDE	EMR
9	1	191-89-00702	32893	PANEL,FRONT,SUBASSY	EMR
10	1	191-89-00759	32940-1	PANEL,ASSY,REAR	EMR
11	1	196-89-00101	32895	PLATE,BASE,SUBASSY	EMR
12	1	196-99-00360	32897	PLATE,CARD GUIDE,FRONT	EMR
13	1	196-99-00361	32898	PLATE,CARD GUIDE,REAR	EMR
14	1	016-99-00515	32899	BRKT,CARD GUIDE SUPPORT	EMR
15	1	401-99-00041	32932	GUIDE,CARD,DIVIDER	EMR
16	1	279-99-00159	32937	SPRT,BASE PLATE,CD GUIDE	EMR
17	1	401-99-00043	34545	GUIDE,CARD	EMR
19	1	205-89-01853	33052	PWA,GND TERMINATOR	EMR
20	1	205-89-01830	32944	PWA,PADDLE BOARD	EMR
21	1	205-89-01829	28072-1	PWA,SUBPANEL	EMR
22	1	205-89-01606	28708-1	PWA,DISPLAY DRIVERS	EMR
23	1	205-89-01592	28708	PWA,DISPLAY DRIVERS	EMR
24	1	154-99-00027	28659	LENS,DISPLAY WORD SELECT	EMR
25	1	154-99-00025	28662	LENS,DISPLAY,PROGRAM	EMR
26	1	154-99-00047	28812-1	LENS,DIGITAL DISPLAY	EMR
27	1	154-99-00026	28653	LENS,DISPLAY	EMR
28	1	016-99-01126	39210	BRKT,DISPLAY MOUNTING	EMR
29	1	016-99-01126	39210	BRKT,DISPLAY MOUNTING	EMR
30	1	196-99-00183	10663-1	PLATE,NAME EQUIP IDENT	EMR
31	AR	229-02-00078	MS51957-18	SCREW,4-40X5/8 PAN HD	PRCMT OPTION
34	AR	273-02-00004	MS15795-803	WASHER,#4, FLT ST STL	PRCMT OPTION
35	AR	273-02-00025	MS35333-70	WASHER,#4,INT TOOTH	PRCMT OPTION
36	AR	287-02-00002	MS35649-244	NUT,HEX, 4-40	PRCMT OPTION
37	AR	273-02-00006	MS15795-805	WASHER,#6, FLT ST STL	PRCMT OPTION
38	AR	273-02-00026	MS35333-71	WASHER,#6,INT TOOTH	PRCMT OPTION
39	AR	287-02-00003	MS35649-264	NUT,HEX, 6-32	PRCMT OPTION
40	AR	229-02-00073	MS51957-13	SCREW,4-40X1/4 PAN HD	PRCMT OPTION
41	AR	229-02-00077	MS51957-17	SCREW,4-40X1/2 PAN HD	PRCMT OPTION
43	AR	229-02-00084	MS51957-27	SCREW,6-32X5/16 PAN HD	PRCMT OPTION
44	AR	229-02-00087	MS51957-30	SCREW,6-32X1/2 PAN HD	PRCMT OPTION
45	AR	273-02-00008	MS15795-807	WASHER,#8, FLT ST STL	PRCMT OPTION
46	AR	273-02-00027	MS35333-72	WASHER,#8,INT TOOTH	PRCMT OPTION
47	AR	229-02-00099	MS51957-42	SCREW,8-32X5/16 PAN HD	PRCMT OPTION
48	AR	229-02-00104	MS51957-46	SCREW,8-32X5/8 PAN HD	PRCMT OPTION
49	AR	229-02-00085	MS51957-28	SCREW,6-32X3/8 PAN HD	PRCMT OPTION
50	AR	229-02-00189	MS51959-17	SCREW,4-40X1/2,FLT HD	PRCMT OPTION
51	AR	229-02-00195	MS51959-28	SCREW,6-32X3/8,FLT HD	PRCMT OPTION
52	AR	229-02-00276	MS51958-81	SCREW,10-32X3/8 PAN HD	PRCMT OPTION
53	AR	273-02-00028	MS35333-73	WASHER,#10,INT TOOTH	PRCMT OPTION
54	1	297-98-00057	8402-SS-0440-7/MML 10	STDF,5/16HEX,4-40X1-3/16	MML 10
55	1	070-98-00028	17250	CORD,POWER,W/PLUG & RCPT	BELDEN/MML36
56	1	047-98-00011	HP-11N	CLAMP,CABLE	BURNDY
57	4	229-98-00120	6141-SS-1032-0	SCREW,CAPTIVE PANEL,10-32	AMATOM


TYP ALL LED'S
.375
.400 TYP LED DS2
TYP 33 PLCS
TYP 5 PLACES
TYP 2 PLCS
SECTION AA
(TYP 2 PL EACH @ S1 THRU S15)
(TYP)
TP1 THRU TP11
J1 REF.
(2 PLCS)
(4 PLCS)
CUT LEADS OF CR61 & CR62 TO .400 LONG.
A ECO
B ECO 50748
C RED CHNG ADDED ITEM 15 WAS ITEM 13
D ECO 51037
E ECO 51515
F ECO ADDED F1.
G ECO 52193 ADDED C10
H ECO 52799
J ECO52743A.
K ECO
L RED CHNG ADD -1 CONFIG
M ECO
N ECO
P ECO DELETED ITEM 15 REV SECTION A
5. WIRE ALL COMPONENTS TO PWA PER SCHEMATIC USING ITEM 9.
4. ITEM 2 TO BE USED WITH J4 U5 & U6.
3. ITEM 3 TO BE USED WITH U1, U2, U3, U7 THRU U15.
2. ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.
1. MAX HEIGHT. A. COMPONENT SIDE 1.515 B. NON-COMPONENT SIDE 1.150
UNLESS OTHERWISE SPECIFIED:
NOTES:
11. INSTALL C10 AS SHOWN ON FAR SIDE & STAMP DESIGNATION IN CONVENIENT LOCATION PER SPEC 902901 USING BLACK INK, COLOR NO. 27038.
10. POSITIONS OF S15 THAT ARE LATCHED TOGETHER.
9. INDICATES 'MOMENTARY' POSITION OF SWITCH.
8. ITEM 12 TO BE USED WITH CR46, CR48, CR49, CR53, CR57.
7. ITEM 11 TO BE USED WITH CR62, CR61.
6. ITEM 13 TO BE USED WITH CR4 THRU CR25.
205-89-01829
205-89-01562
FOR PARTS LIST SEE PL-28072-1
FOR PARTS LIST, SEE PL-28072
PARTS LIST
PWA, SUB-PANEL
D 28072
P

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 32890-1 REV DATE 08/16/79 REV LTR F

LIST TITLE - DECOM,PCM,ASSY,MOD 710-02 CHGE CONT NO. CODE IDENT SHT 3 OF

PART NO. - 425-89-00009 ECO 59053 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
112	26	290-97-00018	B-306-GY	BUTTON,SWITCH GRAY	CENTRALAB
113	AR	060-11-00007	RTV 732	CMPD,ADHESIVE,GENERAL-USE	DOW CORNING
114	AR	229-02-00204	MS51959-43	SCREW,8-32X3/8,FLT HD	PRCMT OPTION
115	50	253-12-00001	W40842	CARD,PROGRAM,700 SERIES	IBM
116	2	016-89-00322	40037	BRKT,SUBASSY,PWR SPLY MTG	EMR
117	1	127-02-00019	MS35489-48	GROM,RBR,11/16ID, 1.312OD	PRCMT OPTION
C 1	1	304-20-43009	600	CAP. 430PF 1% 500V	EMR
DS 1	1	151-02-00004	MS25237-328	LAMP,INCAND, 6V 200MA	PRCMT OPTION
F 1	1	120-98-00044	275001	FUSE,SUBMIN,1A @ 125V	LITTELFUSE
J 1	1	063-99-00036	35154	CONN,PWB130CONT,WIRE WRAP	EMR
J 2	1	063-99-00036	35154	CONN,PWB130CONT,WIRE WRAP	EMR
J 3	12	063-98-00276	MDP7000-100	CONN,PWB100CONT,WIRE WRAP	MML3
THRU					
J 14					
J 15	1	063-99-00036	35154	CONN,PWB130CONT,WIRE WRAP	EMR
J 16	1	063-99-00036	35154	CONN,PWB130CONT,WIRE WRAP	EMR
J 17	1	063-98-00276	MDP7000-100	CONN,PWB100CONT,WIRE WRAP	MML3
K 1	1	219-98-00177	KUP11A55 240V	RLY,PWR,2C 10A,240VAC60HZ	P&B/MML87
PS 1	1	202-98-00077	5G5	PWR SPLY,SW RGLTR, 5V 65A	ALPHA-POWER
PS 2	1	999-04-00162	34544	PWR,SPLY,*POA/VAR*	EMR
R 1	1	616-02-10009	RC07GF101J	RES,100 OHM 5% 1/4W	ALLEN BRAD
S 1	1	250-98-00177	S18111	SW,PB LITED ALTN DPST	CLARE-PENDAR
W 1	1	024-89-00091	30151	CABLE,FLAT,ASSY,50 WIRE	EMR
W 2	1	024-89-00092	30151-1	CABLE,FLAT,ASSY,50 WIRE	EMR
W 3	1	024-89-00093	30151-2	CABLE,FLAT,ASSY,50 WIRE	EMR
W 4	1	024-89-00094	30151-3	CABLE,FLAT,ASSY,50 WIRE	EMR
A1J 18	1	063-98-00266	1-480323-0	CONN,RECT, 15 CONT,PLUG	AMP INC
A1P 2	1	063-98-00279	1-480339-0	CONN,RECT, 10 CONT,RCPT	AMP
A1P 3	1	063-98-00263	1-480305-0	CONN,RECT, 3 CONT,RCPT	AMP INC
A3P 3	1	063-98-00242	201298-1	CONN,14 POSN,SOCKET	AMP
A3P 18	1	063-98-00265	1-480324-0	CONN,RECT, 15 CONT,RCPT	AMP INC
A5J 2	1	063-98-00280	1-480285-0	CONN,RECT, 10 CONT,PLUG	AMP
A5J 39	1	063-98-00239	1-480270-0	CONN,RECT, 6 CONT,PLUG	AMP
A5P 30	25	063-98-00063	220-2N052	CONN,RECP,52PIN,R&P	AMPHENOL
THRU					
A5P 34					
A5P 37	1	063-98-00063	220-2N052	CONN,RECP,52PIN,R&P	AMPHENOL
A5P 38	1	063-98-00063	220-2N052	CONN,RECP,52PIN,R&P	AMPHENOL
REF 1	1	905-05-00458	34544	VAR CHART,PCM DECOM	EMR
REF 2	1	905-13-00323	32945	WIRING DIAGRAM,POWER	EMR
REF 3	1	905-25-00066	32938	I/O CONN LIST,MODEL 710	EMR
REF 4	1	905-13-00302	30156	WIRING DIAGRAM,CD&PT RDRS	EMR
REF 5	1	905-07-00300	34469	SPEC,PROD,PCM DECOM	EMR
REF 6	1	905-31-00004	28853	GMTRY TABLE,XY,PWB 28074	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 28072-1 REV DATE 03/16/79 REV LTR G
LIST TITLE - PWA,SUBPANEL CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01829 ECO 57901 06141 CKD BY

ITEM NO. THRU	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
U 6					
REF -1	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR
REF 2	1	905-01-01338	28070	SCHEM,PWA,SUBPANEL	EMR

FIRST MODEL USAGE 0710-

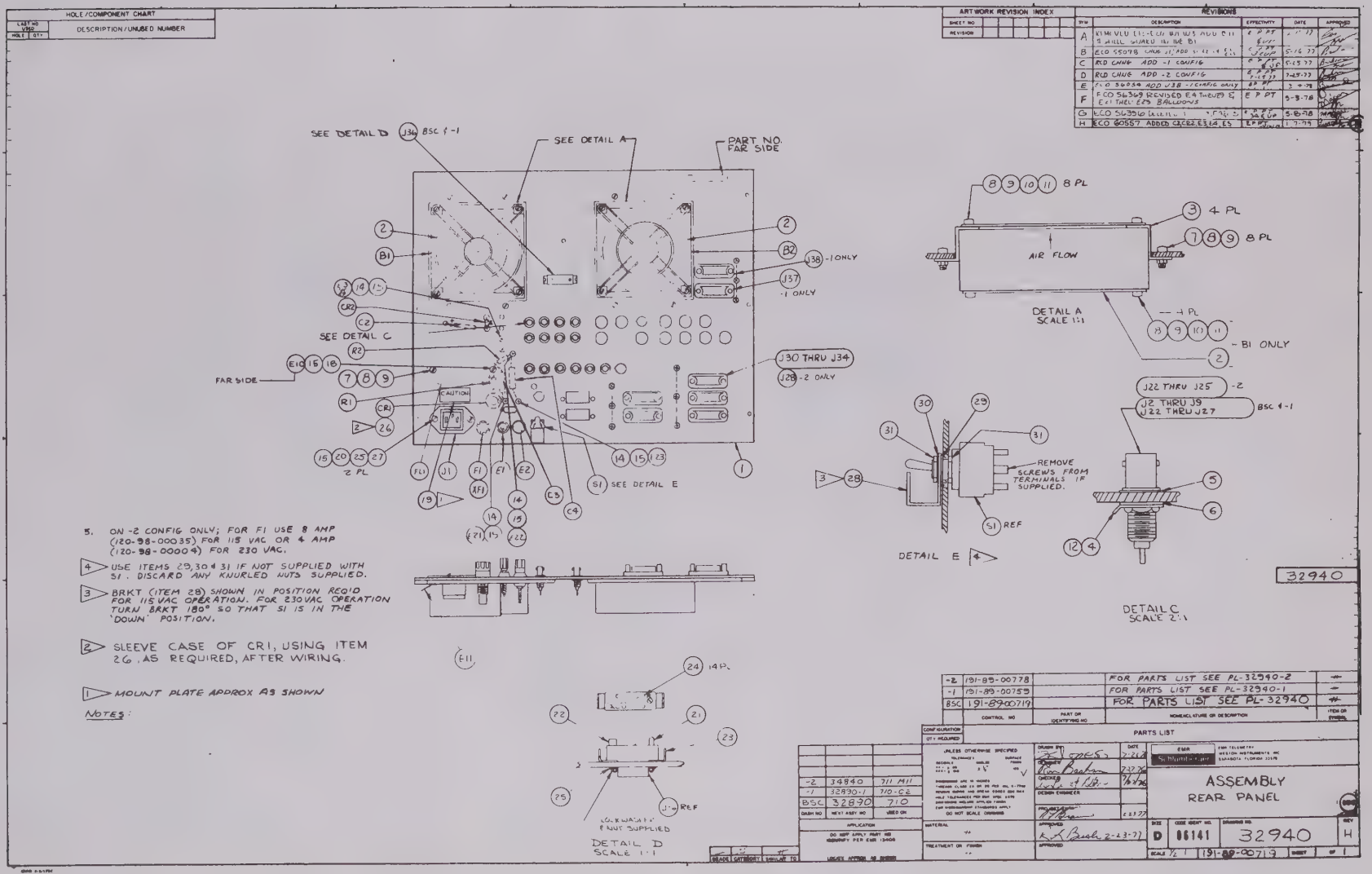
DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 28072-1 REV DATE 03/16/79 REV LTR G

LIST TITLE - PWA,SUBPANEL CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 205-89-01829 ECO 57901 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00505	28071	PWB,SUB-PANEL	EMR
2	3	236-98-00074	6944-265-5	SOCKET,IC,DIP,14PIN,SLDR	ELECT MOLD
4	2	134-98-00026	BEPHB	HOLDER,LAMP BASE BLACK	SHELLY INC
5	1	016-89-00251	28786-1	BRKT,SUBASSY,TEST PT MTG	EMR
6	AR	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT OPTION
7	AR	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
8	AR	287-02-00001	MS35649-224	NUT,HEX, 2-56	PRCMT OPTION
9	AR	276-99-00008	619-22	WIRE,#22,BUSS,SOLID	EMR
10	AR	268-02-00039	MIL-I-22129	TUBING,#22,EXTR TEF,CLEAR	PRCMT OPTION
11	2	134-98-00030	Q086-23D	HLDR,LED,WIRE WRAP TAILS	ELDEMA
12	3	189-99-00003	800-7	PAD,XSTR 4 PIN*USE OPTL*	EMR
13	9	189-98-00004	100-000-NY	PAD,XSTR 4 PIN*USE OPTL*	DEL BLINN
14	14	229-98-00146	BY DESCRIPTION	SCREW,#4X3/8 PAN HD,CD PL	RRCMT OPTION
15	2	239-98-00090	9225-N-140-0	SPACER, 1/4 OD X 5/16L	AMATOM
CR 49	1	137-98-00018	FLV110	IND,LED,RED,.285L,.230 OD	MML41
CR 50	3	137-98-00006	TIL209/TIL209A	IND,LED RED, 15UW AT 20MA	TI
THRU					
CR 52					
CR 53	1	137-98-00018	FLV110	IND,LED,RED,.285L,.230 OD	MML41
CR 54	3	137-98-00006	TIL209/TIL209A	IND,LED RED, 15UW AT 20MA	TI
THRU					
CR 56					
CR 57	1	137-98-00018	FLV110	IND,LED,RED,.285L,.230 OD	MML41
CR 58	5	137-98-00006	TIL209/TIL209A	IND,LED RED, 15UW AT 20MA	TI
THRU					
CR 62					
DS 2	1	151-98-00034	715	LAMP,INCAND, 5V 115MA	SHELLY INC
DS 3	1	151-98-00034	715	LAMP,INCAND, 5V 115MA	SHELLY INC
F 1	1	120-98-00045	275002	FUSE,SUBMIN,2A @ 125V	LITTELFUSE
J 1	1	063-98-00283	252-50-30-360	CONN,100CONT@.100,1/16PWB	CINCH
J 2	1	063-98-00283	252-50-30-360	CONN,100CONT@.100,1/16PWB	CINCH
R 67	3	616-02-15009	RC07GF151J	RES,150 OHM 5% 1/4W	ALLEN BRAD
THRU					
R 69					
R 98	1	616-02-15009	RC07GF151J	RES,150 OHM 5% 1/4W	ALLEN BRAD
R 99	1	182-98-00013	898-3-R220	NTWK,RES, 8/220OHM 2% 1W	BECK/MML47
R 100	1	182-98-00013	898-3-R220	NTWK,RES, 8/220OHM 2% 1W	BECK/MML47
R 104	1	616-02-15009	RC07GF151J	RES,150 OHM 5% 1/4W	ALLEN BRAD
R 105	1	276-98-00196	J0.500X0.250T22	WIRE,JUMPER,#22 SOLID .5L	MML42
S 7	1	250-99-00093	24111-15	SW,PB,5STA,1MOM,2 2INTLK	EMR
S 8	1	250-99-00091	24111-13	SW,PB,2STA,2INTLK,GY BTN	EMR
S 10	1	250-99-00094	24111-16	SW,PB,5STA,4MOM,1ALTN, GY	EMR
S 11	1	250-99-00092	24111-14	SW,PB,4STA,4INTLK,GY BTN	EMR
S 12	1	250-99-00094	24111-16	SW,PB,5STA,4MOM,1ALTN, GY	EMR
S 13	1	250-98-00223	027639	SW,PB,1STA,DPST MOM	CENTRALAB
S 14	1	250-99-00135	24111-37	SW,PB,6 STA,4INTLK	EMR
S 16	1	253-61-00001	12NW7-1	KYBD,ADD MACH FORMAT,1.9W	MICRO SWITCH
TP 1	8	143-98-00028	105-201-200	JACK,TEST PT,PNL MT,WHT	E.F. JOHNSON
THRU					
TP 8					
TP 10	1	143-98-00028	105-201-200	JACK,TEST PT,PNL MT,WHT	E.F. JOHNSON
TP 11	1	143-98-00028	105-201-200	JACK,TEST PT,PNL MT,WHT	E.F. JOHNSON
U 4	3	435-98-00010	5082-7730	DSPL,LED 7-SEG RED .3IN	H-P/MML41


HOLE/COMPONENT CHART
DESCRIPTION/UNUSED NUMBER
ARTWORK REVISION INDEX
REVISIONS
DESCRIPTION
EFFECTIVITY
DATE
APPROVED
SEE DETAIL D
SEE DETAIL A
PART NO. FAR SIDE
SEE DETAIL C
FAR SIDE
CAUTION
J30 THRU J34
J28 -2 ONLY
J36 BSC 1-1
J38 -1 ONLY
J37 -1 ONLY
SEE DETAIL E
8 PL
4 PL
8 PL
AIR FLOW
DETAIL A
SCALE 1:1
4 PL
B1 ONLY
J22 THRU J25 -2
J2 THRU J9
J22 THRU J27
BSC 1-1
REMOVE SCREWS FROM TERMINALS IF SUPPLIED.
REF
DETAIL E
DETAIL C
SCALE 2:1
32940
14 PL
LOCKWASHER & NUT SUPPLIED
REF
DETAIL D
SCALE 1:1
5. ON -2 CONFIG ONLY; FOR F1 USE 8 AMP (120-98-00035) FOR 115 VAC OR 4 AMP (120-98-00004) FOR 230 VAC.
4 USE ITEMS 29, 30 & 31 IF NOT SUPPLIED WITH S1. DISCARD ANY KNURLED NUTS SUPPLIED.
3 BRKT (ITEM 28) SHOWN IN POSITION REQ'D FOR 115 VAC OPERATION. FOR 230 VAC OPERATION TURN BRKT 180° SO THAT S1 IS IN THE 'DOWN' POSITION.
2 SLEEVE CASE OF CR1, USING ITEM 26, AS REQUIRED, AFTER WIRING.
1 MOUNT PLATE APPROX AS SHOWN
NOTES:
-2 191-89-00778 FOR PARTS LIST SEE PL-32940-2
-1 191-89-00759 FOR PARTS LIST SEE PL-32940-1
BSC 191-89-00719 FOR PARTS LIST SEE PL-32940
PARTS LIST
-2 34840 711 MII
-1 32930-1 710-02
BSC 32930 710
ASSEMBLY
REAR PANEL
D 06141 32940 H
191-89-00719

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 32940-1 REV DATE REV LTR C

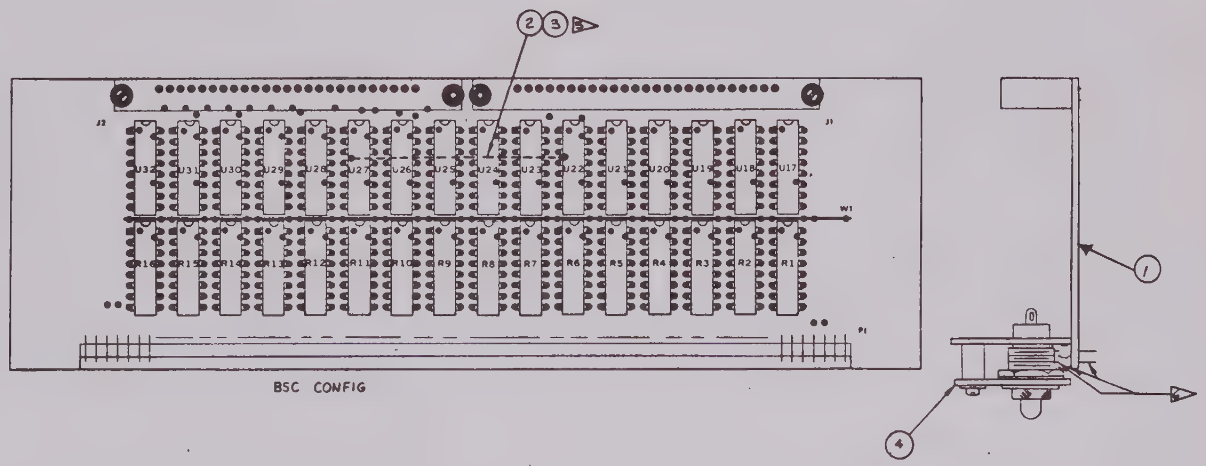
LIST TITLE - PANEL,ASSY,REAR CHGE CONT NO. CODE IDENT 06141 SHT 1 OF

PART NO. - 191-89-00759 ECO RECORD 1 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	191-89-00703	32894	PANEL,REAR,SUBASSY	EMR
2	3	126-98-00001	476042	GRILLE,FAN FINGER GUARD	MML44
3	4	016-99-00359	28789	BRKT,FAN MOUNTING	EMR
4	14	255-98-00012	1497	TERM,SLDR LUG,3/8 STUD	H.H.SMITH
5	14	022-98-00002	10221-N	BSHG,NYLON,BNC CONNECTOR	MILTON ROSS
6	14	273-98-00045	5620-89-62	WASHER,PHENOLIC .385 ID	SEASTROM
7	AR	229-02-00086	MS51957-29	SCREW,6-32X7/16 PAN HD	PRCMT OPTION
8	AR	287-02-00003	MS35649-264	NUT,HEX, 6-32	PRCMT OPTION
9	AR	273-02-00006	MS15795-805	WASHER,#6, FLT ST STL	PRCMT OPTION
10	AR	229-02-00089	MS51957-32	SCREW,6-32X3/4 PAN HD	PRCMT OPTION
11	AR	273-02-00026	MS35333-71	WASHER,#6,INT TOOTH	PRCMT OPTION
12	AR	060-11-00002	GRADE H /#222 PURPLE	CMPD,LOCKING,FINE THREAD	LOCTITE CORP
14	AR	229-02-00073	MS51957-13	SCREW,4-40X1/4 PAN HD	PRCMT OPTION
15	AR	273-02-00025	MS35333-70	WASHER,#4,INT TOOTH	PRCMT OPTION
18	AR	229-02-00074	MS51957-14	SCREW,4-40X5/16 PAN HD	PRCMT OPTION
19	1	999-01-03248	34544	PLATE,CAUTION,*POA/VAR*	EMR
20	AR	287-02-00002	MS35649-244	NUT,HEX, 4-40	PRCMT OPTION
21	1	194-98-00067	200389-4	PIN,GUIDE,CENTER,MALE	AMP
22	1	194-98-00068	200390-4	PIN,GUIDE,CENTER,FEMALE	AMP
23	1	242-98-00009	201922-1	SPRING,LOCKING,FEMALE	AMP
24	14	065-98-00031	66309-3	CONT,SKT,#24-20AWG GOLD	AMP
25	AR	273-02-00004	MS15795-803	WASHER,#4, FLT ST STL	PRCMT OPTION
26	AR	268-98-00012	RNF-100-3/8-WHT	TBG, 3/8 ,THERMO-FIT,WHT	RACHEM/MML82
27	AR	229-02-00076	MS51957-16	SCREW,4-40X7/16 PAN HD	PRCMT OPTION
28	1	016-99-00568	34203	BRKT,TOGGLE SW LOCKING	EMR
29	1	273-02-00065	MS25081-C4	WASHER,KEYED,FOR.468 BSHG	PRCMT OPTION
30	1	273-02-00066	MS35333-121	WASHER,7/16,INT TOOTH	PRCMT OPTION
31	2	287-02-00026	MS25082-C21	NUT,HEX,.469-32,.093THK	PRCMT OPTION
B 1	1	999-01-03249	34544	BLOWER,FAN,*POA/VAR*	EMR
B 2	1	999-01-03249	34544	BLOWER,FAN,*POA/VAR*	EMR
C 3	1	999-01-03250	34544	CAP,*POA/VAR*	EMR
C 4	1	999-01-03255	34544	CAP,*POA/VAR*	EMR
CR 1	1	999-01-03251	34544	XSTR,TRIAC,*POA/VAR*	EMR
E 1	1	200-98-00003	GP30NC/1835	POST,BINDING,5WAY MET	SUP/HH SMITH
E 2	1	200-98-00001	DF30BC/257-103	POST,BINDING,5WAY BLK	SUP/HH SMITH
E 6	5	255-98-00169	4814-1-0516	TERM,STDF,INSULATED,TAP	CAMBRIDGE
THRU					
E 10					
E 11	1	255-98-00013	1466	TERM,LUG,#6,SOLDER	H H SMITH
E 21	3	255-98-00154	4838-1-0516	TERM,STDF,INSULATED,TAP	CTC
THRU					
E 23					
F 1	1	999-01-03252	34544	FUSE,*POA/VAR*	EMR
FL 1	1	114-98-00081	10JX5010	FLTR,LINE 125 OR 250VAC	SPRAG/MML63
J 1	1	063-98-00343	EAC-301	CONN,RECT, 3 CONT,RCPT	SWCRFT/MML76
J 2	8	063-02-00014	UG-1094A/U	CONN,RCPT,BHD,BNC COAX	QVL
THRU					
J 9					
J 22	6	063-02-00014	UG-1094A/U	CONN,RCPT,BHD,BNC COAX	QVL
THRU					
J 27					
J 30	5	063-98-00056	220-1N052	CONN,PLUG,52PIN,R&P	AMPHENOL
THRU					

REVISIONS

LTR	DESCRIPTION		DATE	APPROVED
A	ECO 49839 RE-DESIGN	[illegible]	[illegible]	[illegible]
B	ECO50995 ADD [flag] SHTS 1 & 2	[illegible]	11-21-74	[illegible]
C	ECO57224 REVD NOTE [flag] SHT 1	[illegible]	[illegible]	[illegible]
D	ECO55351 REV D NOTE [flag] SHT 1 & 2	[illegible]	[illegible]	[illegible]
E	ECO58258 MAX HEIGHT NON-COMPONENT SIDE WAS .293	[illegible]	4/17/79	[illegible]
F	ECO 59367 ADDED (NOTE FIRST PIN ON P1 ITEM 4 IS PIN 3.) TO NOTE 4. MADE NOTE 4 A FLAG NOTE, 6 ADDED TO SHT 2.	[illegible]	9-25-79	[illegible]



BSC CONFIG

6 AFTER ASSY OF ITEMS 1 & 4, MARK THE CONNECTING PINS TOP & BOTTOM OF CARD WHERE SHOWN PLUS CARD EDGE OF ITEM 1. (BLACK) AND ACROSS THE FRONT END OF ITEM 1

5 FOR BSC ONLY ADD JUMPERS AS SHOWN ON FAR SIDE OF PWA

4 P1-P3 OF ITEM 4 IS TO ALIGN WITH P1-P3 OF ITEM 1. (NOTE FIRST PIN ON P1, ITEM 4, IS PIN 3)

3 FOR -1 CONFIG. ONLY, ADD JUMPERS AS SHOWN, USING ITEMS 2 & 3, & LISTED IN TABLE I.

2. ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.

1 MAX HEIGHT A. COMPONENT SIDE .290 NOTE: J1&J2 ARE .680
B NON-COMPONENT SIDE .200.

UNLESS OTHERWISE SPECIFIED:
NOTES

	—	205-89-01606	FOR PARTS LIST SEE PL-28708-1	
—		205-89-01592	FOR PARTS LIST SEE PL-28708	

PARTS LIST

-1	28757-1	711
BSC	28757	711

R. BUCHANAN

Schlumberger

PWA, DISPLAY DRIVERS

D 06141 28708 F

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 32940-1 REV DATE REV LTR C

LIST TITLE - PANEL,ASSY,REAR CHGE CONT NO. CODE IDENT SHT 2 OF

PART NO. - 191-89-00759 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
J 34					
J 36	1	063-98-00242	201298-1	CONN,14 POSN,SOCKET	AMP
J 37	1	063-98-00056	220-1N052	CONN,PLUG,52PIN,R&P	AMPHENOL
J 38	1	063-98-00056	220-1N052	CONN,PLUG,52PIN,R&P	AMPHENOL
R 1	1	999-01-03253	34544	RES,*POA/VAR*	EMR
R 2	1	999-01-03254	34544	RES,*POA/VAR*	EMR
S 1	1	250-98-00288	MS25068-23	SW,TOGGLE,4PDT,15A@125VAC	MML17
XF 1	1	134-98-00006	342004-L	HLDR,FUSE,3AG,RTANG TERM	MML71
REF 1	1	905-05-00458	34544	VAR CHART,PCM DECOM	EMR

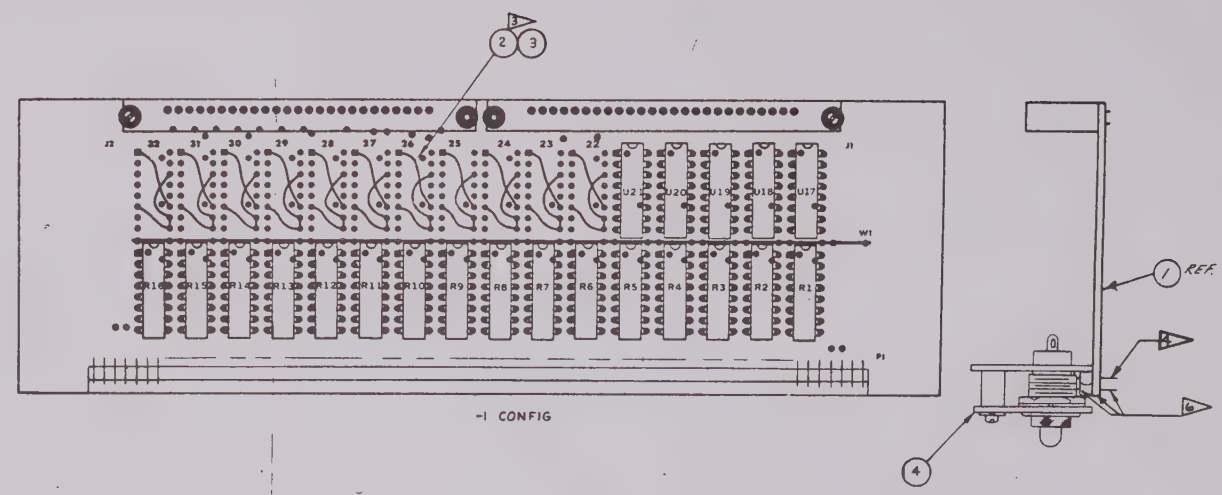
FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 28708 REV DATE 06/11/79 REV LTR A
LIST TITLE - PWA,DISPLAY DRIVERS CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01592 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-99-01062	28707	PWB,DISPLAY DRIVERS	EMR
4	1	205-89-01591	28706	PWA,DISPLAY	EMR
J 1	1	063-98-00278	3433-2002	CONN,50 PIN SCOTCHFLEX	3M/MML70
J 2	1	063-98-00278	3433-2002	CONN,50 PIN SCOTCHFLEX	3M/MML70
R 1	11	182-98-00013	898-3-R220	NTWK,RES, 8/2200HM 2% 1W	BECK/MML47
THRU					
R 11					
R 13	4	182-98-00013	898-3-R220	NTWK,RES, 8/2200HM 2% 1W	BECK/MML47
THRU					
R 16					
U 17	11	046-97-00091	SN7446AN	IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32
THRU					
U 27					
U 29	4	046-97-00091	SN7446AN	IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32
THRU					
U 32					
W 1	1	021-99-00032	30080	BUSBAR,LAM,.32H,17 GROUPS	EMR
REF 1	1	905-01-01358	28704	SCHEM,PWA,DISPLAY	EMR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR

FIRST MODEL USAGE 0711-01

TABLE I
JUMPER
P1 — P11
P6 — P9
P9 — P10
P10 — P14
U22 THRU U32



-1 CONFIG

Schlumberger			
PWA, DISPLAY DRIVERS			
SIZE D	CODE IDENT NO. 06141	DRAWING NO. 28708	REV F
SCALE 2/1	2-5-89	SHEET 2 OF 2	

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

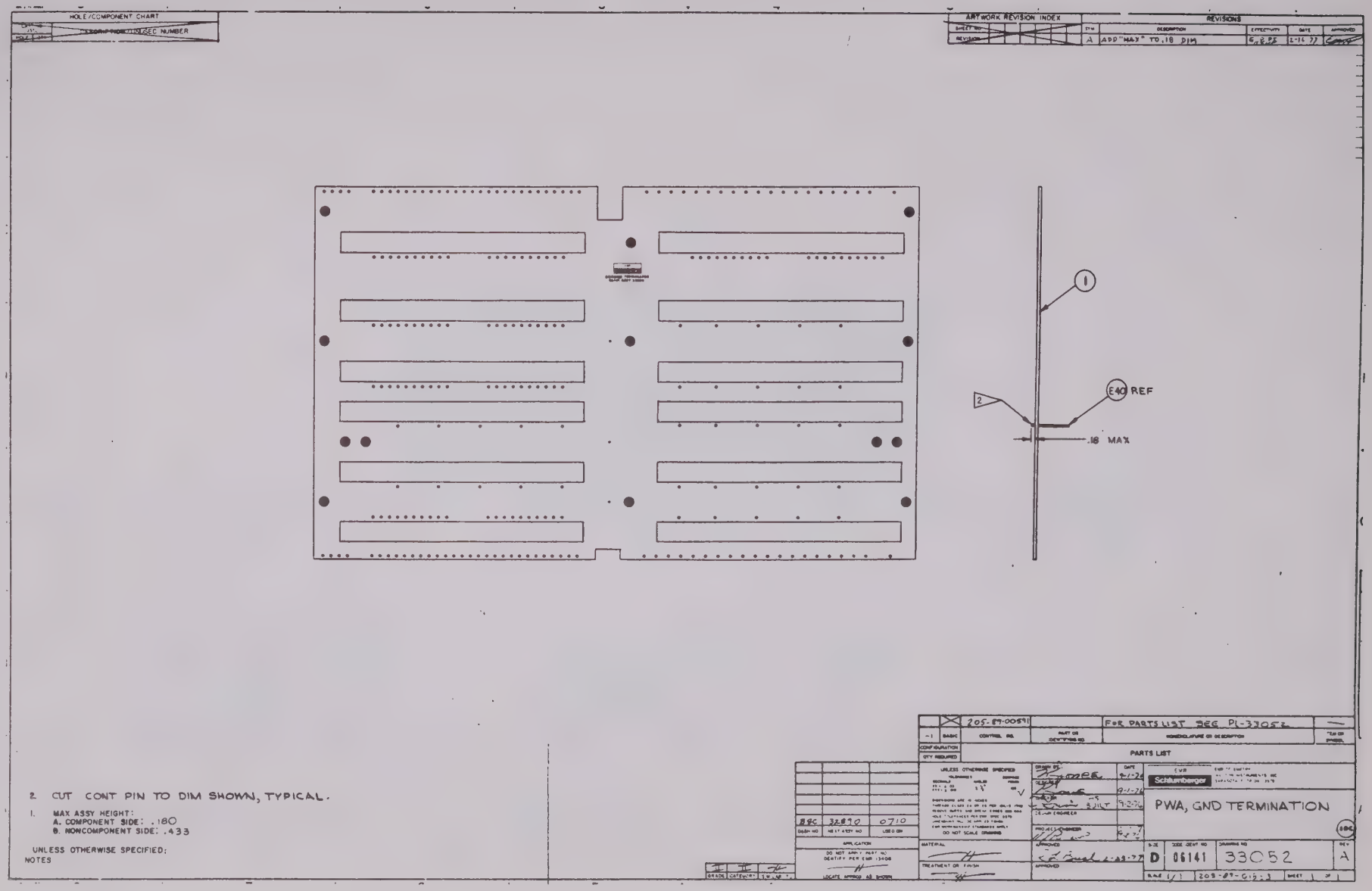
PARTS LIST - 28708-1 REV DATE 06/11/79 REV LTR A

LIST TITLE - PWA,DISPLAY DRIVERS CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 205-89-01606 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-99-01062	28707	PWB,DISPLAY DRIVERS	EMR
2	AR	276-99-00008	619-22	WIRE,#22,BUSS,SOLID	EMR
3	AR	268-02-00046	MIL-I-22129	TUBING,#22,EXTR TEF,WHT	QVL
4	1	205-89-01593	28706-1	PWA, DISPLAY	EMR
J 1	1	063-98-00278	3433-2002	CONN,50 PIN SCOTCHFLEX	3M/MML70
J 2	1	063-98-00278	3433-2002	CONN,50 PIN SCOTCHFLEX	3M/MML70
R 1	16	182-98-00013	898-3-R220	NTWK,RES, 8/220OHM 2% 1W	BECK/MML47
THRU R 16					
U 17	5	046-97-00091	SN7446AN	IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32
THRU U 21					
W 1	1	021-99-00032	30080	BUSBAR,LAM,.32H,17 GROUPS	EMR
REF 1	1	905-01-01360	28749	SCHEM,PWA,DISPLAY	EMR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR

FIRST MODEL USAGE 0711-01


HOLE/COMPONENT CHART
DESCRIPTION/USE SEC NUMBER
ARTWORK REVISION INDEX
REVISIONS
A ADD "MAX" TO .18 DIM
1
2
E40 REF
.18 MAX
205-89-00591
FOR PARTS LIST SEE PL-33052
PARTS LIST
PWA, GND TERMINATION
Schlumberger
D 06141 33052 A
2. CUT CONT PIN TO DIM SHOWN, TYPICAL.
1. MAX ASSY HEIGHT:
A. COMPONENT SIDE: .180
B. NONCOMPONENT SIDE: .433
UNLESS OTHERWISE SPECIFIED:
NOTES
DO NOT SCALE DRAWING
DO NOT APPLY PART NO
DENTIFY PER EMR 13406
LOCATE APPROX AS SHOWN
DRAWN BY
DESIGN ENGINEER
PROJECT ENGINEER
MATERIAL
TREATMENT OR FINISH
APPROVED
GRADE
CATEGORY

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 33052 REV DATE 08/20/77 REV LTR A
LIST TITLE - PWA,GND TERMINATOR CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01853 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
13E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
14E 1	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
14E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
14E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
14E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
14E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 2	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 24	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 26	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 28	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 52	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 54	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 56	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 58	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 60	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 62	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
15E 64	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 3	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 9	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 15	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT

DATE 01/14/80 8MG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 33052 REV DATE 08/20/77 REV LTR A
LIST TITLE - PWA,GND TERMINATOR CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01853 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD.	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
	1	204-89-00591	33051	PWB,GND TERMINATOR	EMR
J1E 2	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 24	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 26	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 28	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 52	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 54	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 56	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 58	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 60	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 62	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J1E 64	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
10E 1	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
10E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
10E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
10E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
10E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
11E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
11E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
11E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
11E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
11E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
12E 1	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
12E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
12E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
12E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
12E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
13E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 33052 REV DATE 08/20/77 REV LTR A
LIST TITLE - PWA,GND TERMINATOR CHGE CONT NO. CODE IDENT SHT 4 OF
PART NO. - 205-89-01853 ECO RECORD 1 06141 CKD BY,

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
J3E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J4E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J5E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J6E 1	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J6E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J6E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J6E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J6E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 33052 REV DATE 08/20/77 REV LTR A

LIST TITLE - PWA,GND TERMINATOR CHGE CONT NO. CODE IDENT SHT 3 OF

PART NO. - 205-89-01853 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
16E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 21	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 24	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 27	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 33	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 39	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 45	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 51	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 54	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 57	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
16E 63	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 3	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 9	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 15	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 21	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 24	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 27	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 33	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 39	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 45	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 51	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 54	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 57	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J2E 63	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 4	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 6	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 8	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 14	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J3E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT

HOLE/COMPONENT CHART

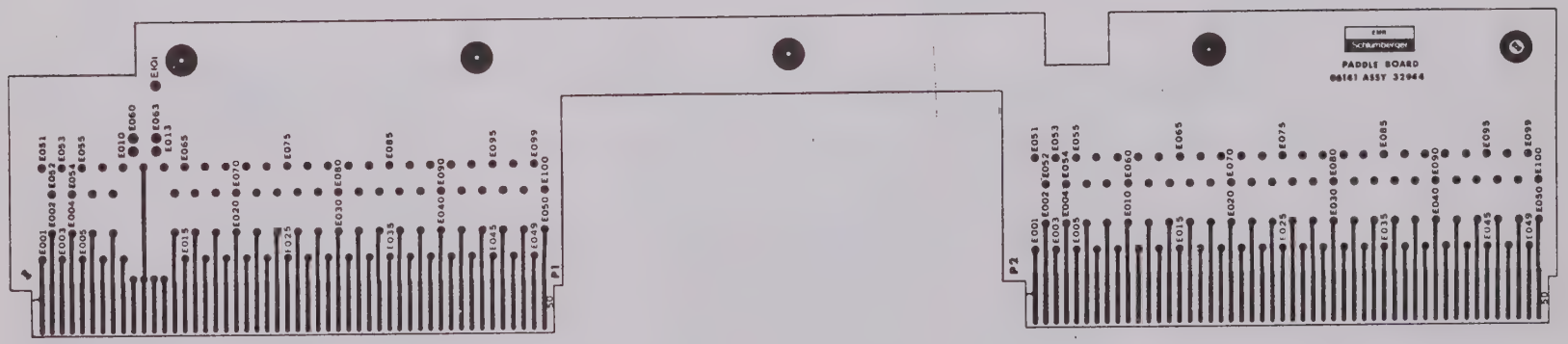
REV	DESCRIPTION/DRAWING NUMBER

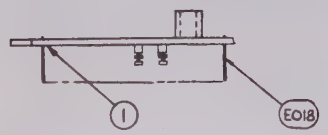
ARTWORK REVISION INDEX

SHEET NO	REVISION

REVISIONS

REV	DESCRIPTION	EFFECTIVITY	DATE	APPROVED
A	MOVED MTG HOLE TO AGREE WITH CLUSTER CWB	6 PCS	1-18-77	
B	ECO 77052 - DELETED P1	6 PCS	3-31-77	





1. MAX HEIGHT : A. COMPONENT SIDE .466
B. NON-COMPONENT SIDE .800

NOTES :

X	205-89-0110		FOR PARTS LIST SEE PL-32944	
-1	BASIC	CONTROL NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
CONFIGURATION				PARTS LIST
QTY REQUIRED				

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES

DO NOT SCALE DRAWING

MATERIAL

APPLICATION

DRAWN Bonk 7-28-77

CHECKED

DESIGN ENGINEER

APPROVED 2-28-77

Schlumberger

PWA, PADDLE BOARD

BSC 32890	710

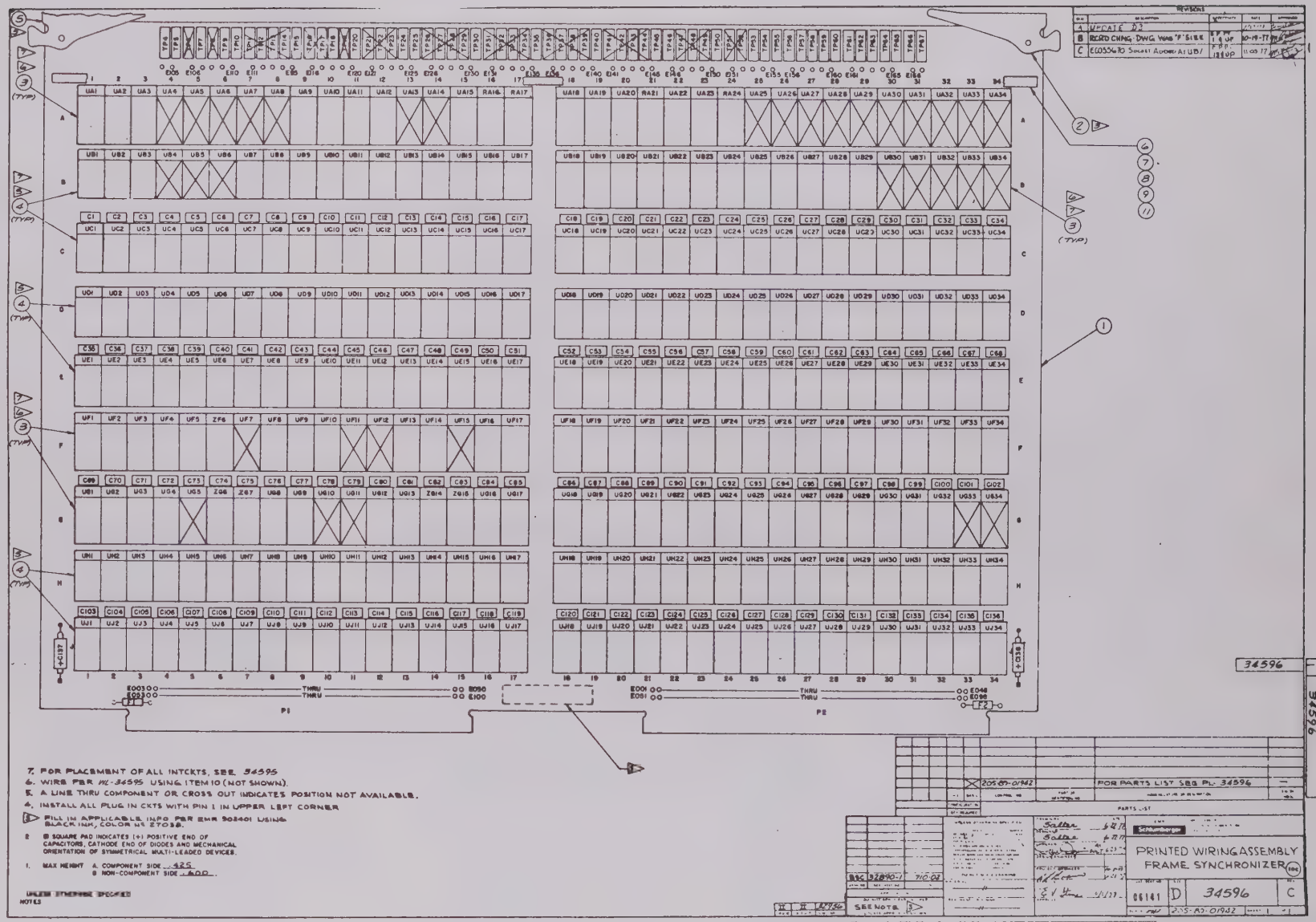
SIZE	CODE IDENT NO	DRAWING NO	REV
D	06141	32944	B

SCALE 2/1 | 205-8*-C 0.0. | SHEET | OF

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 33052 REV DATE 08/20/77 REV LTR A
LIST TITLE - PWA,GND TERMINATOR CHGE CONT NO. CODE IDENT SHT 5 OF
PART NO. - 205-89-01853 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
J7E 16	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 18	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 22	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 32	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 34	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 36	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 38	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 42	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 44	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 46	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 48	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J7E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J8E 1	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J8E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J8E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J8E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J8E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J9E 10	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J9E 20	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J9E 30	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J9E 40	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
J9E 50	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
REF 1	1	905-01-01339	28073	SCHEM,PWA INTERCONNECT	EMR

FIRST MODEL USAGE 0710-


REVISIONS
A UPDATE D2
B RCRD CHNG. DWG WAS 'F' SIZE
C E0055670 SOCKET ADDED AS UB1
P1
P2
34596
7. FOR PLACEMENT OF ALL INTCKTS, SEE 34595
6. WIRE PER WL-34595 USING ITEM 10 (NOT SHOWN).
5. A LINE THRU COMPONENT OR CROSS OUT INDICATES POSITION NOT AVAILABLE.
4. INSTALL ALL PLUG IN CKTS WITH PIN 1 IN UPPER LEFT CORNER
3 FILL IN APPLICABLE INFO PER EMR 902401 USING BLACK INK, COLOR No 27038.
2 ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.
1. MAX HEIGHT A. COMPONENT SIDE .425 B. NON-COMPONENT SIDE .600
UNLESS OTHERWISE SPECIFIED
NOTES
205-89-01942
FOR PARTS LIST SEE PL-34596
PARTS LIST
Schlumberger
PRINTED WIRING ASSEMBLY
FRAME SYNCHRONIZER
06141
D
34596
C
205-89-01942
SEE NOTE 3

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 32944 REV DATE 08/20/77 REV LTR A

LIST TITLE - PWA,PADDLE BOARD CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 205-89-01830 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00585	32943	PWB,PADDLE BOARD	EMR
P1E 1 THRU P1E 9	9	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 11	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 12	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 14 THRU P1E 59	46	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 61	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 62	1	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 64 THRU P1E100	37	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 1 THRU P2E100	100	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
REF 1	1	905-13-00323	32945	WIRING DIAGRAM,POWER	EMR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR

FIRST MODEL USAGE 0710-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34596 REV DATE 12/20/79 REV LTR C
LIST TITLE - PWA,FRAME SYNC CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01942 ECO 60254 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
TP 67	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
UA 1	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UA 2	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UA 3	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UA 9	4	046-97-00067	SN7483AN	IC,TTL ADDR,BIN 4BIT FULL	TI/MML32
THRU					
UA 12					
UA 15	1	046-97-00066	SN7476N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UA 18	1	046-97-00071	SN7493N	IC,TTL CNTR,BIN 4-BIT	TI/MML32
UA 19	1	046-97-00067	SN7483AN	IC,TTL ADDR,BIN 4BIT FULL	TI/MML32
UA 20	1	046-97-00067	SN7483AN	IC,TTL ADDR,BIN 4BIT FULL	TI/MML32
UA 22	1	046-97-00069	SN7490N	IC,TTL CNTR,DECADE ASYN	TI/MML32
UA 23	1	046-97-00069	SN7490N	IC,TTL CNTR,DECADE ASYN	TI/MML32
UB 1	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UB 2	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UB 3	1	046-97-00088	SN7432N	IC,TTL GATE,OR 2-INP	TI/MML32
UB 7	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UB 8	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UB 9	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UB 10	5	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
THRU					
UB 14					
UB 15	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UB 16	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UB 17	1	046-97-00048	SN7405N	IC,TTL INV,OPEN-COLL 5.5V	TI/MML32
UB 18	3	046-97-00178	SN74174N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UB 20					
UB 21	1	046-97-00175	SN74185AN	IC,TTL CONV,BIN-TO-BCD	TI/MML32
UB 22	1	046-97-00175	SN74185AN	IC,TTL CONV,BIN-TO-BCD	TI/MML32
UB 23	1	046-97-00089	SN7442N	IC,TTL DCDR,BCD-TO-DEC	TI/MML32
UB 24	1	046-97-00089	SN7442N	IC,TTL DCDR,BCD-TO-DEC	TI/MML32
UB 25	1	046-97-00175	SN74185AN	IC,TTL CONV,BIN-TO-BCD	TI/MML32
UB 26	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UB 27	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UB 28	1	046-97-00091	SN7446AN	IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32
UB 29	1	046-97-00091	SN7446AN	IC,TTL DCDR/DRVR,BCD-7SEG	TI/MML32
UC 1	17	046-97-00098	SN74H183N	IC,HTTL ADDR,1-BIT FULL	TI/MML78
THRU					
UC 17					
UC 18	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 19	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UC 20	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UC 21	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 22	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 23	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UC 24	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 25	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 26	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 27	1	046-97-00161	SN74H20N	IC,HTTL GATE,NAND 4-INP	TI/MML78
UC 28	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UC 29	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UC 30	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34596 REV DATE 12/20/79 REV LTR C
LIST TITLE - PWA,FRAME SYNC CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01942 ECO 60254 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00603	32955	PWB,UNIVERSAL CIRCUIT	EMR
2	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
3	88	236-98-00058	41018-01-016-1	SOCKET,IC,DIP,16PIN,WW	MML21
4	184	236-98-00057	41014-01-014-1	SOCKET,IC,DIP,14PIN,WW	MML21
5	1	299-99-00078	32199-4	EJCTR/INSR,.062CD,POSN4	EMR
6	1	279-99-00161	32971	SPRT,PWB	EMR
7	1	140-99-00248	32972	INSUL,PWB,.20X14.75 G10	EMR
8	5	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT OPTION
9	5	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
10	AR	276-98-00159	M30015-195A	WIRE,#30 SOL,MILENE,ALLOY	W.H.GORE
11	AR	273-02-00001	NAS620C2	WASHER,#2,FLAT,0.149 DIA	PRCMT OPTION
C 1 THRU C 136	136	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
C 137	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 138	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
E 104 THRU E 167	64	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
F 2	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
RA 16	1	182-98-00011	898-1-R1K	NTWK,RES,15/1.OK 2% 1W	BECK/MML47
RA 17	1	182-98-00011	898-1-R1K	NTWK,RES,15/1.OK 2% 1W	BECK/MML47
RA 21	1	182-98-00011	898-1-R1K	NTWK,RES,15/1.OK 2% 1W	BECK/MML47
RA 24	1	182-98-00011	898-1-R1K	NTWK,RES,15/1.OK 2% 1W	BECK/MML47
TP 4	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 5	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 7	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 9	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 10	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 15	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 18	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 20	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 24	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 25	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 30	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 35	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 40	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 45	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 46	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 50	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 53	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 54	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 55	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 56 THRU TP 59	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 60	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 61 THRU TP 64	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 65	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 66	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UE 25	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 26	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 27	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UE 28	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 29	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UE 30	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 31	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 32	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
UE 33	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
UE 34	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
UF 1	1	046-97-00213	SN74148N	IC,TTL ENCDR,8-TO-3 LINE	TI/MML32
UF 2	1	046-97-00076	SN74192N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
UF 3	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UF 4	1	046-97-00089	SN7442N	IC,TTL DCDR,BCD-TO-DEC	TI/MML32
UF 5	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UF 8	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 9	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 10	1	046-97-00178	SN74174N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 13	1	046-97-00178	SN74174N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 14	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 16	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 17	1	046-97-00104	SN74153N	IC,TTL MUX, 4-INP	TI/MML32
UF 18	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
UF 19 THRU UF 32	14	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 33	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UF 34	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UG 1	1	046-97-00213	SN74148N	IC,TTL ENCDR,8-TO-3 LINE	TI/MML32
UG 2	1	046-97-00076	SN74192N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
UG 3	1	046-97-00076	SN74192N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
UG 4	1	046-97-00077	SN74193N	IC,TTL CNTR,BIN UP/DN SYN	TI/MML32
UG 8	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UG 9	1	046-97-00169	SN74184N	IC,TTL CONV,BCD-TO-BIN	TI/MML32
UG 12	1	046-97-00178	SN74174N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UG 13	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UG 16	3	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
UG 18 THRU UG 32	14	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UH 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 2	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 4	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 5	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 6	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UH 7	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 8	3	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UH 10 THRU UH 11	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UC 31	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 32	1	046-97-00086	SN7403N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 33	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UC 34	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 1	3	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
THRU					
UD 3					
UD 4	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UD 5	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UD 6	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UD 7	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UD 8	7	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
THRU					
UD 14					
UD 15	3	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UD 17					
UD 18	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 19	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 20	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UD 21	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 22	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 23	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 24	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 25	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UD 26	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 27	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UD 28	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 29	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UD 30	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 31	4	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
THRU					
UD 34					
UE 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 2	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UE 3	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 4	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 5	4	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
THRU					
UE 8					
UE 9	6	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
THRU					
UE 14					
UE 15	1	046-11-00036	SN74H74N	IC,HTTL FF,D TYPE POS	TI/MML78
UE 16	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 17	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 18	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 19	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UE 20	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 21	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 22	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 23	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 24	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 34596
LIST TITLE - PWA,FRAME SYNC
PART NO. - 205-89-01942

REV DATE 12/20/79
CHGE CONT NO. CODE IDENT
ECO 60254 06141

REV LTR C
SHT 6 OF
CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
THRU					
P2E 48					
P2E 51	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P2E 98					
REF 1	1	905-01-01548	34595	SCHEM,PWA,FRAME SYNC	EMR
REF 2	1	905-31-00002	28230	GMTRY TABLE,XY,PWB 29328	EMR
REF 3	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR

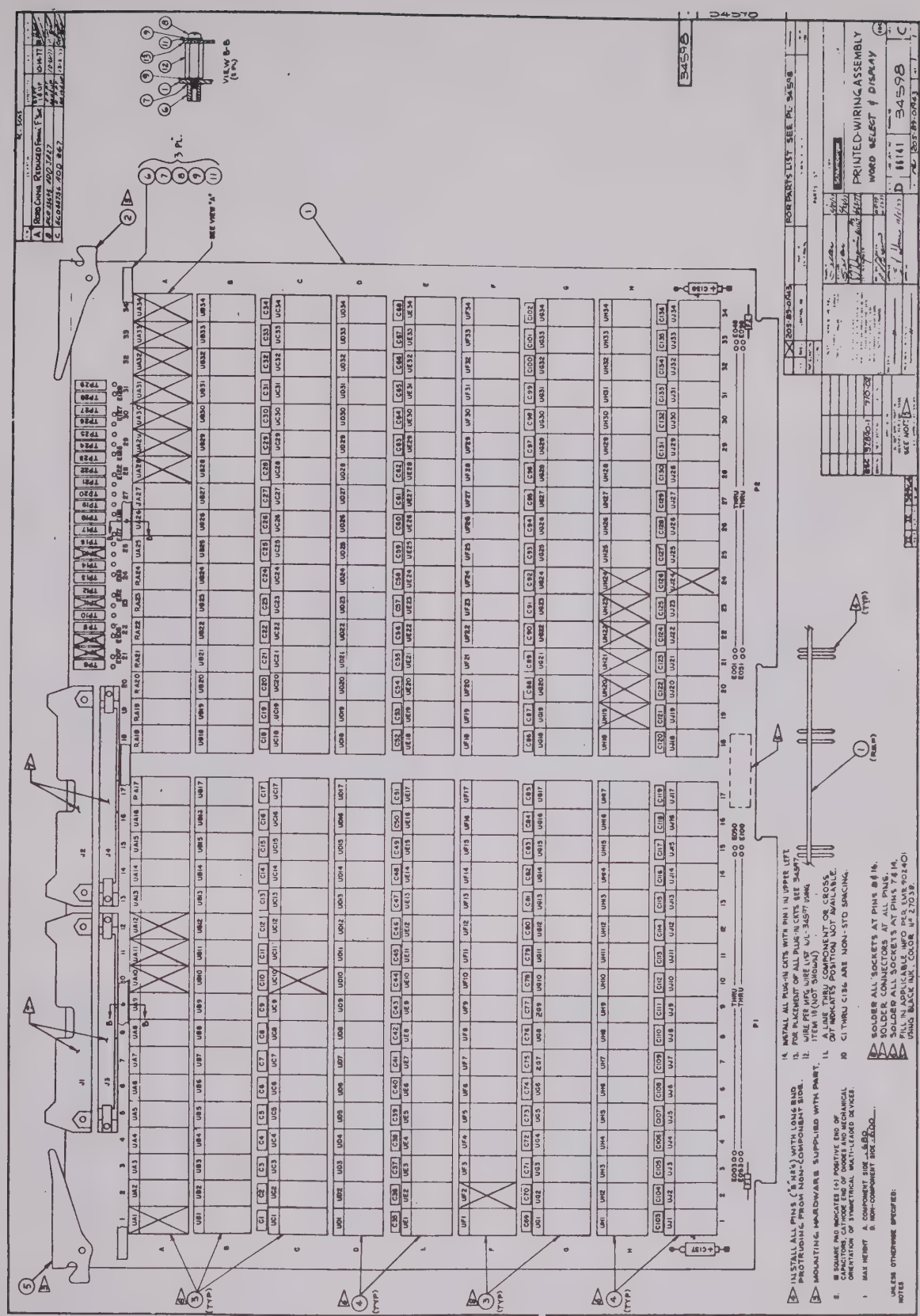
FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34596 REV DATE 12/20/79 REV LTR C
LIST TITLE - PWA,FRAME SYNC CHGE CONT NO. CODE IDENT SHT 5 OF
PART NO. - 205-89-01942 ECO 60254 06141 CKD BY

ITEM NO.	QTY RQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UH 12	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 13	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
UH 14	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UH 15	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 16	1	046-97-00159	SN7413N	IC,TTL ST GATE,NAND 4-INP	TI/MML32
UH 17	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 18	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 19	8	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UH 26	*				
UH 27	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UH 28	6	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UH 33					
UH 34	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 2	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 3	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 4	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 5	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 6	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UJ 7	3	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
THRU					
UJ 9					
UJ 10	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UJ 11	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UJ 12	1	046-97-00165	SN74S04N	IC,STTL INV	TI/MML80
UJ 13	1	046-97-00080	SN74H04N	IC,HTTL INV	TI/MML78
UJ 14	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 15	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 16	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 17	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 18	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 19	4	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UJ 22					
UJ 23	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 24	10	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UJ 33					
UJ 34	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
ZF 6	1	182-89-00013	22400-73	NTWK,2 RES,2 CAP,1 DIODE	EMR
ZG 6	1	182-89-00014	22400-74	NTWK,4 RES,2 CAPACITOR	EMR
ZG 7	1	182-89-00018	22400-78	NTWK,1RES 20K,1CAP 130PF	EMR
ZG 14	1	182-89-00015	22400-75	NTWK	EMR
ZG 15	1	182-89-00016	22400-76	NTWK,3 RES,1 XTR,1 DIODE	EMR
P1E 3	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P1E 50					
P1E 53	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P1E100					
P2E 1	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34598 REV DATE 06/08/78 REV LTR F
LIST TITLE - PWA,WD SEL & DSPL CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01943 ECO 55978 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00606	32963	PWB,UNIVERSAL CIRCUIT	EMR
2	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
3	152	236-98-00058	41018-01-016-1	SOCKET,IC,DIP,16PIN,WW	MML21
4	126	236-98-00057	41014-01-014-1	SOCKET,IC,DIP,14PIN,WW	MML21
5	1	299-99-00082	32199-8	EJCTR/INSR,.062CD,POSN8	EMR
6	1	279-99-00161	32971	SPRT,PWB	EMR
7	1	140-99-00248	32972	INSUL,PWB,.20X14.75 G10	EMR
8	5	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT OPTION
9	5	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
10	AR	276-98-00159	M30015-195A	WIRE,#30 SOL,MILENE,ALLOY	W.H.GORE
11	AR	273-02-00001	NAS620C2	WASHER,#2,FLAT,0.149 DIA	PRCMT OPTION
12	2	297-98-00149	9729-SS-0256	STDF,HEX, .562L,.187DIA	AMATOM
13	1	140-99-00260	34231	INSUL,PWA,9.68X15X.031THK	EMR
C 1 THRU C 136	136	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
C 137	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 138	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
E 106 THRU E 129	576	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
F 2	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
J 1	1	063-98-00285	3433-3005	CONN,50 PIN WW RT ANGLE	3M/MML70
J 2	1	063-98-00285	3433-3005	CONN,50 PIN WW RT ANGLE	3M/MML70
J 3	1	063-98-00284	3433-4005	CONN,50 PIN WW STRAIGHT	3M/MML70
J 4	1	063-98-00284	3433-4005	CONN,50 PIN WW STRAIGHT	3M/MML70
RA 17 THRU RA 24	8	182-98-00011	898-1-R1K	NTWK,RES,15/1.OK 2% 1W	BECK/MML47
TP 6	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 9	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 10	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 12 THRU TP 14	3	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 16 THRU TP 19	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 20	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 21 THRU TP 24	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 25	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 26 THRU TP 29	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
UA 2	1	046-97-00375	SN74LS96N	IC,LS SR,5BIT PRL OUT	TI/MML60
UA 3	1	046-97-00375	SN74LS96N	IC,LS SR,5BIT PRL OUT	TI/MML60
UA 4	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UA 5	1	046-97-00310	SN74LS155N	IC,LS DEMUX,1-TO-4 LINE	TI/MML60
UA 6	1	046-97-00310	SN74LS155N	IC,LS DEMUX,1-TO-4 LINE	TI/MML60
UA 7	1	046-97-00375	SN74LS96N	IC,LS SR,5BIT PRL OUT	TI/MML60


PRINTED-WIRING ASSEMBLY
WORD SELECT & DISPLAY
34598
FOR PARTS LIST SEE PL 34598
VIEW B-B
SEE VIEW "A"
INSTALL ALL PINS ("B" NO'S) WITH LONG END PROTRUDING FROM NON-COMPONENT SIDE.
MOUNTING HARDWARE SUPPLIED WITH PART.
SOLDER ALL SOCKETS AT PINS 8 & 16.
SOLDER CONNECTORS AT ALL PINS.
SOLDER ALL SOCKETS AT PINS 7 & 14.
FILL IN APPLICABLE INFO PER EMR 902401 USING BLACK INK, COLOR No 27038.
UNLESS OTHERWISE SPECIFIED:
NOTES

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34598 REV DATE 06/08/78 REV LTR F
LIST TITLE - PWA,WD SEL & DSPL CHGE CONT NO. CODE IDENT 06141 SHT 3 OF
PART NO. - 205-89-01943 ECO 55978 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UD 1	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UD 2	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UD 3	1	046-97-00300	SN74LS05N	IC,LS INV,OPEN-COLL 5.5V	TI/MML60
UD 4	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UD 5	1	046-97-00300	SN74LS05N	IC,LS INV,OPEN-COLL 5.5V	TI/MML60
UD 6	1	046-97-00300	SN74LS05N	IC,LS INV,OPEN-COLL 5.5V	TI/MML60
UD 7	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UD 8	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UD 9	4	046-97-00386	SN74LS38N	IC,LS BFR,NAND 2-INP	TI/MML60
THRU					
UD 12					
UD 13	3	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
THRU					
UD 15					
UD 16	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UD 17	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 18	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UD 19	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UD 20	1	046-97-00305	SN74LS32N	IC,LS GATE,OR 2-INP	TI/MML60
UD 21	1	046-97-00305	SN74LS32N	IC,LS GATE,OR 2-INP	TI/MML60
UD 22	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UD 23	1	046-97-00302	SN74LS10N	IC,LS GATE,NAND 3-INP	TI/MML60
UD 24	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UD 25	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UD 26	1	046-97-00308	SN74LS51N	IC,LS GATE,AND-OR-INV	TI/MML60
UD 27	1	046-97-00302	SN74LS10N	IC,LS GATE,NAND 3-INP	TI/MML60
UD 28	1	046-97-00303	SN74LS20N	IC,LS GATE,NAND 4-INP	TI/MML60
UD 29	1	046-97-00304	SN74LS30N	IC,LS GATE,NAND 8-INP	TI/MML60
UD 30	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UD 31	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UD 32	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UD 33	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UD 34	1	046-97-00170	SN74S10N	IC,STTL GATE,NAND 3-INP	TI/MML80
UE 1	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UE 2	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UE 3	1	046-97-00305	SN74LS32N	IC,LS GATE,OR 2-INP	TI/MML60
UE 4	3	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
THRU					
UE 6					
UE 7	1	046-97-00303	SN74LS20N	IC,LS GATE,NAND 4-INP	TI/MML60
UE 8	1	046-97-00300	SN74LS05N	IC,LS INV,OPEN-COLL 5.5V	TI/MML60
UE 9	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UE 10	1	046-97-00300	SN74LS05N	IC,LS INV,OPEN-COLL 5.5V	TI/MML60
UE 11	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UE 12	3	046-97-00300	SN74LS05N	IC,LS INV,OPEN-COLL 5.5V	TI/MML60
THRU					
UE 14					
UE 15	1	046-97-00303	SN74LS20N	IC,LS GATE,NAND 4-INP	TI/MML60
UE 16	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UE 17	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UE 18	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UE 19	4	046-97-00370	SN74LS164N	IC,LS SR,8BIT SER-PRL	TI/MML60
THRU					

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34598 REV DATE 06/08/78 REV LTR F
LIST TITLE - PWA,WD SEL & DSPL CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01943 ECO 55978 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UA 8	1	046-97-00310	SN74LS155N	IC,LS DEMUX,1-TO-4 LINE	TI/MML60
UA 9	1	046-97-00310	SN74LS155N	IC,LS DEMUX,1-TO-4 LINE	TI/MML60
UA 13	4	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
THRU					
UA 16					
UA 25	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UA 26	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 1	1	046-97-00305	SN74LS32N	IC,LS GATE,OR 2-INP	TI/MML60
UB 2	1	046-97-00316	SN74LS193N	IC,LS CNTR,BIN UP/DN	TI/MML60
UB 3	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 4	4	046-97-00315	SN74LS192N	IC,LS CNTR,DECADE UP/DN	TI/MML60
THRU					
UB 7					
UB 8	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 9	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 10	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 11	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 12	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 13	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 14	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 15	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 16	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 17	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 18	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 19	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 20	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 21	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UB 22	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UB 23	12	046-97-00290	SN74LS190BN	IC,LS CNTR,DECADE UP/DN	TI/MML60
THRU					
UB 34					
UC 1	1	046-97-00291	SN74LS283N	IC,LS ADDR,BIN 4BIT FULL	TI/MML60
UC 2	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UC 3	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UC 4	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UC 5	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UC 6	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UC 7	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UC 8	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UC 9	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UC 11	1	046-97-00307	SN74LS42N	IC,LS DCDR,BCD-TO-DEC	TI/MML60
UC 12	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UC 13	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UC 14	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UC 15	8	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
THRU					
UC 22					
UC 23	4	046-97-00368	SN74LS160N	IC,LS CNTR,DECADE 4-BIT	TI/MML60
THRU					
UC 26					
UC 27	8	046-97-00309	SN74LS85N	IC,LS COMPTR,MAGTD 4-BIT	TI/MML60
THRU					
UC 34					

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34598 REV DATE 06/08/78 REV LTR F
LIST TITLE - PWA,WD SEL & DSPL CHGE CONT NO. CODE IDENT SHT 5 OF
PART NO. - 205-89-01943 ECO 55978 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UH 2	1	046-97-00171	SN74S20N	IC,STTL GATE,NAND 4-INP	TI/MML80
UH 3	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UH 4	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UH 5	1	046-97-00303	SN74LS20N	IC,LS GATE,NAND 4-INP	TI/MML60
UH 6	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UH 7	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UH 8	1	046-97-00306	SN74LS37N	IC,LS BFR,NAND 2-INP	TI/MML60
UH 9	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UH 10	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UH 11	1	046-97-00302	SN74LS10N	IC,LS GATE,NAND 3-INP	TI/MML60
UH 12	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UH 13	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 14	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UH 15	1	046-97-00319	SN74LS107N	IC,LS FF,JK TYPE W/CLR	TI/MML60
UH 16	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UH 17	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UH 18	1	046-97-00308	SN74LS51N	IC,LS GATE,AND-OR-INV	TI/MML60
UH 25	1	046-97-00280	SN74LS86N	IC,LS GATE,EXCL-OR 2-INP	TI/MML60
UH 26	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UH 27	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UH 28	7	046-97-00387	SN74LS125N	IC,LS BFR,3-STATE BUS	TI/MML60
THRU					
UH 34					
UJ 1	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
UJ 2	1	046-97-00165	SN74S04N	IC,STTL INV	TI/MML80
UJ 3	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UJ 4	1	046-97-00387	SN74LS125N	IC,LS BFR,3-STATE BUS	TI/MML60
UJ 5	1	046-97-00306	SN74LS37N	IC,LS BFR,NAND 2-INP	TI/MML60
UJ 6	1	046-97-00306	SN74LS37N	IC,LS BFR,NAND 2-INP	TI/MML60
UJ 7	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UJ 8	1	046-97-00306	SN74LS37N	IC,LS BFR,NAND 2-INP	TI/MML60
UJ 9	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UJ 10	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UJ 11	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UJ 12	3	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
THRU					
UJ 14					
UJ 15	3	046-97-00302	SN74LS10N	IC,LS GATE,NAND 3-INP	TI/MML60
THRU					
UJ 17					
UJ 18	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UJ 19	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 20	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UJ 21	1	046-97-00299	SN74LS04N	IC,LS INV	TI/MML60
UJ 22	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UJ 23	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UJ 25	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UJ 26	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UJ 27	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UJ 28	7	046-97-00387	SN74LS125N	IC,LS BFR,3-STATE BUS	TI/MML60
THRU					
UJ 34					
ZG 9	1	182-89-00137	22400-116	NTWK,SPECIAL	EMR

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UE 22					
UE 23	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UE 24	4	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
THRU					
UE 27					
UE 28	1	046-97-00296	SN74LS00N	IC,LS GATE,NAND 2-INP	TI/MML60
UE 29	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UE 30	1	046-97-00279	SN74LS74N	IC,LS FF,D TYPE POS EDGE	TI/MML60
UE 31	1	046-97-00297	SN74LS02N	IC,LS GATE,NOR 2-INP	TI/MML60
UE 32	1	046-97-00304	SN74LS30N	IC,LS GATE,NAND 8-INP	TI/MML60
UE 33	1	046-97-00302	SN74LS10N	IC,LS GATE,NAND 3-INP	TI/MML60
UE 34	1	046-97-00292	SN74S08N	IC,STTL GATE,AND 2-INP	TI/MML80
UF 1	1	046-97-00301	SN74LS08N	IC,LS GATE,AND 2-INP	TI/MML60
UF 3	4	046-97-00368	SN74LS160N	IC,LS CNTR,DECADE 4-BIT	TI/MML60
THRU					
UF 6					
UF 7	4	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
THRU					
UF 10					
UF 11	1	046-97-00288	SN74LS174N	IC,LS FF,D TYPE W/CLR	TI/MML60
UF 12	1	046-97-00288	SN74LS174N	IC,LS FF,D TYPE W/CLR	TI/MML60
UF 13	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UF 14	4	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
THRU					
UF 17					
UF 18	8	046-97-00175	SN74185AN	IC,TTL CONV,BIN-TO-BCD	TI/MML32
THRU					
UF 25					
UF 26	1	046-97-00309	SN74LS85N	IC,LS COMPTR,MAGTD 4-BIT	TI/MML60
UF 27	1	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
UF 28	7	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
THRU					
UF 34					
UG 1	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UG 2	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UG 3	4	046-97-00309	SN74LS85N	IC,LS COMPTR,MAGTD 4-BIT	TI/MML60
THRU					
UG 6					
UG 10	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UG 11	1	046-97-00288	SN74LS174N	IC,LS FF,D TYPE W/CLR	TI/MML60
UG 12	1	046-97-00288	SN74LS174N	IC,LS FF,D TYPE W/CLR	TI/MML60
UG 13	1	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
UG 14	4	046-97-00285	SN74LS157N	IC,LS MUX, 2-INP	TI/MML60
THRU					
UG 17					
UG 18	8	046-97-00175	SN74185AN	IC,TTL CONV,BIN-TO-BCD	TI/MML32
THRU					
UG 25					
UG 26	1	046-97-00369	SN74LS161N	IC,LS CNTR,BIN 4-BIT SYN	TI/MML60
UG 27	8	046-97-00289	SN74LS175N	IC,LS FF,D TYPE W/CLR	TI/MML60
THRU					
UG 34					
UH 1	1	046-97-00387	SN74LS125N	IC,LS BFR,3-STATE BUS	TI/MML60

HOLE/COMPONENT CHART

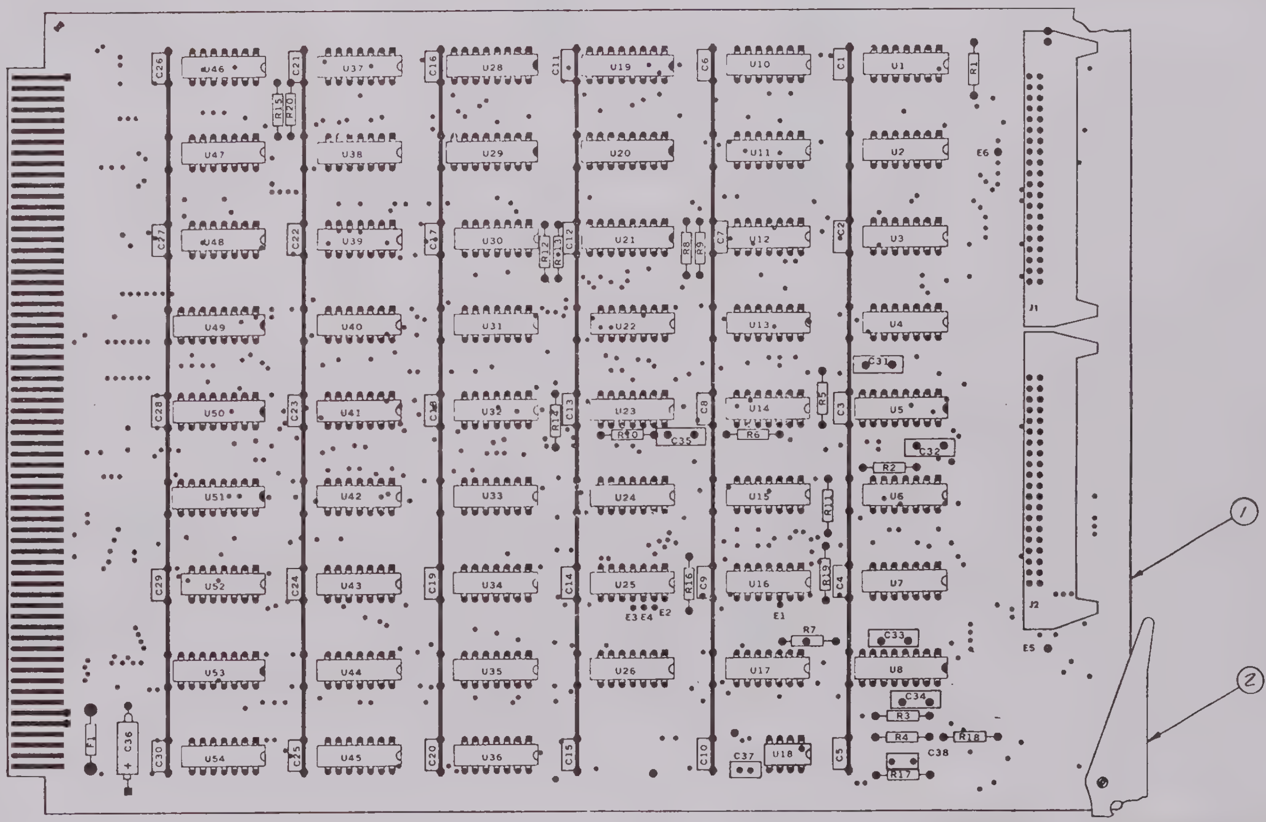
DESCRIPTION/UNUSED NUMBER

ARTWORK REVISION INDEX

SHEET NO							
REVISION							

REVISIONS

LTR	DESCRIPTION	DATE	APPROVAL
E	ECO 55949 (INTERIM) REV CKT	1-30-78	
F	ECO 55936 REV CKT & ADD R20		



-1	205-89-01951	FOR PARTS LIST, SEE PL-34311-1	—
BSC	205-89-01939	FOR PARTS LIST, SEE PL-34311	—
CONTROL NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	ITEM OR SYMBOL

PARTS LIST

3. ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.

2. DESIGN REF. HEIGHT: .656

1. MAX ASSY HEIGHT: A. COMPONENT SIDE: .500
   B. NONCOMPONENT SIDE: .093

NOTES
UNLESS OTHERWISE SPECIFIED:

DASH NO	NEXT ASSY	USED ON
-1	34550	708
BSC	32890-1	710-02

DRAWN BY SALTER 6-8-77
CHECKED SALTER 6-8-77
D. DAGENAIS 6-10-77
R.F.B. 6-10-77
APPROVED F. V. STONE 10-5-77

Schlumberger

PWA
DATA ENTRY

SIZE D | CODE IDENT NO 06141 | DRAWING NO 34311 | REV F

205-89-01939

16-43

7-40

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 34598 REV DATE 06/08/78 REV LTR F

LIST TITLE - PWA,WD SEL & DSPL CHGE CONT NO. CODE IDENT 06141 SHT 6 OF

PART NO. - 205-89-01943 ECO 55978 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
P1E 3 THRU P1E 50	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 53 THRU P1E100	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 1 THRU P2E 48	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 51 THRU P2E 98	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR
REF 2	1	905-31-00023	33109	GMTRY TABLE,XY,PWB 32963	EMR
REF 3	1	905-01-01549	34597	SCHEM,PWA,WD SEL & DSPL	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA REV LTR B
PARTS LIST - 34311 REV DATE 09/21/78 SHT 2 OF
LIST TITLE - PWA,DATA ENTRY CHGE CONT NO. CODE IDENT CKD BY
PART NO. - 205-89-01939 ECO 56991 06141

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
U 22	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
U 23	1	046-97-00193	SN7414N	IC,TTL ST INV	TI/MML32
U 24	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
U 25	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
U 26	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 28	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
U 29	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
U 30	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 31	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
U 32	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
U 33	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
U 34	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 35	8	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
U 42					
U 43	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 44	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 45	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 46	3	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
THRU					
U 48					
U 49	3	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
THRU					
U 51					
U 52	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 53	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
U 54	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
W 1	6	021-99-00058	30080-15	BUSBAR,LAM,.50H, 9 GROUPS	EMR
THRU					
W 6					
REF 1	1	905-01-01545	34309	SCHEM,PWA,DATA ENTRY	EMR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR

FIRST MODEL USAGE 0708-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 34311 REV DATE 09/21/78 REV LTR B

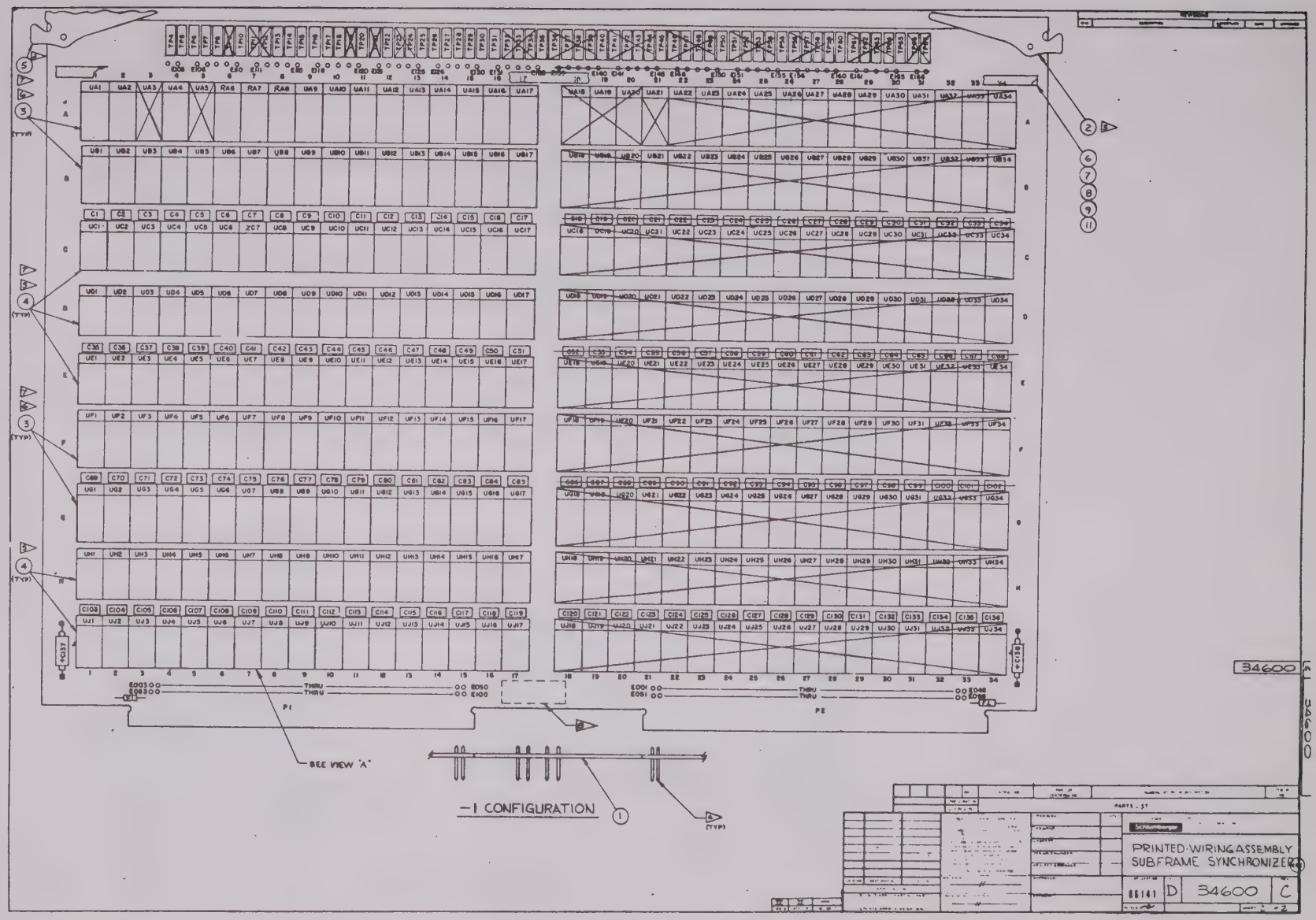
LIST TITLE - PWA,DATA ENTRY CHGE CONT NO. CODE IDENT 06141 SHT 1 OF

PART NO. - 205-89-01939 ECO 56991 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00610	34310	PWB,DATA ENTRY	EMR
2	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
3	AR	276-02-00049	MIL-W-16878/4*SIL CTD*	WIRE,#26,SOL, WHT, 600V	PRCMT OPTION
C 1	30	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
THRU					
C 30					
C 31	1	301-13-68002	8131-050-651-684M/MML	CAP,CR , 50V .680 UF 20%	MML 48
C 32	1	304-20-13009	600	CAP. 130PF 1% 500V	EMR
C 33	1	304-08-03609	600	CAP. 36PF .5PF 500V	EMR
C 34	1	304-08-03609	600	CAP. 36PF .5PF 500V	EMR
C 35	1	304-20-43009	600	CAP. 430PF 1% 500V	EMR
C 36	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 37	1	301-03-10001	8121-050-651-103M/MML	CAP,CR , 50V .010 UF 20%	MML 48
C 38	1	301-13-10003	8131-050-651-105M/MML	CAP,CR , 50V 1.00UF 20%	MML 48
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
R 1	1	616-02-51000	RC07GF512J	RES,5.1K 5% 1/4W	ALLEN BRAD
R 2	1	616-02-20001	RC07GF203J	RES,20K 5% 1/4W	ALLEN BRAD
R 3	1	616-02-10001	RC07GF103J	RES,10K 5% 1/4W	ALLEN BRAD
R 4	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 5	1	616-02-27001	RC07GF273J	RES,27K 5% 1/4W	ALLEN BRAD
R 6	1	616-02-51009	RC07GF511J	RES,510 OHM 5% 1/4W	ALLEN BRAD
R 7	1	616-02-10001	RC07GF103J	RES,10K 5% 1/4W	ALLEN BRAD
R 8	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 9	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 10	1	616-02-47009	RC07GF471J	RES,470 OHM 5% 1/4W	ALLEN BRAD
R 11	5	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
THRU					
R 15					
R 16	1	616-02-47000	RC07GF472J	RES,4.7K 5% 1/4W	ALLEN BRAD
R 17	1	616-02-33003	RC07GF335J	RES,3.3 MEG 5% 1/4W	ALLEN BRAD
R 18	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 19	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 20	1	616-02-10001	RC07GF103J	RES,10K 5% 1/4W	ALLEN BRAD
U 1	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 2	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
U 3	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 4	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
U 5	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
U 6	1	046-97-00193	SN7414N	IC,TTL ST INV	TI/MML32
U 7	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 8	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
U 10	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
U 11	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
U 12	1	046-97-00071	SN7493N	IC,TTL CNTR,BIN 4-BIT	TI/MML32
U 13	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
U 14	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
U 15	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
U 16	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 17	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 18	1	046-97-00220	NE555V	IC,LIN TIMER	SIG/MML40
U 19	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
U 20	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML32
U 21	1	046-97-00169	SN74184N	IC,TTL CONV,BCD-TO-BIN	TI/MML32

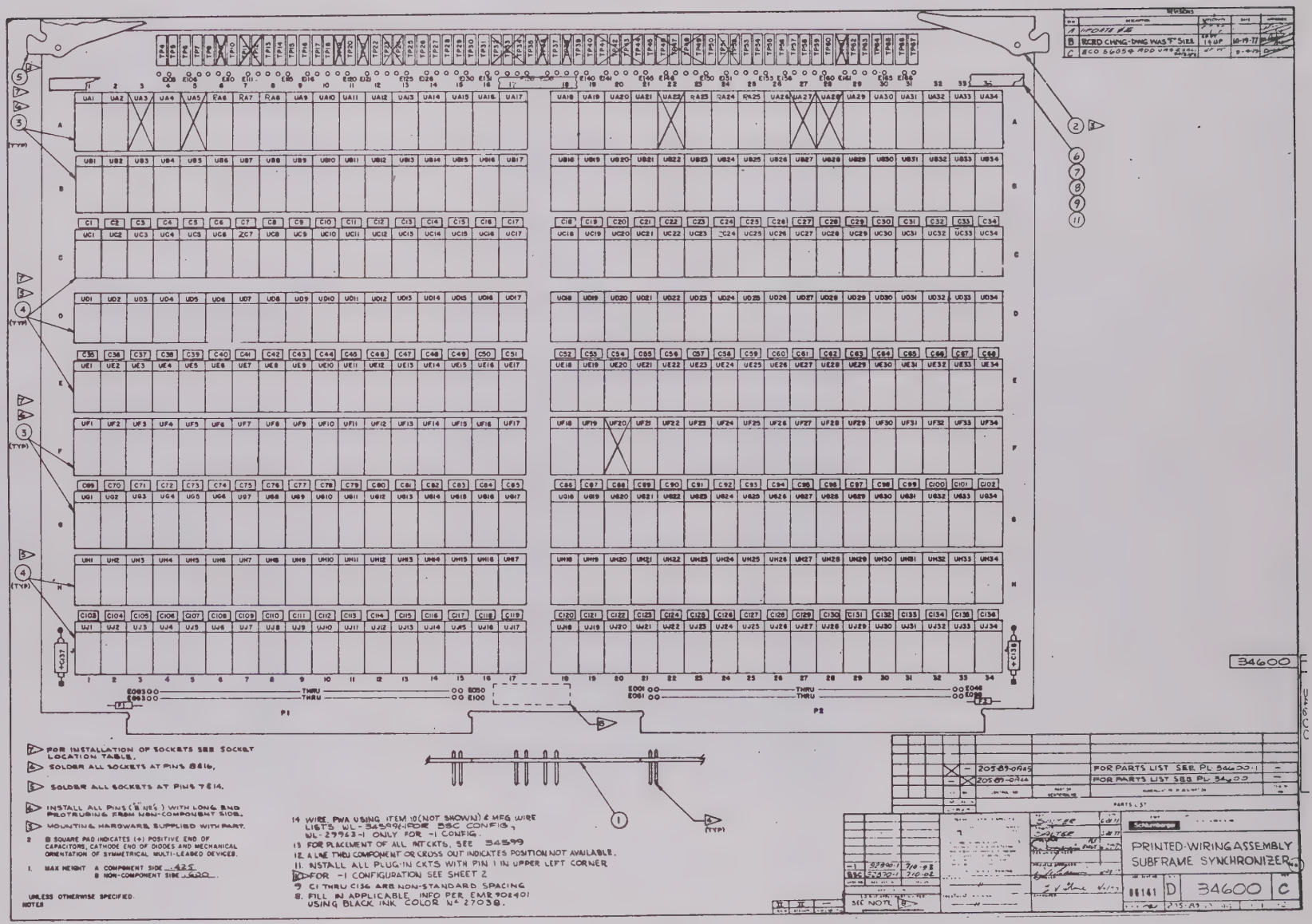
DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34600-1 REV DATE 08/30/79 REV LTR E
LIST TITLE - PWA,SUBFRAME SYNC 1 CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01945 ECO 59048 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00604	32957	PWB,UNIVERSAL CIRCUIT	EMR
2	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
3	66	236-98-00058	41018-01-016-1	SOCKET,IC,DIP,16PIN,WW	MML21
4	85	236-98-00057	41014-01-014-1	SOCKET,IC,DIP,14PIN,WW	MML21
5	1	299-99-00079	32199-5	EJCTR/INSR,.062CD,POSN5	EMR
6	1	279-99-00161	32971	SPRT,PWB	EMR
7	1	140-99-00248	32972	INSUL,PWB,.20X14.75 G10	EMR
8	5	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT OPTION
9	5	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
10	AR	276-98-00159	M30015-195A	WIRE,#30 SOL,MILENE,ALLOY	W.H.GORE
11	AR	273-02-00001	NAS620C2	WASHER,#2,FLAT,0.149 DIA	PRCMT OPTION
C 1	17	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 17					
C 35	17	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 51					
C 69	17	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 85					
C 103	17	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 119					
C 137	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 138	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
E 104	32	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
E 135					
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
F 2	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
RA 6	3	182-98-00011	898-1-R1K	NTWK,RES,15/1.0K 2% 1W	BECK/MML47
THRU					
RA 8					
TP 4	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 5	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 6	3	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
THRU					
TP 8					
TP 10	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 13	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 14	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 15	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 16	3	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
THRU					
TP 18					
TP 20	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 22	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 25	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 26	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
THRU					
TP 29					
TP 30	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 31	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16


-1 CONFIGURATION
SEE VIEW "A"
PRINTED-WIRING ASSEMBLY
SUBFRAME SYNCHRONIZER
34600
D
C

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UD 12	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 13	5	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UD 17					
UE 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 2	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 3	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 4	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 5	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 6	1	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
UE 7	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 8	4	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
THRU					
UE 11					
UE 12	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UE 13	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 14	4	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UE 17					
UF 1	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 2	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 3	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
UF 4	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UF 5	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 6	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 7	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 8	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 9	5	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
THRU					
UF 13					
UF 14	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 15	1	046-97-00103	SN74151N	IC,TTL MUX, 8-INP	TI/MML32
UF 16	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UF 17	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UG 1	1	046-97-00095	SN74155N	IC,TTL DEMUX,1-TO-4 LINE	TI/MML32
UG 2	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UG 3	3	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
THRU					
UG 5					
UG 6	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UG 7	7	046-97-00177	SN74161N	IC,TTL CNTR,BIN 4-BIT SYN	TI/MML32
THRU					
UG 13					
UG 14	4	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
THRU					
UG 17					
UH 1	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 2	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UH 3	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 4	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 5	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UH 6	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 7	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
TP 35	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 40	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 45	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 50	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 55	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 60	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 65	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
UA 1	1	046-97-00073	SN7496N	IC,TTL SR,5BIT PRL OUT	TI/MML32
UA 2	1	046-97-00073	SN7496N	IC,TTL SR,5BIT PRL OUT	TI/MML32
UA 4	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UA 9	3	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
THRU					
UA 11					
UA 12	1	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
UA 13	4	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UA 16					
UA 17	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
UB 1	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 2	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 3	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 4	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 5	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 6	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 7	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 8	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 9	1	046-97-00167	SN74S112N	IC,STTL FF,J-K TYPE W/CLR	TI/MML80
UB 10	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UB 11	7	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UB 17					
UC 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 2	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 4	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 5	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UC 6	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 8	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UC 9	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 10	8	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UC 17					
UD 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 2	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 4	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UD 5	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 6	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UD 7	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 8	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 9	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 10	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 11	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32


PRINTED-WIRING ASSEMBLY
SUBFRAME SYNCHRONIZER
34600
D
C
P1
P2
FOR INSTALLATION OF SOCKETS SEE SOCKET LOCATION TABLE.
SOLDER ALL SOCKETS AT PINS 8&16.
SOLDER ALL SOCKETS AT PINS 7&14.
INSTALL ALL PINS (8 NOS) WITH LONG END PROTRUDING FROM NON-COMPONENT SIDE.
MOUNTING HARDWARE SUPPLIED WITH PART.
2 SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.
1. MAX HEIGHT A COMPONENT SIDE .425
B NON-COMPONENT SIDE .600
UNLESS OTHERWISE SPECIFIED.
NOTES
14 WIRE, PWA USING ITEM 10 (NOT SHOWN) & MFG WIRE LISTS WL-34599-1 FOR 55C CONFIG, WL-27963-1 ONLY FOR -1 CONFIG.
13 FOR PLACEMENT OF ALL INT CKTS, SEE 34599
12. A LINE THRU COMPONENT OR CROSS OUT INDICATES POSITION NOT AVAILABLE.
11. INSTALL ALL PLUG-IN CKTS WITH PIN 1 IN UPPER LEFT CORNER
FOR -1 CONFIGURATION SEE SHEET 2
9 C1 THRU C136 ARE NON-STANDARD SPACING.
8. FILL IN APPLICABLE INFO PER EMR 902401 USING BLACK INK COLOR No 27038.
FOR PARTS LIST SEE PL 34600-1
FOR PARTS LIST SEE PL 34600

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UH 8	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 9	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 10	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 11	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 12	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 13	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 14	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 15	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 16	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 17	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UJ 1	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 2	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 4	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 5	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UJ 6	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 7	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 8	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 9	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 10	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 11	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 12	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 13	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UJ 14	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 15	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 16	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UJ 17	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
ZC 7	1	182-89-00017	22400-77	NTWK,1RES,1CAPACITOR	EMR
P1E 1 THRU P1E 50	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 53 THRU P1E100	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 1 THRU P2E 48	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 51 THRU P2E 98	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR
REF 2	1	905-31-00002	28230	GMTRY TABLE,XY,PWB 29328	EMR
REF 3	1	905-01-01550	34599	SCHEM,PWA,SUBFRAME SYNC	EMR

FIRST MODEL USAGE 0710-02

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
TP 53	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 54	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 55	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 56	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
THRU					
TP 59					
TP 60	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 62	3	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
THRU					
TP 64					
TP 65	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 66	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 67	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
UA 1	1	046-97-00073	SN7496N	IC,TTL SR,5BIT PRL OUT	TI/MML32
UA 2	1	046-97-00073	SN7496N	IC,TTL SR,5BIT PRL OUT	TI/MML32
UA 4	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UA 9	3	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
THRU					
UA 11					
UA 12	1	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
UA 13	4	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UA 16					
UA 17	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
UA 18	1	046-97-00073	SN7496N	IC,TTL SR,5BIT PRL OUT	TI/MML32
UA 19	1	046-97-00073	SN7496N	IC,TTL SR,5BIT PRL OUT	TI/MML32
UA 20	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UA 21	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UA 26	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UA 29	1	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
UA 30	4	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UA 33					
UA 34	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
UB 1	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 2	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 3	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 4	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 5	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 6	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 7	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 8	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 9	1	046-97-00167	SN74S112N	IC,STTL FF,J-K TYPE W/CLR	TI/MML80
UB 10	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UB 11	7	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UB 17					
UB 18	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 19	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 20	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 21	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 22	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 23	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34600 REV DATE 08/30/79 REV LTR E
LIST TITLE - PWA,SUBFRAME SYNC 2 CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01944 ECO 59048 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00604	32957	PWB,UNIVERSAL CIRCUIT	EMR
2	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
3	130	236-98-00058	41018-01-016-1	SOCKET,IC,DIP,16PIN,WW	MML21
4	170	236-98-00057	41014-01-014-1	SOCKET,IC,DIP,14PIN,WW	MML21
5	1	299-99-00079	32199-5	EJCTR/INSR,.062CD,POSN5	EMR
6	1	279-99-00161	32971	SPRT,PWB	EMR
7	1	140-99-00248	32972	INSUL,PWB,.20X14.75 G10	EMR
8	5	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT OPTION
9	5	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
10	AR	276-98-00159	M30015-195A	WIRE,#30 SOL,MILENE,ALLOY	W.H.GORE
11	AR	273-02-00001	NAS620C2	WASHER,#2,FLAT,0.149 DIA	PRCMT OPTION
C 1 THRU C 136	136	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
C 137	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 138	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
E 104 THRU E 167	64	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
F 2	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
RA 6 THRU RA 8	3	182-98-00011	898-1-R1K	NTWK,RES,15/1.0K 2% 1W	BECK/MML47
RA 23 THRU RA 25	3	182-98-00011	898-1-R1K	NTWK,RES,15/1.0K 2% 1W	BECK/MML47
TP 4	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 5	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 6 THRU TP 8	3	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 10	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 13	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 14	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 15	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 16 THRU TP 18	3	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 20	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 22	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 25	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 26 THRU TP 29	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 30	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 31	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 35	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 37	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 39	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 40	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 45	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 50	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UD 27	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 28	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UD 29	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 30	5	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UD 34					
UE 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 2	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 3	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 4	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 5	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 6	1	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
UE 7	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 8	4	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
THRU					
UE 11					
UE 12	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UE 13	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 14	4	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UE 17					
UE 18	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 19	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 20	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 21	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UE 22	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 23	1	046-97-00146	SN74164N	IC,TTL SR,8BIT SER-PRL	TI/MML32
UE 24	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 25	4	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
THRU					
UE 28					
UE 29	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UE 30	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 31	4	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UE 34					
UF 1	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 2	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 3	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
UF 4	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UF 5	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 6	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 7	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 8	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 9	5	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
THRU					
UF 13					
UF 14	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 15	1	046-97-00103	SN74151N	IC,TTL MUX, 8-INP	TI/MML32
UF 16	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UF 17	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UF 18	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 19	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34600 REV DATE 08/30/79 REV LTR E
LIST TITLE - PWA,SUBFRAME SYNC 2 CHGE CONT NO. CODE IDENT SHT 3 OF
PART NO. - 205-89-01944 ECO 59048 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UB 24	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UB 25	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UB 26	1	046-97-00167	SN74S112N	IC,STTL FF,J-K TYPE W/CLR	TI/MML80
UB 27	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UB 28	7	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UB 34					
UC 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 2	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 4	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 5	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UC 6	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 8	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UC 9	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 10	8	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UC 17					
UC 18	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UC 19	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 20	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 21	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 22	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UC 23	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 25	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UC 26	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 27	8	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UC 34					
UD 1	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 2	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 4	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UD 5	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 6	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UD 7	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 8	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 9	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 10	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 11	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UD 12	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 13	5	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UD 17					
UD 18	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 19	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 20	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 21	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UD 22	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 23	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UD 24	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 25	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 26	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UH 18	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 19	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UH 20	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 21	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 22	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UH 23	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 24	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UH 25	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 26	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 27	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 28	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 29	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 30	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH B1	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 32	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 33	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 34	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UJ 1	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 2	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 4	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 5	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UJ 6	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 7	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 8	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 9	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 10	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 11	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 12	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 13	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UJ 14	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 15	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 16	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UJ 17	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UJ 18	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 19	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 20	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 21	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 22	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UJ 23	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 24	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 25	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 26	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 27	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 28	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 29	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 30	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UJ 31	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 32	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 33	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UJ 34	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
ZC 7	1	182-89-00017	22400-77	NTWK,1RES,1CAPACITOR	EMR
ZC 24	1	182-89-00017	22400-77	NTWK,1RES,1CAPACITOR	EMR

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UF 21	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
UF 22	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 23	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 24	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UF 25	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 26	5	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
THRU					
UF 30					
UF 31	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 32	1	046-97-00103	SN74151N	IC,TTL MUX, 8-INP	TI/MML32
UF 33	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UF 34	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UG 1	1	046-97-00095	SN74155N	IC,TTL DEMUX,1-TO-4 LINE	TI/MML32
UG 2	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UG 3	3	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
THRU					
UG 5					
UG 6	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UG 7	7	046-97-00177	SN74161N	IC,TTL CNTR,BIN 4-BIT SYN	TI/MML32
THRU					
UG 13					
UG 14	4	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
THRU					
UG 17					
UG 18	1	046-97-00095	SN74155N	IC,TTL DEMUX,1-TO-4 LINE	TI/MML32
UG 19	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UG 20	3	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
THRU					
UG 22					
UG 23	1	046-97-00145	SN7485N	IC,TTL COMPTR,MAGTD 4-BIT	TI/MML32
UG 24	7	046-97-00177	SN74161N	IC,TTL CNTR,BIN 4-BIT SYN	TI/MML32
THRU					
UG 30					
UG 31	4	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
THRU					
UG 34					
UH 1	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 2	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UH 3	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 4	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 5	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
UH 6	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 7	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UH 8	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 9	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 10	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 11	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 12	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 13	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 14	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UH 15	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 16	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 17	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 34592 REV DATE 12/20/79 REV LTR A

LIST TITLE - PWA,SIMULATOR 1 CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 205-89-01940 ECO 60261 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00609	34591	PWB,SIMULATOR 1	EMR
2	1	273-98-00047	5600-40-16	WASHER,FIBRE .016THK	SEASTROM
3	5	189-99-00001	800-1	PAD,XSTR TO-5,9 OR 11,4 P	EMR
5	3	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*	EMR
6	2	189-98-00004	100-000-NY	PAD,XSTR 4 PIN*USE OPTL*	DEL BL INN
7	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
8	1	299-99-00080	32199-6	EJCTR/INSR,.062CD,POSN6	EMR
9	1	276-98-00195	J0.250X0.250T22	WIRE,JUMPER,#22 SOLID .25	MML42
10	1	276-98-00196	J0.500X0.250T22	WIRE,JUMPER,#22 SOLID .5L	MML42
11	AR	276-02-00048	MIL-W-16878/4*SIL CTD*	WIRE,#24,SOL, WHT, 600V	PRCMT OPTION
12	1	232-89-00024	30337	SHIELD,ASSY,SIM #1	EMR
13	4	239-98-00022	FW106	SPCR,RND,.2500D X .125L	MML75
14	AR	229-02-00073	MS51957-13	SCREW,4-40X1/4 PAN HD	PRCMT CPTION
15	AR	287-02-00002	MS35649-244	NUT,HEX, 4-40	PRCMT CPTION
16	AR	273-02-00025	MS35333-70	WASHER,#4,INT TOOTH	PRCMT OPTION
17	AR	276-99-00006	619-18	WIRE,#18,BUSS,SOLID	EMR
18	AR	268-02-00026	MIL-I-22129	TUBING,#18,EXTR TEF,CLEAR	PRCMT OPTION
19	AR	060-11-00019	0151	CMPD,EPOXY,GENL PURPOSE	HYSOL
20	1	279-99-00161	32971	SPRT,PWB	EMR
21	1	140-99-00248	32972	INSUL,PWB,.20X14.75 G10	EMR
22	5	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT CPTION
23	5	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
24	AR	273-02-00001	NAS620C2	WASHER,#2,FLAT,0.149 DIA	PRCMT OPTION
C 1	1	304-20-30009	600	CAP. 300PF 1% 500V	EMR
C 2	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 3	1	304-08-03009	600	CAP. 30PF .5PF 500V	EMR
C 4	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 5	1	301-03-10001	8121-050-651-103M/MML	CAP,CR , 50V .010 UF 20%	MML 48
C 6	1	301-03-10001	8121-050-651-103M/MML	CAP,CR , 50V .010 UF 20%	MML 48
C 7	1	304-08-02409	600	CAP.,24PF .5PF 500V	EMR
C 8	1	304-41-57009	600	CAP. 570PF 1% 300V	EMR
C 9	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 10	1	301-13-22002	8131-050-651-224M/MML	CAP,CR , 50V .220 UF 20%	MML 48
C 11	1	337-13-15004	601	CAP., 15MF 10% 20V	EMR
C 12	1	338-14-22004	601	CAP., 22MF 10% 35V	EMR
C 13	1	304-62-91009	600	CAP.,910PF 1% 100V	EMR
C 14	1	304-62-91009	600	CAP.,910PF 1% 100V	EMR
C 15	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 16	1	304-62-10000	600	CAP. 1000PF 1% 100V	EMR
C 17	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 18	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 19	1	304-08-03009	600	CAP. 30PF .5PF 500V	EMR
C 20	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 21	1	301-23-22003	8141-050-651-225M/MML	CAP,CR , 50V 2.2 UF 20%	MML 48
C 22	1	301-13-22002	8131-050-651-224M/MML	CAP,CR , 50V .220 UF 20%	MML 48
C 23	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 24	1	339-13-10005	601	CAP, 100MF 10% 20V D CASE	EMR
C 25	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 26	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 27	1	336-12-33003	601	CAP., 3.3MF 10% 15V	EMR
C 28	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 29	1	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
C 30	1	304-20-10009	600	CAP. 100PF 1% 500V	EMR

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA REV LTR E
PARTS LIST - 34600 REV DATE 08/30/79 SHT 7 OF
LIST TITLE - PWA,SUBFRAME SYNC 2 CHGE CONT NO. CODE IDENT CKD BY
PART NO. - 205-89-01944 ECO 59048 06141

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
P1E 3 THRU P1E 50	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 53 THRU P1E100	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 1 THRU P2E 48	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P2E 51 THRU P2E 98	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
REF 1	1	905-01-01550	34599	SCHEM,PWA,SUBFRAME SYNC	EMR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR
REF 3	1	905-31-00002	28230	GMTRY TABLE,XY,PWB 29328	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34592 REV DATE 12/20/79 REV LTR A
LIST TITLE - PWA,SIMULATOR 1 CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01940 ECO 60261 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
C 31	4	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
THRU					
C 34					
C 35	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR
C 36	1	301-03-10001	8121-050-651-103M/MML	CAP,CR , 50V .010 UF 20%	MML 48
C 37	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR
C 38	3	301-03-10001	8121-050-651-103M/MML	CAP,CR , 50V .010 UF 20%	MML 48
THRU					
C 40					
C 41	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR
C 42	1	301-03-10001	8121-050-651-103M/MML	CAP,CR , 50V .010 UF 20%	MML 48
C 43	1	337-14-68003	601	CAP. 6.8MF 10% 35V	EMR
C 44	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 45	1	320-98-00004	538-011,7-25PF,B	CAP, TRMR, 7-25PF 350V	MML 23
C 46	24	301-13-10002	8131-050-651-104M/MML	CAP,CR , 50V .100 UF 20%	MML 48
THRU					
C 69					
C 70	1	303-61-13009	600	CAP., 130PF 2% 100V	EMR
C 71	1	339-13-10005	601	CAP, 100MF 10% 20V D CASE	EMR
C 72	1	394-03-10006	T140D108M006AS	CAP., 1000MF 20% 6V	KEMET/MML22
C 73	1	339-13-10005	601	CAP, 100MF 10% 20V D CASE	EMR
CR 1	5	088-10-41480	1N4148	DIODE,SW,75V/5UA,4NS/10MA	JEDEC
THRU					
CR 5					
CR 6	1	088-10-09381	1N938/1N938A/1N938B	DIODE,REF,9V/7.5MA,.001 %	JEDEC
CR 7	1	088-10-41480	1N4148	DIODE,SW,75V/5UA,4NS/10MA	JEDEC
CR 8	1	088-10-41480	1N4148	DIODE,SW,75V/5UA,4NS/10MA	JEDEC
F 1	1	120-98-00047	275004	FUSE,SUBMIN,4A @ 125V	LITTELFUSE
F 2	1	120-98-00047	275004	FUSE,SUBMIN,4A @ 125V	LITTELFUSE
Q 1	1	263-10-51790	2N5179	XSTR,NPN VHF CONVERTERS	JEDEC
Q 2	1	263-10-51790	2N5179	XSTR,NPN VHF CONVERTERS	JEDEC
Q 3	1	263-10-22700	2N2270	XSTR,PWR NPN, 5W, 1A	JEDEC
Q 4	1	263-10-40370	2N4037	XSTR,PWR PNP, 7W, 1A	JEDEC
Q 5	1	263-10-39470	2N3947	XSTR,NPN 40V SW-AMPL,HFE	JEDEC
Q 6	1	263-10-39470	2N3947	XSTR,NPN 40V SW-AMPL,HFE	JEDEC
Q 7	1	263-97-00093	2N3251/2N3251A	XSTR,PNP,SWITCH/AMPL,50V	MML 4
R 1	1	608-09-30100	624	RES. 3.01K 1% 1/10W	EMR
R 2	1	608-09-75009	624	RES, 750.0 OHM 1% 1/10W	EMR
R 3	1	608-09-49909	624	RES, 499.0 OHM 1% 1/10W	EMR
R 4	1	201-98-00091	62PR1K	POT,TRMR, 1.0 K 10% .5W	BECK/MML27
R 5	1	608-09-16500	624	RES. 1.65K OHM 1% 1/10W	EMR
R 6	1	608-09-41209	624	RES, 412.0 OHM 1% 1/10W	EMR
R 7	1	608-09-21500	624	RES. 2.15K 1% 1/10W	EMR
R 8	1	608-09-27400	624	RES. 2.74K 1% 1/10W	EMR
R 9	1	608-09-23200	624	RES, 2.32K 1% 1/10W	EMR
R 10	1	608-09-24300	624	RES, 2.43K 1% 1/10W	EMR
R 11	1	608-09-25500	624	RES, 2.55K 1% 1/10W	EMR
R 12	1	608-09-25500	624	RES, 2.55K 1% 1/10W	EMR
R 13	1	608-09-28700	624	RES, 2.87K 1% 1/10W	EMR
R 14	1	608-09-20500	624	RES. 2.05K 1% 1/10W	EMR
R 15	1	608-09-93109	624	RES, 931.0 OHM 1% 1/10W	EMR
R 16	1	608-09-30100	624	RES. 3.01K 1% 1/10W	EMR
R 17	1	616-02-30009	RC07GF301J	RES. 300 OHM 5% 1/4W	ALLEN BRAD

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34592 REV DATE 12/20/79 REV LTR A
LIST TITLE - PWA,SIMULATOR 1 CHGE CONT NO. CODE IDENT SHT 4 OF
PART NO. - 205-89-01940 ECO 60261 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
R 71	1	608-09-30101	624	RES, 30.1K 1% 1/10W	EMR
R 72	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 73	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 74	1	608-09-30100	624	RES. 3.01K 1% 1/10W	EMR
R 75	1	616-02-01009	RC07GF100J	RES,10 OHM 5% 1/4W	ALLEN BRAD
TP 1	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 2	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 3	1	143-98-00012	105-0856-001	JACK,TEST PT,PW TYPE,ORN	E F JOHNSON
TP 10	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
U 1	4	046-97-00069	SN7490N	IC,TTL CNTR,DECADE ASYN	TI/MML32
THRU					
U 4					
U 5	1	046-97-00251	SN74196N	IC,TTL CNTR/LCH,DECADE	TI/MML32
U 6	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 7	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 8	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
U 9	1	046-97-00187	SN74195N	IC,TTL SR,4BIT PRL OUT	TI/MML32
U 10	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 11	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
U 12	1	046-97-00119	SN74H11N	IC,HTTL GATE,AND 3-INP	TI/MML78
U 13	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
U 14	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
U 15	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
U 16	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
U 17	1	046-97-00119	SN74H11N	IC,HTTL GATE,AND 3-INP	TI/MML78
U 18	1	046-97-00069	SN7490N	IC,TTL CNTR,DECADE ASYN	TI/MML32
U 19	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
U 20	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 21	1	046-97-00176	SN74S151N	IC,STTL MUX, 8-INP	TI/MML80
U 22	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
U 23	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
U 24	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 25	1	046-97-00187	SN74195N	IC,TTL SR,4BIT PRL OUT	TI/MML32
U 26	1	046-97-00188	SN74166N	IC,TTL SR,8BIT SER OUT	TI/MML32
U 27	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 28	1	046-97-00067	SN7483AN	IC,TTL ADDR,BIN 4BIT FULL	TI/MML32
U 29	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 30	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 31	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
U 32	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 33	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
U 34	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 35	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
U 36	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
U 37	1	046-97-00167	SN74S112N	IC,STTL FF,J-K TYPE W/CLR	TI/MML80
U 38	1	046-97-00067	SN7483AN	IC,TTL ADDR,BIN 4BIT FULL	TI/MML32
U 39	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
U 40	1	046-97-00165	SN74S04N	IC,STTL INV	TI/MML80
U 41	1	046-97-00162	SN74S00N	IC,STTL GATE,NAND 2-INP	TI/MML80
U 42	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
U 43	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
U 44	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
U 45	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34592 REV DATE 12/20/79 REV LTR A
LIST TITLE - PWA,SIMULATOR 1 CHGE CONT NO. CODE IDENT SHT 3 OF
PART NO. - 205-89-01940 ECO 60261 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
R 18	1	616-02-30009	RC07GF301J	RES. 300 OHM 5% 1/4W	ALLEN BRAD
R 19	1	616-02-20009	RC07GF201J	RES,200 OHM 5% 1/4W	ALLEN BRAD
R 20	1	616-02-20009	RC07GF201J	RES,200 OHM 5% 1/4W	ALLEN BRAD
R 21	1	616-02-75009	RC07GF751J	RES,750 OHM 5% 1/4W	ALLEN BRAD
R 22	1	616-02-12000	RC07GF122J	RES,1.2K 5% 1/4W	ALLEN BRAD
R 23	1	616-02-39000	RC07GF392J/RCR07G392JS	RES,3.9K 5% 1/4W	AB/STACKPOLE
R 24	1	622-02-10009	RC20GF101J	RES. 100 OHM 5% 1/2W	ALLEN BRAD
R 25	1	608-09-10501	624	RES, 10.5K 1% 1/10W	EMR
R 26	1	608-09-78700	624	RES, 7.87K 1% 1/10W	EMR
R 27	1	608-09-71509	624	RES, 715.0 OHM 1% 1/10W	EMR
R 28	1	608-09-90900	624	RES. 9.09K 1% 1/10W	EMR
R 29	1	608-09-32400	624	RES. 3.24K 1% 1/10W	EMR
R 30	1	622-02-05109	RC20GF510J	RES, 51 OHM 5% 1/2W	ALLEN BRAD
R 31	1	608-09-18701	624	RES, 18.7K 1% 1/10W	EMR
R 32	1	608-09-11301	624	RES, 11.3K 1% 1/10W	EMR
R 33	1	616-02-15009	RC07GF151J	RES,150 OHM 5% 1/4W	ALLEN BRAD
R 34	1	608-09-59009	624	RES, 590.0 OHM 1% 1/10W	EMR
R 35	1	616-02-20000	RC07GF202J	RES,2K 5% 1/4W	ALLEN BRAD
R 36	1	616-02-20000	RC07GF202J	RES,2K 5% 1/4W	ALLEN BRAD
R 37	1	616-02-56009	RC07GF561J	RES,560 OHM 5% 1/4W	ALLEN BRAD
R 38	1	616-02-56009	RC07GF561J	RES,560 OHM 5% 1/4W	ALLEN BRAD
R 39	1	608-09-00000	624	RES,*TVAR* 1%,1/10W	EMR
R 40	1	201-98-00092	62PR2K	POT,TRMR, 2.0 K 10% .5W	BECK/MML27
R 41	1	608-09-57600	624	RES. 5.76K 1% 1/10W	EMR
R 42	1	616-02-15009	RC07GF151J	RES,150 OHM 5% 1/4W	ALLEN BRAD
R 43	1	608-09-49909	624	RES, 499.0 OHM 1% 1/10W	EMR
R 44	1	201-98-00093	62PR5K	POT,TRMR, 5.0 K 10% .5W	BECK/MML27
R 45	1	622-02-13009	RC20GF131J	RES, 130 OHM 5% 1/2W	ALLEN BRAD
R 46	1	616-02-20009	RC07GF201J	RES,200 OHM 5% 1/4W	ALLEN BRAD
R 47	1	616-02-05109	RC07GF510J	RES,51 OHM 5% 1/4W	ALLEN BRAD
R 48	1	622-02-13009	RC20GF131J	RES, 130 OHM 5% 1/2W	ALLEN BRAD
R 49	1	616-02-15009	RC07GF151J	RES,150 OHM 5% 1/4W	ALLEN BRAD
R 50	1	616-02-51000	RC07GF512J	RES,5.1K 5% 1/4W	ALLEN BRAD
R 51	1	622-02-07509	RC20GF750J	RES, 75 OHM 5% 1/2W	ALLEN BRAD
R 52	1	608-09-49900	624	RES. 4.99K 1% 1/10W	EMR
R 53	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R 54	1	201-98-00220	3339H-1-501	POT. 500 OHM 20% 1/2W	BOURNS
R 55	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR
R 56	1	616-02-75000	RC07GF752J	RES,7.5K 5% 1/4W	ALLEN BRAD
R 57	1	608-09-10001	624	RES. 10K 1% 1/10W	EMR
R 58	1	616-02-75000	RC07GF752J	RES,7.5K 5% 1/4W	ALLEN BRAD
R 59	1	608-09-10001	624	RES. 10K 1% 1/10W	EMR
R 60	1	608-09-10009	624	RES, 100.0 OHM 1% 1/10W	EMR
R 61	1	201-98-00136	62PR100	POT,TRMR,100 OHM 10% .5W	BECK/MML27
R 62	1	616-02-39001	RC07GF393J	RES,39K 5% 1/4W	ALLEN BRAD
R 63	1	608-09-75000	624	RES, 7.50K 1% 1/10W	EMR
R 64	1	608-09-45300	624	RES, 4.53K 1% 1/10W	EMR
R 65	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR
R 66	1	608-09-75000	624	RES, 7.50K 1% 1/10W	EMR
R 67	1	608-09-19600	624	RES, 1.96K 1% 1/10W	EMR
R 68	1	608-09-71500	624	RES. 7.15K 1% 1/10W	EMR
R 69	1	608-09-10000	624	RES. 1K 1% 1/10W	EMR
R 70	1	608-09-30101	624	RES, 30.1K 1% 1/10W	EMR

DATE 01/16/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34594 REV DATE 05/11/79 REV LTR C
LIST TITLE - PWA,SIMULATOR 2 CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01941 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00604	32957	PWB,UNIVERSAL CIRCUIT	EMR
2	1	299-98-00005	107	EJCTR/INSR,CARD,.062 BD	CALMARK CORP
3	73	236-98-00058	41018-01-016-1	SOCKET,IC,DIP,16PIN,WW	MML21
4	136	236-98-00057	41014-01-014-1	SOCKET,IC,DIP,14PIN,WW	MML21
5	1	299-99-00081	32199-7	EJCTR/INSR,.062BD,POSN7	EMR
6	1	279-99-00161	32971	SPRT,PWB	EMR
7	1	140-99-00248	32972	INSUL,PWB,.20X14.75 G10	EMR
8	5	229-02-00065	MS51957-3	SCREW,2-56X1/4 PAN HD	PRCMT OPTION
9	5	273-02-00024	MS35333-69	WASHER,#2,INT TOOTH	PRCMT OPTION
10	AR	276-98-00159	M30015-195A	WIRE,#30 SOL,MILENE,ALLOY	W.H.GORE
11	AR	273-02-00001	NAS620C2	WASHER,#2,FLAT,0.149 DIA	PRCMT OPTION
12	2	297-98-00149	9729-SS-0256	STDF,HEX, .562L,.187DIA	AMATOM
13	1	140-99-00260	34231	INSUL,PWA,9.68X15X.031THK	EMR
C 1	136	301-71-10001	8050002S5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 136					
C 137	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
C 138	1	337-13-10004	601	CAP., 10MF 10% 20V	EMR
E 104	64	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
E 167					
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
F 2	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
RA 1	3	182-98-00011	898-1-R1K	NTWK,RES,15/1.0K 2% 1W	BECK/MML47
THRU					
RA 3					
RA 15	3	182-98-00011	898-1-R1K	NTWK,RES,15/1.0K 2% 1W	BECK/MML47
THRU					
RA 17					
TP 4	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 5	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 10	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 15	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 20	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 25	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 30	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 35	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 40	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 45	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 49	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 50	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 51	4	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
THRU					
TP 54					
TP 55	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 56	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 57	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 60	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 65	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 67	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
UC 3	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 6	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 7	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32

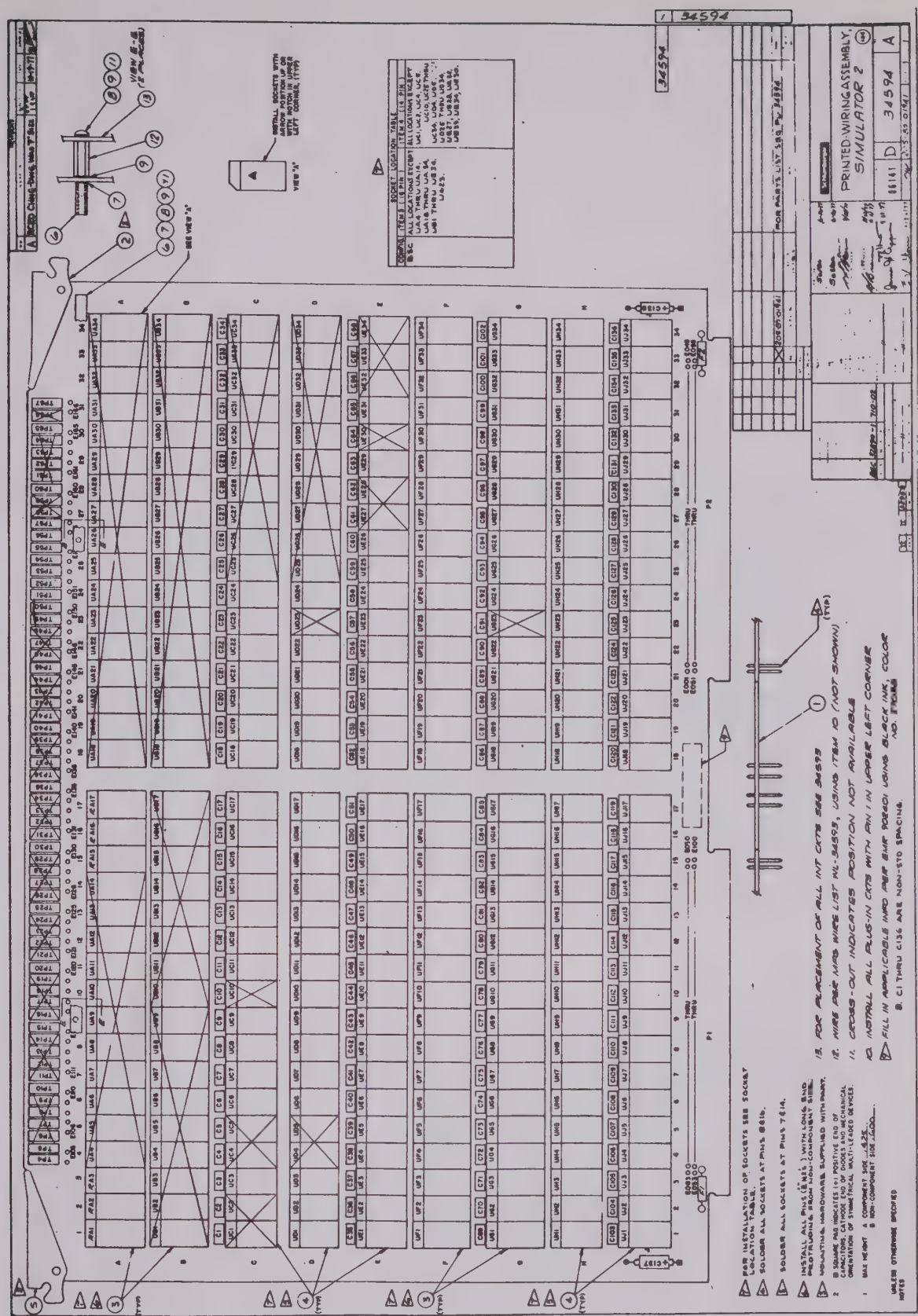
DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34592 REV DATE 12/20/79 REV LTR A
LIST TITLE - PWA,SIMULATOR 1 CHGE CONT NO. CODE IDENT SHT 5 OF
PART NO. - 205-89-01940 ECO 60261 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
U 46	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
U 47	1	046-97-00103	SN74151N	IC,TTL MUX, 8-INP	TI/MML32
U 48	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 49	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 50	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 51	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
U 52	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
U 53	1	046-97-00167	SN74S112N	IC,STTL FF,J-K TYPE W/CLR	TI/MML80
U 54	1	046-97-00110	SN74190N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
U * 55	1	046-97-00110	SN74190N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
U 56	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 57	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 58	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
U 59	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 60	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 61	1	046-97-00165	SN74S04N	IC,STTL INV	TI/MML80
U 62	1	046-97-00152	SN74S74N	IC,STTL FF,D POS EDGE	TI/MML80
U 63	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
U 64	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
U 65	1	046-97-00167	SN74S112N	IC,STTL FF,J-K TYPE W/CLR	TI/MML80
U 66	1	046-97-00110	SN74190N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
U 67	1	046-97-00110	SN74190N	IC,TTL CNTR,DECADE UP/DN	TI/MML32
U 68	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
U 69	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
U 70	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
U 71	1	046-97-00089	SN7442N	IC,TTL DCDR,BCD-TO-DEC	TI/MML32
U 72	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 73	1	046-34-00004	LM301AH	IC,LIN AMPL,OPNL	MML 40
U 74	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
U 75	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
U 76	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
U 77	1	046-97-00069	SN7490N	IC,TTL CNTR,DECADE ASYN	TI/MML32
U 78	1	046-97-00069	SN7490N	IC,TTL CNTR,DECADE ASYN	TI/MML32
U 79	1	046-97-00109	SN74107N	IC,TTL FF,J-K TYPE W/CLR	TI/MML32
U 80	1	046-16-00026	MC4044P	IC,TTL DET,PHASE-FREQ	MOT
U 81	1	046-97-00189	SN72558L	IC,LIN AMPL,OPNL,COMPEN	TI/MML40
U 82	1	046-97-00075	SN74121N	IC,TTL OSMV	TI/MML32
U 83	1	046-97-00075	SN74121N	IC,TTL OSMV	TI/MML32
U 84	1	046-97-00214	MC1658L	IC,ECL MV,VOLT-CONTROLLED	MOT/MML77
U 85	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
U 86	1	046-34-00004	LM301AH	IC,LIN AMPL,OPNL	MML 40
U 87	1	046-97-00078	SN74H00N	IC,HTTL GATE,NAND 2-INP	TI/MML78
U 88	1	046-34-00019	LH0033CG	IC,LIN AMPL,V FOL,FET-INP	NSC
U 89	1	046-18-00037	9614DC	IC,LIN DRVR,LINE DIFF	FCH/MML40
U 90	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
W 1 THRU W 3	3	021-99-00033	30080-1	BUSBAR,LAM,.32H,17 GROUPS	EMR
REF 1	1	905-01-01546	34590	SCHEM,PWA,SIMULATOR 1	EMR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR

FIRST MODEL USAGE 0710-02

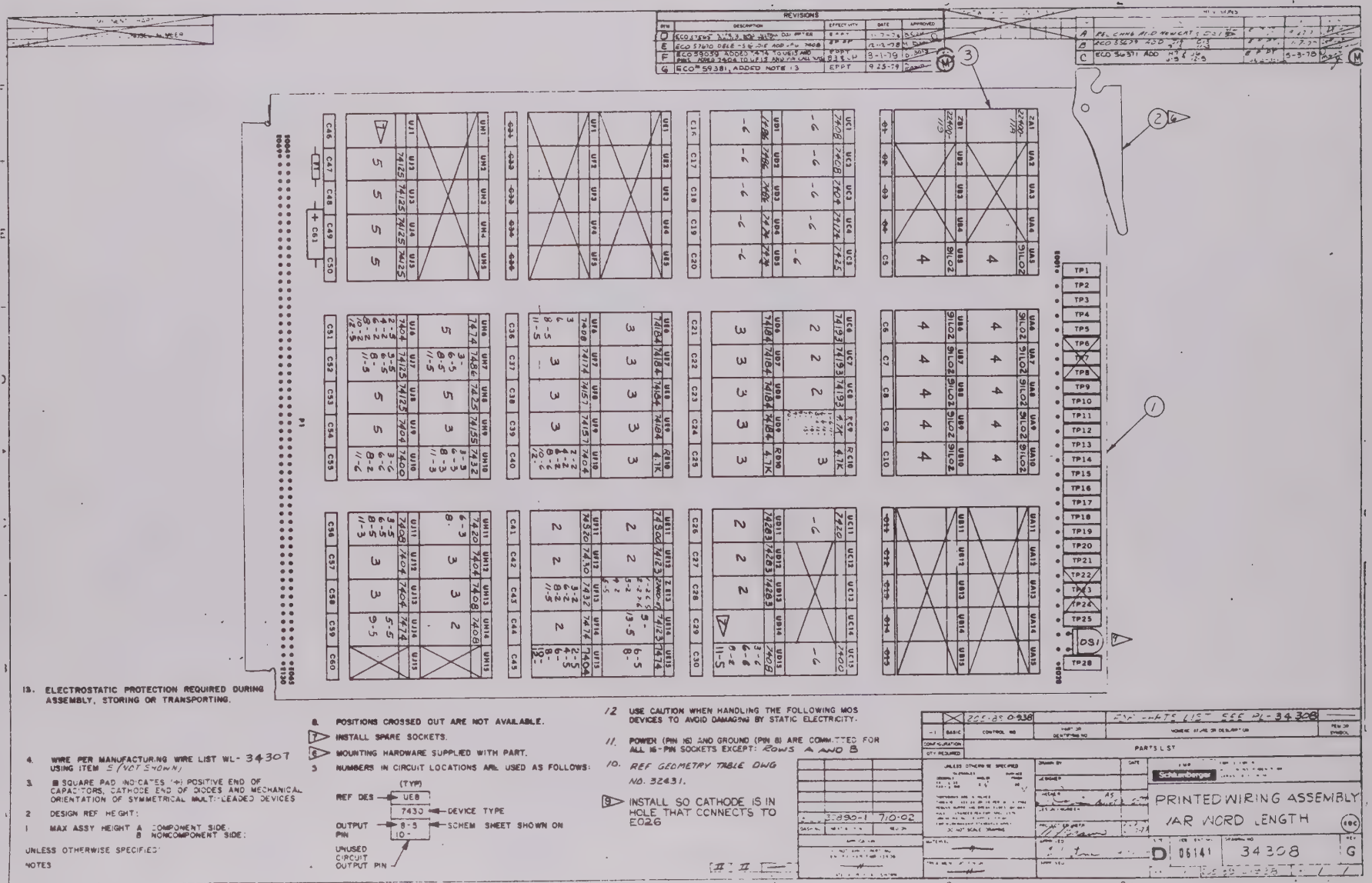
DATE 01/16/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34594 REV DATE 06/11/79 . REV LTR C
LIST TITLE - PWA,SIMULATOR 2 CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01941 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UC 8	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UC 9	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UC 11	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 12	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UC 13	3	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UC 15					
UC 16	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UC 17	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UC 18	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UC 19	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 20	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 21	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UC 22	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UC 23	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 24	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UD 1	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UD 2	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UD 3	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 6	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 7	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 8	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UD 9	3	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
THRU					
UD 11					
UD 12	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 13	3	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UD 15					
UD 16	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 17	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UD 18	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UD 19	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UD 20	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 21	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 22	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UD 24	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 1	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UE 2	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 3	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 4	4	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
THRU					
UE 7					
UE 8	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UE 9	3	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
THRU					
UE 11					
UE 12	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UE 13	1	046-97-00057	SN7451N	IC,TTL GATE,AND-OR-INV	TI/MML32
UE 14	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 15	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 16	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 17	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32


PRINTED-WIRING ASSEMBLY, SIMULATOR 2
34594
A
SOCKET LOCATION TABLE
FOR PARTS LIST SEE PL 34594
FOR INSTALLATION OF SOCKETS SEE SOCKET LOCATION TABLE.
SOLDER ALL SOCKETS AT PINS 8&16.
SOLDER ALL SOCKETS AT PINS 7&14.
INSTALL ALL PINS (8 NEG) WITH LONG END PROTRUDING FROM NON-COMPONENT SIDE.
MOUNTING HARDWARE SUPPLIED WITH PART.
2 B SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.
1 MAX HEIGHT A COMPONENT SIDE .425 B NON-COMPONENT SIDE .600
UNLESS OTHERWISE SPECIFIED NOTES
13. FOR PLACEMENT OF ALL INT CKTS SEE 34593
12. WIRE PER MFG WIRE LIST WL-34593, USING ITEM 10 (NOT SHOWN)
11. CROSS-OUT INDICATES POSITION NOT AVAILABLE
10. INSTALL ALL PLUS-IN CKTS WITH PIN 1 IN UPPER LEFT CORNER
9. FILL IN APPLICABLE INFO PER EMR 90601 USING BLACK INK, COLOR NO. 17038
8. C1 THRU C136 ARE NON-STD SPACING.

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UH 10	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 11	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 12	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UH 13	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 14	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 15	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 16	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UH 17	6	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UH 22					
UH 23	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 24	11	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UH 34					
UJ 1	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 2	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 3	1	046-97-00050	SN7410N	IC,TTL GATE,NAND 3-INP	TI/MML32
UJ 4	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 5	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UJ 6	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UJ 7	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 8	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UJ 9	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UJ 10	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 11	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 12	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UJ 13	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UJ 14	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 15	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 16	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UJ 17	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UJ 18	5	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UJ 22					
UJ 23	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 24	1	046-97-00083	SN7437N	IC,TTL BFR,NAND 2-INP	TI/MML32
UJ 25	10	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UJ 34					
P1E 3	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P1F 50					
P1E 53	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P1F100					
P2E 1	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P2E 48					
P2E 51	48	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
P2E 98					
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING	EMR
REF 2	1	905-31-00002	29330	GNTRY TABLE,XY,2WB 29328	EMR

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UE 18	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 19	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 20	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UE 21	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UE 22	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 23	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UE 24	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 25	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UE 26	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 29	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UE 31	1	046-97-00046	SN7402N	IC,TTL GATE,NOR 2-INP	TI/MML32
UF 1	1	046-97-00177	SN74161N	IC,TTL CNTR,BIN 4-BIT SYN	TI/MML32
UF 2	1	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
UF 3	1	046-97-00112	SN74170N	IC,TTL MEM,RAM 4X4	TI/MML9
UF 4	1	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
UF 5	7	046-97-00203	SN74160N	IC,TTL CNTR,DECADE 4-BIT	TI/MML 32
THRU					
UF 11					
UF 12	1	046-97-00188	SN74166N	IC,TTL SR,8BIT SER OUT	TI/MML32
UF 13	4	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
THRU					
UF 16					
UF 17	1	046-97-00188	SN74166N	IC,TTL SR,8BIT SER OUT	TI/MML32
UF 18	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 19	3	046-97-00089	SN7442N	IC,TTL DCDR,BCD-TO-DEC	TI/MML32
THRU					
UF 21					
UF 22	1	046-97-00111	SN74191N	IC,TTL CNTR,BIN UP/DN,SYN	TI/MML32
UF 23	12	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UF 34					
UG 1	1	046-97-00095	SN74155N	IC,TTL DEMUX,1-TO-4 LINE	TI/MML32
UG 2	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UG 3	15	046-97-00314	SN74LS170N	IC,LS MEM,RNDM ACS 4X4	TI/MML9
THRU					
UG 17					
UG 18	1	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UG 19	3	046-97-00089	SN7442N	IC,TTL DCDR,BCD-TO-DEC	TI/MML32
THRU					
UG 21					
UG 22	1	046-99-00011	24957-1	IC,TTL MEM,PROM 32X8	EMR
UG 24	11	046-97-00153	SN74175N	IC,TTL FF,D TYPE W/CLR	TI/MML32
THRU					
UG 34					
UH 1	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UH 2	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 4	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 5	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 6	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UH 7	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 8	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 9	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32



13. ELECTROSTATIC PROTECTION REQUIRED DURING ASSEMBLY, STORING OR TRANSPORTING.

8. POSITIONS CROSSED OUT ARE NOT AVAILABLE.

△ INSTALL SPARE SOCKETS.

△6 MOUNTING HARDWARE SUPPLIED WITH PART.

5 NUMBERS IN CIRCUIT LOCATIONS ARE USED AS FOLLOWS:

(TYP)
REF DES — UE8
7430 — DEVICE TYPE
OUTPUT PIN — 8-5 — SCHEM SHEET SHOWN ON
10-
UNUSED CIRCUIT OUTPUT PIN

4. WIRE PER MANUFACTURING WIRE LIST WL- 34307 USING ITEM 5 (NOT SHOWN)

3. ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES

2. DESIGN REF HEIGHT:

1. MAX ASSY HEIGHT A COMPONENT SIDE.
B NONCOMPONENT SIDE:

UNLESS OTHERWISE SPECIFIED

NOTES

12 USE CAUTION WHEN HANDLING THE FOLLOWING MOS DEVICES TO AVOID DAMAGING BY STATIC ELECTRICITY.

11. POWER (PIN 16) AND GROUND (PIN 8) ARE COMMITTED FOR ALL 16-PIN SOCKETS EXCEPT: ROWS A AND B

10. REF GEOMETRY TABLE DWG NO. 32431.

9 INSTALL SO CATHODE IS IN HOLE THAT CONNECTS TO E026

PARTS LIST

DATE 01/16/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 34594
LIST TITLE - PWA,SIMULATOR 2
PART NO. - 205-89-01941

REV DATE 06/11/79
CHGE CONT NO.
ECO RECORD 1

CODE IDENT 06141

REV LTR C
SHT 5 OF
CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
REF 3	1	905-01-01547	34593	SCHEM,PWA,SIMULATOR 2	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34308 REV DATE 12/20/79 REV LTR D
LIST TITLE - PWA,VAR WORD LENGTH CHGE CONT NO. CODE IDENT SHT 2 OF
PART NO. - 205-89-01938 ECO 60257 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
UC 11	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UC 15	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UD 1	3	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
THRU					
UD 3					
UD 4	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 5	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UD 6	4	046-97-00169	SN74184N	IC,TTL CONV,BCD-TO-BIN	TI/MML32
THRU					
UD 9					
UD 11	3	046-97-00247	SN74283N	IC,TTL ADDR,BIN 4BIT FULL	TI/MML32
THRU					
UD 13					
UD 15	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UE 6	4	046-97-00169	SN74184N	IC,TTL CONV,BCD-TO-BIN	TI/MML32
THRU					
UE 9					
UE 11	1	046-97-00162	SN74S00N	IC,STTL GATE,NAND 2-INP	TI/MML80
UE 12	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UE 14	1	046-97-00160	SN74123N	IC,TTL OSMV,RETRIG	TI/MML32
UE 15	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UF 6	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UF 7	1	046-97-00178	SN74174N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UF 8	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 9	1	046-97-00105	SN74157N	IC,TTL MUX, 2-INP	TI/MML32
UF 10	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UF 11	1	046-97-00171	SN74S20N	IC,STTL GATE,NAND 4-INP	TI/MML80
UF 12	1	046-97-00054	SN7430N	IC,TTL GATE,NAND 8-INP	TI/MML32
UF 13	1	046-97-00088	SN7432N	IC,TTL GATE,OR 2-INP	TI/MML32
UF 14	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UF 15	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 6	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
UH 7	1	046-97-00068	SN7486N	IC,TTL GATE,EXCL-OR 2-INP	TI/MML32
UH 8	1	046-97-00210	SN7425N	IC,TTL GATE,NOR 4-INP	TI/MML32
UH 9	1	046-97-00095	SN74155N	IC,TTL DEMUX,1-TO-4 LINE	TI/MML32
UH 10	1	046-97-00088	SN7432N	IC,TTL GATE,OR 2-INP	TI/MML32
UH 11	1	046-97-00052	SN7420N	IC,TTL GATE,NAND 4-INP	TI/MML32
UH 12	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UH 13	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UH 14	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 2	4	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
THRU					
UJ 5					
UJ 6	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 7	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UJ 8	1	046-97-00212	SN74125N	IC,TTL BFR,3-STATE BUS	TI/MML32
UJ 9	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 10	1	046-97-00044	SN7400N	IC,TTL GATE,NAND 2-INP	TI/MML32
UJ 11	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UJ 12	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 13	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UJ 14	1	046-97-00064	SN7474N	IC,TTL FF,D TYPE POS EDGE	TI/MML32
ZA 1	1	182-89-00224	22400-118	NTWK,JUMPER	EMR

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA
PARTS LIST - 34308 REV DATE 12/20/79 REV LTR D
LIST TITLE - PWA,VAR WORD LENGTH CHGE CONT NO. CODE IDENT SHT 1 OF
PART NO. - 205-89-01938 ECO 60257 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	204-89-00608	34306	PWB,UNIVERSAL CKT,120 DIP	EMR
2	1	299-99-00076	32199-2	EJCTR/INSR,.062CD,POSN2	EMR
3	84	236-98-00058	41018-01-016-1	SOCKET,IC,DIP,16PIN,WW	MML21
5	AR	276-98-00159	M30015-195A	WIRE,#30 SOL,MILENE,ALLOY	W.H.GORE
C 5	6	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 10					
C 16	15	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 30					
C 36	25	301-71-10001	805000Z5U0103Z/TA-.01	CAP, .01UF +80-20% 100V	ERIE/MALLORY
THRU					
C 60					
C 61	1	337-12-22004	601	CAP., 22MF 10% 15V	EMR
DS 1	1	137-98-00019	XC556-2	IND,LED,RED,.200 OD,.340L	XCITON
E 1	5	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
E 5					
E 9	13	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
E 21					
E 25	4	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
THRU					
E 28					
F 1	1	120-98-00048	275005	FUSE,SUBMIN,5A @ 125V	LITTELFUSE
RC 9	1	182-98-00017	898-1-R4.7K	NTWK,RES,15/4.7K 2% 1W	BECK/MML47
RC 10	1	182-98-00017	898-1-R4.7K	NTWK,RES,15/4.7K 2% 1W	BECK/MML47
RD 10	1	182-98-00017	898-1-R4.7K	NTWK,RES,15/4.7K 2% 1W	BECK/MML47
RE 10	1	182-98-00017	898-1-R4.7K	NTWK,RES,15/4.7K 2% 1W	BECK/MML47
TP 1	5	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
THRU					
TP 5					
TP 9	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 10	1	143-98-00058	430-103	JACK,TEST PT,PW TYPE,BLK	MML 16
TP 11	11	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
THRU					
TP 21					
TP 25	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
TP 28	1	143-98-00051	430-102	JACK,TEST PT,PW TYPE,RED	MML 16
UA 5	6	046-97-00318	SYP21L02B/AM91L02BPC	IC,MOS MEM,RAM 1024X1,STA	SYNERTEK/AMD
THRU					
UA 10					
UB 5	6	046-97-00318	SYP21L02B/AM91L02BPC	IC,MOS MEM,RAM 1024X1,STA	SYNERTEK/AMD
THRU					
UB 10					
UC 1	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 2	1	046-97-00049	SN7408N	IC,TTL GATE,AND 2-INP	TI/MML32
UC 3	1	046-97-00047	SN7404N	IC,TTL INV	TI/MML32
UC 4	1	046-97-00178	SN74174N	IC,TTL FF,D TYPE W/CLR	TI/MML32
UC 5	1	046-97-00210	SN7425N	IC,TTL GATE,NOR 4-INP	TI/MML32
UC 6	3	046-97-00077	SN74193N	IC,TTL CNTR,BIN UP/DN SYN	TI/MML32
THRU					
UC 8					

DATE 01/14/80 8MG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 33101
LIST TITLE - KIT,POWER SUPPLY
PART NO. - 147-89-00019

REV DATE 09/01/77 REV LTR D
CHGE CONT NO. CODE IDENT SHT 1 OF
ECO 55320 06141 CKD BY

ITEM NO.		QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
	1	1	202-98-00036	2J15D-.5B	PWR SPLY,DUAL 12/15V@0.5A	POWERTEC
	2	3	297-98-00103	8158-SS-0832/MML 10	STDF,1/4 DX8-32X5/8 SST	MML 10
	3	AR	229-02-00100	MS51957-43	SCREW,8-32X3/8 PAN HD	PRCMT OPTION
	4	AR	273-02-00008	MS15795-807	WASHER,#8, FLT ST STL	PRCMT OPTION
	5	AR	273-02-00027	MS35333-72	WASHER,#8,INT TOOTH	PRCMT OPTION
	6	1	255-98-00015	1486-10	TERM,LUG,SOLDER,#10HOLE	H H SMITH
	7	5	065-98-00027	60620-1	CONT,PIN,#20-14AWG TIN	AMP
	8	3	065-98-00026	60619-1	CONT,SKT,#20-14AWG TIN	AMP
	9	AR	276-98-00064	NAS-703-18-U-C-9	WIRE,#18,STRD,WHT,600V	MML42
J	1	1	063-98-00264	1-480303-0	CONN,RECT, 3 CONT,PLUG	AMP INC
P	1	1	063-98-00230	1-480340-0	CONN,RECT, 6 CONT,RCPT	AMP

FIRST MODEL USAGE 0710-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 34308 REV DATE 12/20/79 REV LTR D

LIST TITLE - PWA,VAR WORD LENGTH CHGE CONT NO. CODE IDENT SHT 3 OF

PART NO. - 205-89-01938 ECO 60257 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
ZB 1	1	182-89-00225	22400-119	NTWK,JUMPER	EMR
ZE 13	1	182-89-00138	22400-117	NTWK,SPECIAL	EMR
P1E 4 THRU P1E 65	62	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
P1E 69 THRU P1E130	62	065-98-00045	75481-014	CONT,PIN,.025SQ, .620L	BERG ELECT
REF 1	1	905-01-01544	34307	SCHEM,PWA,VAR WD LENGTH	EMR
REF 2	1	905-01-01545	34309	SCHEM,PWA,DATA ENTRY	EMR
REF 3	1	905-31-00026	32431	GMTRY TABLE,XY,PWB 34306	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-73
LIST TITLE - NTWK,2 RES,2 CAP,1 DIODE
PART NO. - 182-89-00013

REV DATE 08/09/74
CHGE CONT NO.
ECO

CODE IDENT 06141

REV LTR
SHT 1 OF
CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
	1	1 015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
C	1	1 301-33-33003	8151-050-651-335M/MML	CAP,CR , 50V 3.30UF 20%	MML 48
C	2	1 304-20-13009	600	CAP. 130PF 1% 500V	EMR
CR	1	1 088-10-41480	1N4148	DIODE,SW,75V/5UA,4NS/10MA	JEDEC
R	1	1 616-02-20001	RC07GF203J	RES,20K 5% 1/4W	ALLEN BRAD
R	2	1 616-02-20001	RC07GF203J	RES,20K 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0711-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 33100 REV DATE 10/06/76 REV LTR

LIST TITLE - KIT,CARD READER CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 147-89-00018 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	016-99-00415	30878	BRKT,CARD READER	EMR
2	1	253-06-00002	11310A	RDR,CARD,96CHAR HOLLERITH	HEWLETT-P
3	14	065-98-00030	66308-3	CONT,PIN,#24-20AWG GOLD	AMP
4	1	194-98-00061	R62-3	PIN,CONTACT	BEAD CHAIN
5	1	194-98-00068	200390-4	PIN,GUIDE,CENTER,FEMALE	AMP
6	1	285-98-00008	201378-2	HOOD,14 POSN,1 PIECE,LONG	AMP
7	AR	276-98-00107	NAS-703-26-U-C-9	WIRE,#26,STRD,WHT,600V	MML42
8	AR	276-98-00070	NAS-703-20-U-C-9	WIRE,#20,STRD,WHT,600V	MML42
9	AR	268-98-00015	RNF-100-3/8-BLK	TBG, 3/8 ,THERMO-FIT,BLK	RACHEM/MML82
10	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
P 1	1	063-98-00244	201297-1	CONN,BLOCK,14 POSN	AMP
REF 1	1	905-13-00302	30156	WIRING DIAGRAM,CD&PT RDRS	EMR

FIRST MODEL USAGE 0710-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-75 REV DATE 01/09/78 REV LTR A

LIST TITLE - NTWK CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00015 ECO 55724 06141 CKD BY

ITEM NO.	QTY REQD		STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
	1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
C	1	1	304-00-00000	600	CAP,*TVAR*	EMR
C	2	1	304-00-00000	600	CAP,*TVAR*	EMR
R	1	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0711-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-74 REV DATE 05/22/75 REV LTR A

LIST TITLE - NTWK,4 RES,2 CAPACITOR CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00014 ECO 51973 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
C 1	1	304-20-13009	600	CAP. 130PF 1% 500V	EMR
C 2	1	304-20-13009	600	CAP. 130PF 1% 500V	EMR
R 1	1	616-02-20001	RC07GF203J	RES,20K 5% 1/4W	ALLEN BRAD
R 2	1	616-02-20001	RC07GF203J	RES,20K 5% 1/4W	ALLEN BRAD
R 3	1	616-02-20009	RC07GF201J	RES,200 OHM 5% 1/4W	ALLEN BRAD
R 4	1	616-02-20009	RC07GF201J	RES,200 OHM 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0711-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-77 REV DATE 08/09/74 REV LTR

LIST TITLE - NTWK,1RES,1CAPACITOR CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00017 ECO 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00029	H-2723-01	BOARD,CMPNT,14PIN@.1X.3SP	EECO/MML57
C	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR
R	1	616-02-51000	RC07GF512J	RES,5.1K 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0711-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-76
LIST TITLE - NTWK,3 RES,1 XTR,1 DIODE
PART NO. - 182-89-00016

REV DATE 08/09/74
CHGE CONT NO.
ECO

CODE IDENT 06141

REV LTR
SHT 1 OF
CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
C	1	301-13-10003	8131-050-651-105M/MML	CAP,CR , 50V 1.00UF 20%	MML 48
CR	1	088-10-41480	1N4148	DIODE,SW,75V/5UA,4NS/10MA	JEDEC
Q	1	263-38-00019	SU676 SEE EMR 9026	XSTR,FET P-CHAN,-30V	SILICONIX
R	1	616-02-10000	RC07GF102J	RES,1K 5% 1/4W	ALLEN BRAD
R	2	616-02-10009	RC07GF101J	RES,100 OHM 5% 1/4W	ALLEN BRAD
R	3	616-02-22002	RC07GF224J	RES,220K 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0711-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-117 REV DATE 12/01/77 REV LTR A

LIST TITLE - NTWK,SPECIAL CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00138 ECO 55419 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTRCL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
C	1	304-08-02009	600	CAP.,20PF .5PF 500V	EMR
C	2	304-08-03609	600	CAP. 36PF .5PF 500V	EMR
C	3	304-01-01009	600	CAP. 10PF .5PF 500V	EMR
R	1	616-02-10001	RC07GF103J	RES,10K 5% 1/4W	ALLEN BRAD
R	2	616-02-10001	RC07GF103J	RES,10K 5% 1/4W	ALLEN BRAD
R	3	616-02-51000	RC07GF512J	RES,5.1K 5% 1/4W	ALLEN BRAD
R	4	616-02-22009	RC07GF221J	RES,220 OHM 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-78 REV DATE 01/20/77 REV LTR C

LIST TITLE - NTWK,1RES 20K,1CAP 130PF CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00018 ECO 54174 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
C 1	1	304-20-13009	600	CAP. 130PF 1% 500V	EMR
C 2	1	304-00-00000	600	CAP,*TVAR*	EMR
C 3	1	301-13-10003	8131-050-651-105M/MML	CAP,CR , 50V 1.00UF 20%	MML 48
R 1	1	616-02-20001	RC07GF203J	RES,20K 5% 1/4W	ALLEN BRAD
R 2	1	616-02-51000	RC07GF512J	RES,5.1K 5% 1/4W	ALLEN BRAD

FIRST MODEL USAGE 0711-

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-119
LIST TITLE - NTWK,JUMPER
PART NO. - 182-89-00225

REV DATE 10/20/77
CHGE CONT NO.
ECO

CODE IDENT 06141

REV LTR
SHT I OF
CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
2	AR	276-99-00010	619-26	WIRE,#26,BUSS,SOLID	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-118 REV DATE 10/20/77 REV LTR

LIST TITLE - NTWK,JUMPER CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00224 ECO 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
2	AR	276-99-00010	619-26	WIRE,#26,BUSS,SOLID	EMR

FIRST MODEL USAGE 0710-02

DATE 01/14/80 BMG011 SANGAMO WESTON, SARASOTA

PARTS LIST - 22400-120 REV DATE 01/09/78 REV LTR

LIST TITLE - NTWK,SPIKE FILTER CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. - 182-89-00271 ECO 06141 CKD BY

ITEM NO.	QTY REQD	STOCK CONTROL NO.	DRAWING SPEC OR VENDOR NUMBER	DESCRIPTION	VENDOR NAME
1	1	015-98-00030	H-2723-03	BOARD,CMPNT,16PIN@.1X.3SP	EECO/MML57
R 1	1	304-20-30009	600	CAP. 300PF 1% 500V	EMR

FIRST MODEL USAGE 0710-02

32938

REVISIONS

SYM	DESCRIPTION	EFFECTIVITY	DATE	APPROVED
A	RCD CHNG RE-DRAWN W/O CHNG ALL SH; ADD 22 & 23	EPPT 5-26-77	5-26-77	[illegible] Brown
B	RCD CHNG SH. 8, 12, 14 ADD 710-02 DATA	EPPT 6-30-77	6-30-77	BRAWN Brown
C	ECO55447 CORRECTED ERRORS SHTS 11 & 14	EPPT 1 & UP	9-9-77	[illegible]
D	ECO55557 A1 WAS A2 SHTS 22,23	EPPT 1 & UP	1-28-77	[illegible] Brown
E	RCD CHNG AT TOP OF PAGE CHNG REF FROM 711 TO 710 SH 7 & 8	EPPT 1 & UP	10/20/77	BRAWN Brown
F	ECO 55645 WAS WINC NOW WDRATE ADD INF E12 & F11 SHT 14 SHT 23	EP PT SN13 & UP	10-26-77	[illegible] Brown
G	ECO 56078 ADDED A5J38 SHT 24 & 25	EP PT 24,25, & [illegible] UP	3-7-78	[illegible]

3 A5J37 & A5J38 USED ON 710-02 ONLY (SH 22, 23, 24 & 25).

2. ALL WIRING IS #26 TWPR UNLESS OTHERWISE SPECIFIED.

1 THIS DOCUMENT IS COMPLETE WITHOUT PAGES 2, 3, 4, 16, 17, 19 & 20.

NOTES:

SIMILAR TO 30163

		DRAWN BY RON RAGHAM	DATE 8-19-76
		DESIGNER [illegible]	8-19-76
		CHECKER [illegible]	[illegible]
32800-1	710-02	DESIGN ENGINEER	
32800	710	PROJECT ENGINEER [illegible]	8-23-77
NEXT ASSY NO.	USED ON	APPROVED [illegible]	2-22-77
APPLICATION		APPROVED	
II	II		
GRADE	CATEGORY		

EMR — EMR Schlumberger

EMR TELEMETRY
WESTON INSTRUMENTS, INC.
BOX 3041-SARASOTA FLORIDA 33578

I/O CONNECTOR LIST
MODEL 710

SIZE	CODE IDENT NO.	DRAWING NO	REV
A	06141	32938	G

SCALE —"— 905-25-00066 SHEET 1 OF 25

EMR 3/2/31C

1

A5.J30 Comp. I/O

Setup Input

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	DOR 1		A1J16P118
B1	GND		J16E51
A4	DOR 2		J16P119
B3	GND		J16E51
A6	DOR 3		J16P120
B5	GND		J16E51
A8	DOR 4		J16P128
B7	GND		J16E63
A10	DOR 5		J16P124
B9	GND		J16E57
A12	DOR 6		J16P123
B11	GND		J16E54
D13	DOR 7		J16P112
B13	GND		J16E45
C2	DOR 8		J16P113
D1	GND		J16E45
C4	DOR 9		J16P114
D3	GND		J16E45
C6	DOR 10		J16P122
D5	GND		J16E54
C8	DOR 11		J16P129
D7	GND		J16E63
C10	DOR 12		J16P130
D9	GND		J16E63
C12	DOR 13		J16P115
D11	GND		A1J16E48

CODE IDENT NO.	SIZE		REV
06141	A	32938	A
SCALE —			SHEET 5

A5 J30 Comp. I/O

Setup Input

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2	DOR 14		A1J16P116
F1	GND		J16E48
E4	DOR 15		J16P117
F3	GND		J16E48
E6	DOR 16		J16P127
F5	GND		J16E57
E8	INSTRB		J16P121
F7	GND		J16E54
E10	INRQ		J16P56
F9	GND		A1J16E57
E12			
F11			
H13			
F13			
G2			
H1			
G4			
H3			
G6			
H5			
G8			
H7			
G10			
H9			
G12			
H11			

CODE IDENT NO.	SIZE		REV
06141	A	32938	A
SCALE —			SHEET 6

EMR 3/2/24 gaf OZALID

A5 J31 Comp. I/O

710 Data Output

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	CMPD 1		A1J16P21
B1	GND		J16E18
A4	CMPD 2		J16P24
B3	GND		J16E18
A6	CMPD 3		J16P28
B5	GND		J16E24
A8	CMPD 4		J16P31
B7	GND		J16E24
A10	CMPD 5		J16P97
B9	GND		J16E42
A12	CMPD 6		J16P18
B11	GND		J16E18
D13	CMPD 7		J16P100
B13	GND		J16E42
C2	CMPD 8		J16P25
D1	GND		J16E24
C4	CMPD 9		J16P52
D3	GND		J16E39
C6	CMPD 10		J16P54
D5	GND		J16E42
C8	CMPD 11		J16P110
D7	GND		J16E36
C10	CMPD 12		J16P108
D9	GND		J16E33
C12	CMPD 13		J16P48
D11	GND		A1J16E39

EDC

CODE IDENT NO.	SIZE		REV
06141	A	32938	E
SCALE —H—			SHEET 7

A5 J31 Comp. I/O

710 Data Output

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2	CMPD 14		A1J16P50
F1	GND		J16E39
E4	CMPD 15		J16P105
F3	GND		J16E33
E6	CMPD 16		J16P107
F5	GND		J16E33
E8	DATARDY		J14P83
F7	GND		J14E40
E10	ACK		J14P82
F9	GND		J14E40
E12	EXT STRT		J16P59
F11	GND		J14E40
H13	TIME NAB	A1J5P74 } 710-02	J13P95 }
F13	GND	A1J5E32 }	A1J13E32 } 710-01
G2	PAR DATA 1	710-02 Only	A1J6P90
H1	GND	710-02 Only	A1J6E40
G4			
H3			
G6			
H5			
G8			
H7			
G10			
H9			
G12			
H11			

CODE IDENT NO.	SIZE		REV
06141	A	32938	E
SCALE —H—			SHEET 8

A5 J32 System I/O

Setup Output

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	Setup 1		A1 J5 P55
B1	GND		J5 E6
A4	Setup 2		J5 P56
B3	GND		J5 E6
A6	Setup 3		J5 P57
B5	GND		J5 E10
A8	Setup 4		J5 P58
B7	GND		J5 E10
A10	Setup 5		J5 P59
B9	GND		J5 E10
A12	Setup 6		J5 P60
B11	GND		J5 E12
D13	Setup 7		J5 P61
B13	GND		J5 E12
C2	Setup 8		J5 P62
D1	GND		J5 E12
C4	Setup 9		J5 P63
D3	GND		J5 E16
C6	Setup 10		J5 P64
D5	GND		J5 E16
C8	Setup 11		J5 P65
D7	GND		J5 E16
C10	Setup 12		J5 P66
D9	GND		J5 E18
C12	Setup 13		J5 P67
D11	GND		A1 J5 E18

EDO

CODE IDENT NO.	SIZE		REV
06141	A	32938	A
SCALE —/1—			SHEET 9

A5 J32 System I/O

Setup Output

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2	Setup 14		A1 J5 P68
F1	GND		J5 E18
E4	Setup 15		J5 P69
F3	GND		J5 E20
E6	Setup 16		J5 P70
F5	GND		J5 E20
E8	Setup STRB		J5 P71
F7	GND		J5 E20
E10	INRQ In		J16 P46
F9	GND		J16 E36
E12	Flag 11		J13 P66
F11	GND		J13 E16
H13	Flag 12		J13 P67
F13	GND		J13 E16
G2	Flag 13		J13 P68
H1	GND		J13 E16
G4	Flag 14		J13 P69
H3	GND		J13 E18
G6	Flag 15		J13 P70
H5	GND		J13 E18
G8	Flag 16		J13 P71
H7	GND		J13 E18
G10	/ENCRPST		J16 P44
H9	GND		J16 E36
G12	/CRSTDLY		J16 P45
H11	GND		A1 J16 E39

CODE IDENT NO.	SIZE		REV
06141	A	32938	A
SCALE			SHEET 10

A5 J33 System I/O

S Frame Timing, System Status

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	SF Rate 1		A1 J7 P25
B1	GND		J7 E20
A4	SF Rate 2		J8 P32
B3	GND		J8 E30
A6	SF INC 1		J7 P26
B5	GND		J7 E22
A8	SF INC 2		J7 P29
B7	GND		J7 E22
A10	SFRS 1		J7 P27
B9	GND		J7 E32
A12	SFRS 2		J7 P30
B11	GND		J7 E32
D13	SFPRSEN 1		J7 P28
B13	GND		J7 E22
C2	SFPRSEN 2		J7 P31
D1	GND		J7 E34
C4	SF Search		J7 P91
D3	GND		J7 E40
C6	SF Verify		J7 P92
D5	GND		J7 E40
C8	SF Lock		J7 P93
D7	GND		J7 E40
C10	SF Check		J7 P94
D9	GND		J7 E42
C12	SF 2 Search		J7 P83
D11	GND		A1 J7 E34

CODE IDENT NO.	SIZE		REV
06141	A	32938	C
SCALE —H—			SHEET 11

A5 J33 System I/O

S Frame Timing, System Status

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2	SF2 Verify		A1 J7 P84
F1	GND		J7 E34
E4	SF2 Lock		J7 P85
F3	GND		J7 E34
E6	SF2 Check		J7 P86
F5	GND		J7 E36
E8	F Search		J5 P87
F7	GND		J5 E32
E10	F Verify		J5 P88
F9	GND		J5 E34
E12	F Lock		J5 P89
F11	GND		J5 E34
H13	F Check		J5 P90
F13	GND		A1 J5 E34
G2	PAR DATA 2	710-02 Only	A1 J6 P97
H1	GND	710-02 Only	A1 J6 E40
G4			
H3			
G6	RDY		A1 J6 P98
H5	GND		A1 J6 E40
G8			
H7			
G10	Frate		A1 J13 P29
H9	GND		A1 J13 E30
G12			
H11			

CODE IDENT NO.	SIZE		REV
06141	A	32938	B
SCALE —			SHEET 12

A5 J34 System I/O

Parallel Data Output and Timing

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	Parallel Data Out 1		A1 J13 P53
B1	GND		J13 E4
A4	2		J13 P54
B3	GND		J13 E4
A6	3		J13 P55
B5	GND		J13 E4
A8	4		J13 P57
B7	GND		J13 E6
A10	5		J13 P58
B9	GND		J13 E6
A12	6		J13 P60
B11	GND		J13 E6
D13	7		J13 P61
B13	GND		J13 E8
C2	8		J13 P62
D1	GND		J13 E8
C4	9		J13 P63
D3	GND		J13 E8
C6	10		J13 P65
D5	GND		J13 E10
C8	11		J13 P72
D7	GND		J13 E20
C10	12		J13 P73
D9	GND		J13 E20
C12	13		J13 P74
D11	GND		A1 J13 E20

EDC

CODE IDENT NO.	SIZE		REV
06141	A	32938	A
SCALE —			SHEET 13

A5 J34 System I/O

Parallel Data Output and Timing

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2	Parallel Data Out 14		A1J13P75
F1	GND		J13E22
E4	15		J13P76
F3	GND		J13E22
E6	16		J13P77
F5	GND		J13E22
E8	WD INC	A1J5P80 -	J13P25
F7	GND	A1J5PE36 710-02	J13E18 710-01
E10	WDRS	A1J5P100	J13P26
F9	GND	A1J5PE50	J13E18 710-01
E12	Frame Rate	A1J14P9	J13P29
F11	GND	A1J14E10	J13E32
H13	WDPRSEN		J13P27
F13	GND		J13E18
G2	Word Rate		J13P28
H1	GND		J13E32
G4	Word Sel Strobe		J13P21
H3	GND		A1J13E18
G6			
H5			
G8			
H7			
G10			
H9			
G12			
H11			

CODE IDENT NO.	SIZE		REV
06141	A	32938	F
SCALE —			SHEET 14

A5 Simulator I/O

CONN	SIGNAL	TO/FROM	
J2	EXT CLK	SIG	A1 J9 P77
		SHLD	J9 E30
J3	DATA ENABLE	SIG	J10 P72
		SHLD	J10 E10
J4	NOISE	SIG	J10 P73
		SHLD	J10 P23
J5	DEV	SIG	J9 P55
		SHLD	J9 P5
J6	NRZL	SIG	J10 P15
		SHLD	J10 E10
J7	0° CLK	SIG	J9 P96
		SHLD	J9 E50
J8	PCM 1	SIG	J10 P96
		SHLD	J10 P46
J9	PCM 2	SIG	J10 P21
		SHLD	A1 J10 E20
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	

SIZE	CODE IDENT NO.	DRAWING NO.	
A	06141	32938	A
SCALE			SHEET 15

A5 F Sync

CONN	SIGNAL	TO/FROM	
J22	EXT 1 DATA	SIG	A1 J5 P42
		SHLD	J5 E38
J23	EXT 1 CLK	SIG	J5 P43
		SHLD	J5 E42
J24	EXT 2 DATA	SIG	J5 P44
		SHLD	J5 E40
J25	EXT 2 CLK	SIG	J5 P45
		SHLD	J5 E44
J26	EXT 3 DATA	SIG	J5 P46
		SHLD	J5 E46
J27	EXT 3 CLK	SIG	J5 P47
		SHLD	A1 J5 E48
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	
		SIG	
		SHLD	

SIZE	CODE IDENT NO.	DRAWING NO.	
A	06141	32938	A
SCALE			SHEET 18

A5 J36 Card Reader

PIN NO.	SIGNAL	REMARKS	TO/FROM
A	CRSET 1 (/CRDATA 1)	#26	A1 J16 P3
B	2 2		P4
C	3 3		P5
D	4 4		P6
E	5 5		P7
F	6 6		P8
H	7 7		P9
J	CRSET 8(/CRDATA 8)		P10
K			
L	/CRSTROBE		P86
M	/CARDPRSNT	#26	A1 J16 P37
N	GND	#20	A1 E010
P			
R	+5V	#20	A1 E101

CODE IDENT NO.	SIZE		REV
06141	A	32938	A
SCALE — H —			SHEET 21

3

A5 J37 Data Port 2 Out

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	PORT 2 B1		A1 J2 P4
B1	GND		E3
A4	B2		P5
B3	GND		E3
A6	B3		P6
B5	GND		E6
A8	B4		P7
B7	GND		E6
A10	B5		P8
B9	GND		E9
A12	B6		P9
B11	GND		E9
D13	B7		P10
B13	GND		E12
C2	B8		P11
D1	GND		E12
C4	B9		P12
D3	GND		E15
C6	B10		P13
D5	GND		E15
C8	B11		P14
D7	GND		E18
C10	B12		P15
D9	GND		E18
C12	PORT 2 B13		P16
D11	GND		A1 J2 E21

CODE IDENT NO.	SIZE		REV
06141	A	32938	D
SCALE —H—			SHEET 22

3 A5J37 Data Port 2 Out

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2	PORT 2 B14		A1 J2 P17
F1	GND		E21
E4	B15		P18
F3	GND		E24
E6	B16		P19
F5	GND		E24
E8	DATA RDY		P20
F7	GND		P21
E10	ACK		P22
F9	GND		E27
E12	FRATE		P85
F11	GND		E27
H13	WDRATE		P86
F13	GND		E30
G2	WDRST		P87
H1	GND		E30
G4	EXT STRT		P88
H3	GND		E33
G6	TIME NAB		P89
H5	GND		E33
G8	PORT 2 PARITY DATA		P117
H7	GND		E51
G10	ENAB PORT		P97
H9	GND		A1 J2 E36
G12			
H11			

CODE IDENT NO.	SIZE		REV
06141	A	32938	F
SCALE —			SHEET 23

A5J38 Data Port 2 Out

PIN NO.	SIGNAL	REMARKS	TO/FROM
A2	DCU SFRATE		A1J7 P66
B1	GND		E12
A4	DCU SFRATE 2		P69
B3	GND		E14
A6	DCU SFINC		P67
B5	GND		E12
A3	DCU SFINC 2		P70
B7	GND		A1J7 E16
A10			
B9			
A12			
B11			
D13			
B13			
C2			
D1			
C4	DCU SFSCH		A1J7 P 68
D3	GND		A1J7 E14
C6			
D5			
C8			
D7			
C10			
D9			
C12	DCU SFSCH 2		A1J7 P71
D11	GND		A1J7 E18

EDC

CODE IDENT NO.	SIZE		REV.
06141	A	32938	G
SCALE -H-			SHEET 29

EMR 3/2/1046

A5J38 Data Port 2 Out

PIN NO.	SIGNAL	REMARKS	TO/FROM
E2			
F1			
E4			
F3			
E6			
F5			
E8			
F7			
E10			
F9			
E12	DCU FRLOCK		A1J5 P81
F11	GND		A1J5 E32
H13			
F13			
G2			
H1			
G4			
H3			
G6			
H5			
G8			
H7			
G10			
H9			
G12			
H11			

CODE IDENT NO.	SIZE		REV.
06141	A	32938	G
SCALE —			SHEET 25

HOLE/COMPONENT CHART

LAST NO USED HOLE	LAST NO USED QTY	DESCRIPTION/UNUSED NUMBER

ARTWORK REVISION INDEX

SHEET NO						
REVISION						

REVISIONS

SYM	DESCRIPTION	EFFECTIVITY	DATE	APPROVED

CONFIG.	BOARD	COMPONENT & CONNECTION 1	2	3	4	5	6	7	8
-69	FIG. 1		C1, 240 pf 304-20-24009 2 ⊣⊢ 13	R1, 180 Ω 616-02-18009 3 ∿ 12	R2, 100 Ω 616-02-10009 4 ∿ 11	R3, 100 Ω 616-02-10009 5 ∿ 10	R4, 100 Ω 616-02-10009 6 ∿ 9	R5, 100 Ω 616-02-10009 7 ∿ 8	
-70	FIG. 1	R1, 2K 616-02-20000 1 ∿ 14		R2, 30K 616-02-30001 3 ∿ 12	CR1. IN4148 088-10-41480 4 ⊳| 11				
-71	FIG. 2		C1, 33pf 304-08-03309 2 ⊣⊢ 13	R1, 100 Ω 616-02-10009 3 ∿ 14	R2, 100 Ω 616-02-10009 4 ∿ 13	R3, 100 Ω 616-02-10009 5 ∿ 12	R5, 180 Ω 616-02-18009 6 ∿ 11	C2, 150pf 304-20-15009 7 ⊣⊢ 10	R4, 100 Ω 616-02-10009 8 ∿ 9
-72	FIG. 2	R1, 330K 616-02-33002 1 ∿ 16							
-73	FIG. 2	R1, 20K 616-02-20001 1 ∿ 16	CR1, IN4148 088-10-41480 2 ⊳| 15	C1, 3.3 μF 301-33-33003 3 ⊣⊢ 14	R2, 20K 616-02-20001 4 ∿ 13	C2, 130 PF 304-20-13009 5 ⊣⊢ 12			
-74	FIG. 2	R1, 20K 616-02-20001 1 ∿ 16	C1, 130 PF 304-20-13009 2 ⊣⊢ 15		R2, 20K 616-02-20001 4 ∿ 13	C2, 130 PF 304-20-13009 5 ⊣⊢ 12		R3 200 Ω 616-02-20009 7 ∿ 10	R4 200 Ω 616-02-20009 8 ∿ 9
-75	FIG. 2	R1, 1K 616-02-10000 1 ∿ 16	C3, ≅ 1000 PF 304-00-00000 2 ⊣⊢ 15		C4, ≅ 1000 pf 304-00-00000 4 ⊣⊢ 13		C1, ≅ 1000 pf 304-00-00000 6 ⊣⊢ 11		C2, ≅ 1000 PF 304-00-00000 8 ⊣⊢ 9
-76	FIG. 2	R1, 1K 616-02-10000 1 ∿ 16	R2, 100 Ω 616-02-10009 2 ∿ 15	R3, 220K 616-02-22002 3 ∿ 14	CR1, IN4148 088-10-41480 4 ⊳| 13		Q1, SU676 263-38-00019 5 → S, 6 → S, D → 11		C1, 1 μF 301-13-10003 8 ⊣⊢ 9
-77	FIG. 1	R1 5.1K 616-02-51000 1 ∿ 14		C1 20PF 304-08-02009 3 ⊣⊢ 12					
-78	FIG. 2	R1, 20K 616-02-20001 1 ∿ 16		C1 130 PF 304-20-13009 8 ⊣⊢ 14		R2 5.1K 616-02-51000 5 ∿ 12		C2 TVAR 5PF 304-00-0000 7 ⊣⊢ 10, 0 → 20PF	C3, 1 μF 301-13-10003 8 ⊣⊢ 9

5

5

5

5

6

CLIP CASE LEAD AT HEADER

Q1 OF 22400-76 (VIEWED FROM LEAD END)

22400

-1	BASIC	CONTROL NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	ITEM OR SYMBOL
CONFIGURATION					
QTY REQUIRED					

PARTS LIST

DASH NO	NEXT ASY NO	USED ON

UNLESS OTHERWISE SPECIFIED
TOLERANCES: DECIMALS, ANGLES, SURFACE FINISH
DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING

APPLICATION
DO NOT APPLY PART NO IDENTIFY PER EMR 13408

MATERIAL

TREATMENT OR FINISH

	DRAWN BY	DATE
	DESIGNER	
	CHECKER	
	DESIGN ENGINEER	
	PROJECT ENGINEER	
	APPROVED	
	APPROVED	

GRADE | CATEGORY | SIMILAR TO

LOCATE APPROX AS SHOWN

EMR
Schlumberger
EMR TELEMETRY
WESTON INSTRUMENTS INC
SARASOTA FLORIDA 33578

SPECIAL NETWORKS
14 & 16 PIN

IDC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	06141	22400	53

SCALE — | SHEET 11 OF

...LE/COMPONENT CHART

LAST NO USED HOLE	QTY	DESCRIPTION/UNUSED NUMBER

ARTWORK REVISION INDEX

SHEET NO							
REVISION							

REVISIONS

SYM	DESCRIPTION	EFFECTIVITY	DATE	APPROVED

CONFIG.	BOARD	COMPONENT & CONNECTION 1	2	3	4	5	6	7	8
-112	FIG 2	R1 47K 616-02-47001 1—16	CR1 IN4148 088-10-41480 2—15	R2 5.1K 616-02-51000 3—14		C1 360PF 304-20-36009 5—12			
-113	FIG 2	C1 47μF 338-13-47004 1—9							
-114	FIG 2	R1 2.2K 616-02-22001 1—16	R2 51K 616-02-51001 2—15	R3 1MEG 616-02-10003 3—14	CR1 IN4148 088-10-41480 4—13	CR2 IN4148 088-10-41480 5—12	CR3 IN4148 088-10-41480 6—11	Q1 2N3947 SEE DETAIL A	263-10-3947
-115	FIG 2		R1 5.1K 616-02-51000 2—15						
-116	FIG 2	R1 20K 616-02-20001 1—16	C3 100PF 304-20-10009 2—15	C1 130PF 304-20-13009 3—14	C4 100PF 304-20-10009 4—13	R2 5.1K 616-02-51000 5—12		C2 TVAR 304-02-00000 SEE 5PF 20PF 7—10	
-117	FIG 2	R1 10K 616-02-10001 1—16	C1 20PF 304-08-02009 2—15	R2 10K 616-02-10001 3—14	C2 36PF 304-08-03609 4—13	R3 5.1K 616-02-51000 5—12	C3 10PF 304-01-01009 6—11	R4 220Ω 616-02-22009 7—10	
-118	FIG2	JUMPER #26 276-99-00010 1—16	JUMPER #26 276-99-00010 2—15	JUMPER #26 276-99-00010 3—14	JUMPER #26 276-99-00010 4—13	JUMPER #26 276-99-00010 5—12	JUMPER #26 276-99-00010 6—11		
-119	FIG2	JUMPER #26 276-99-00010 1—13	JUMPER #26 276-99-00010 2—12	JUMPER #26 276-99-00010 3—11	JUMPER #26 276-99-00010 4—9	JUMPER #26 276-99-00010 5—8	JUMPER #26 276-99-00010 6—7		
-120	FIG2								R1 300PF 304-20-30009 8—9
-121	FIG 1	R1 4.7K 616-02-47000 1—14	R2 160Ω 616-02-16009 2—13	R3 160Ω 616-02-16009 3—12	R4 160Ω 616-02-16009 4—11	R5 160Ω 616-02-16009 5—10	R6 160Ω 616-02-16009 6—9		
-122	FIG 1	R1 10K 616-02-10001 1—14	C1 10PF 304-01-01009 2—13	R2 10K 616-02-10001 3—12	C2 20PF 304-08-02009 4—11				

22400

-1	BASIC	CONTROL NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	ITEM OR SYMBOL
CONFIGURATION				PARTS LIST	
QTY REQUIRED					

DASH NO	NEXT ASSY NO	USED ON

APPLICATION
DO NOT APPLY THIS NO. IDENTIFY PER EMR 13406

GRADE	CATEGORY	SIMILAR TO

UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ANGLES SURFACE FINISH
DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING

MATERIAL

TREATMENT OR FINISH

DRAWN BY DATE
DESIGNER
CHECKER
DESIGN ENGINEER
PROJECT ENGINEER
APPROVED
APPROVED

EMR
Schlumberger

SPECIAL NETWORKS
14 & 16 PIN

EDC

SIZE	CODE IDENT NO	DRAWING NO	REV
C	06141	22400	

SCALE — SHEET 15

APPENDIX A+B

APPENDIX A

List of Mneumonics

SOURCE	MNEMONIC	DESCRIPTION
Simulator ▲	$\overline{\text{BBITS}}$	Beginning bit simulator, 1/4-bit wide pulse occurring at the beginning of each bit period.
	$\overline{\text{ENABDWD}}$	Enable D Word.
	$\overline{\text{ENABHWD}}$	Enable H Word.
	$\overline{\text{XBRMSDO}}$ through $\overline{\text{XBRMSD3}}$	Bit rate stores, most significant digit.
	$\overline{\text{XIDMSB}}$	Controls simulator ID word orientation, -i.e.- MSB/LSB first.
	$\overline{\text{XIDSTRTO}}$ through $\overline{\text{XIDSTRT3}}$	ID start stores. Selects the bit within the simulator D word at which the ID word starts.
	$\overline{\text{XIDUP}}$	ID count up/down control store.
	$\overline{\text{XPRi6}}$	Selects pseudo random generator length of 16 bits.
	BBITS	1/4-bit wide pulse aligned with leading edge of data from simulator.
	BN	Bit wide pulse occurring during last bit of each word.
	BN-1	Bit wide pulse occurring one bit time before last bit of each word.
	BND	Bit wide pulse beginning 1/2-bit time after BN.
	BWO through BW3	Simulator bits/word counter output.
	EOF	End of frame pulse.
	EOFFP	End of frame pulse to front panel.
	EOSF	End of subframe pulse.
▼	EOSFFP	End of subframe pulse to front panel.
Simulator	FRCMP	Frame compare.

SOURCE	MNEMONIC	DESCRIPTION
Simulator ▲	MBITS	1/4-bit wide pulse beginning at mid bit of simulator output.
	POLCTRL	Polarity control of simulator data.
	SERDATA	Serial data.
	SETDISPI through SETDISP8	Set display bus. Drives display from selected stores.
	SIMCLK	Simulator clock input to frame sync.
	SIMNRZL	Simulator data input to frame sync.
	XBRLSD0 through XBRLSD3	Least significant digit of simulator bit rate store.
	XBRMSD0 through XBRMSD3	Most significant digit of simulator bit rate store.
	XBR2SD0 through XBR2SD3	Second most significant digit of simulator bit rate store.
	XBR3SD0 through XBR3SD3	Third most significant digit of simulator bit rate store.
	XCODE0 through XCODE3	Selects simulator output clock.
	XIDINIT0 through XIDINIT7	Initial ID count store.
	XIDLNG0 through XIDLNG3	ID word length store.
▼	XIDMSB	ID MSB first store.
Simulator	XINTCLK	Internal clock store. Selects internal clock for simulator.

SOURCE	MNEMONIC	DESCRIPTION
Simulator	XPR16	Pseudo random generator length store.
	XRIDEOSF	Selects EOSF to reset simulator ID counter.
	XRPREOF	Selects EOF to reset pseudo random generator.
Simulator	XRPREOSF	Selects EOSF to reset pseudo random generator.

SOURCE	MNEMONIC	DESCRIPTION
Front Panel	$\overline{\text{CURSLEFTS}}$	Cursor left set. Sets cursor left flip flop.
	$\overline{\text{CURSRITES}}$	Cursor right set. Sets cursor right flip flop.
	$\overline{\text{ENABCOMP}}$	Enables computer mode.
	$\overline{\text{ENABCR}}$	Enables card reader mode.
	$\overline{\text{ENABPTR}}$	Enable paper tape reader mode.
	$\overline{\text{ERRNGE}}$	Error range. Selects frame sync pattern error rang.
	$\overline{\text{FREEZE}}$	Freezes cursor in present position.
	$\overline{\text{FSSTRAT}}$	Frame sync strategy. Sets adapt/ non adapt mode.
	$\overline{\text{LOCENTER}}$	Local enter. Loads 711 stores in local mode.
	$\overline{\text{SELMF}}$	Select main frame made.
	$\overline{\text{SELSF}}$	Select subframe mode.
	$\overline{\text{SELWD1}}$	Select word mode.
	$\overline{\text{SELOFF}}$	Select printer off.
	$\overline{\text{SETUPMOM}}$	Selects program mode.
	$\overline{\text{SFIRST}}$	Resets subframe 1 to search mode.
	$\overline{\text{SFIR2SEL}}$	Selects SF1 or SF2 to control display and printer SF mode.
	$\overline{\text{SF2RST}}$	Resets subframe 2 to search mode.
	$\overline{\text{SIMRST}}$	Resets simulator to initial condition.
	$\overline{\text{STARTPTR}}$	Places paper tape reader in run mode.
Front Panel	$\overline{\text{STEP}}$	Increments function address in program mode.

SOURCE	MNEMONIC	DESCRIPTION
Front Panel	$\overline{\text{FSRST}}$	Resets frame sync to search mode.
	$\overline{\text{WDIMOM}}$	Selects word display mode.
	BCD/OCT	Selects BCD or octal data to printer.
	BITSYNC	Selects bit sync input to frame sync.
	BLANK	Keyboard switch output.
	CURSORL	Cursor left. Sets cursor left flip flop.
	CURSORR	Cursor right. Sets cursor right flip flop.
	DISPBIN	Display binary. Selects binary data for display.
	ENABCOMP	Enables computer mode.
	ERRNGE	Selects display error range.
	EXTIN1	Selects external 1 input to frame sync.
	EXTIN2	Selects external 2 input to frame sync.
	FSRST	Frame sync reset to search mode.
	FSSTRAT	Frame sync strategy.
	KEY 0 to KEY 9	Keyboard switches output.
	LOCENTER	Local entry. Loads 711 stores in local mode.
	LOCALMODE	Selects local program/display mode.
	READSTORES	Places memory stores in static mode for display purposes.
Front Panel	SELMF	Select main frame mode.

SOURCE	MNEMONIC	DESCRIPTION
Front Panel	SELSF	Select subframe mode.
	SFIRST	Subframe 1 reset to search mode.
	SF1R2SEL	Selects SF1 or SF2 to control display and printer SF mode.
	SF2RST	Subframe 2 reset to search mode.
	SIMINPUT	Selects simulator input to frame sync.
	SIMRST	Resets simulator.
	STEP	Increments function address in local program mode.
Front Panel	STEPMODE	Selects step mode.

SOURCE	MNEMONIC	DESCRIPTION
Word Select and Display	$\overline{\text{EXTSTRTFR}}$	External start frame.
↑	$\overline{\text{LDWSDERCTR}}$	Load word select/display frame counter.
	$\overline{\text{LDWSDWCTR}}$	Load word select/display word counter.
	$\overline{\text{XSTARTFR}}$	Start frame store. Selects frame rate for external start to computer.
	$\overline{\text{XTHRU}}$	Selects throughput mode for frame sync.
	BCDH1, 2, 4, 8	Hundreds digit, BCD data.
	BCDTH1, 2, 4, 8	Thousands digit, BCD data.
	BCDTTH1, 2, 4, 8	Ten thousands digit, BCD data.
	BCDT1, 2, 4, 8	Tens digit, BCD data.
	BCDU2, 4, 8	Units digit, BCD data.
	CLKWSDFRCTR	Clock word select/display frame counter.
	CLKWSDWCTR	Clock word select/display word counter.
	DACSTRB	DAC strobe. Loads. DAC store.
	DAC 1 through DAC 12	Data bits controlling DAC output.
	DATRUE	Data true. Indicates data on output lines and stable each word time.
	EXTSTRTSFR	External start subframe.
	FRATEFP	Frame rate pulse to front panel.
Word Select and Display	LSB1 through LSB16	LSB aligned data output.

SOURCE	MNEMONIC	DESCRIPTION
Word Select and Display	STRBDISPFP	Strobe display pulse to front panel.
	WD1DATRUE	Selected word data on line and stable.
	XFRSTFR0 through XFRSTFR2	First frame number store.
	XFRSTWD0 through XFRSTWD2	First word number store.
	XSF1STRT	Selects SF1 to generate external start to computer.
	XSF2STRT	Selects SF2 to generate external start to computer.
Word Select and Display	XSTARTFR	Selects FRATE to generate external start to computer.

SOURCE	MNEMONIC	DESCRIPTION
Subframe Synchronizer	$\overline{\text{FRNFFX}}$	Frame N. Pulse from selected subframe.
	$\overline{\text{LDFRCTRX}}$	Load frame counter. Pulse frame selected subframe.
	$\overline{\text{SFSRCHX}}$	Subframe search status line from selected subframe.
	$\overline{\text{SF1CHKLD}}$	Subframe 1 check lamp drive.
	$\overline{\text{SF1LCKLD}}$	Subframe 1 lock lamp drive.
	$\overline{\text{SF1SRCHLD}}$	Subframe 1 search lamp drive.
	$\overline{\text{SF1VFYLD}}$	Subframe 1 verify lamp drive.
	$\overline{\text{SF2CHKLD}}$	Subframe 2 check lamp drive.
	$\overline{\text{SF2LCKLD}}$	Subframe 2 lock lamp drive.
	$\overline{\text{SF2SRCHLD}}$	Subframe 2 search lamp drive.
	$\overline{\text{SF2VFYLD}}$	Subframe 2 verify lamp drive.
	FRNFFX	Frame N. Pulse from selected subframe.
	IDONX	Selected subframe in ID mode.
	SFLOCKX	Subframe lock status from selected subframe.
	SFRATEFP	Subframe 1 rate pulse to front panel.
	SFRATEFP2	Subframe 2 rate pulse to front panel.
	SFSELLD	Controls subframe indication to printer column 6.
	SFSRCHX	Selected subframe search status.
Subframe Synchronizer	SFONX	Selected subframe on.

SOURCE	MNEMONIC	DESCRIPTION
Data Entry	$\overline{\text{SELSETUP}}$	Select setup. Places memory stores in static mode to allow display of contents.
	$\overline{\text{SETSTRB}}$	Set strobe. Loads 711 stores from setup bus.
Data Entry	$\overline{\text{SET 1}}$ through $\overline{\text{SET 16}}$	Setup bus which loads 711 stores
DAC	ANALOGOUT	Analog equivalent of word selected for display.
Bit Synchronizer	BSCLK	Bit sync clock input to frame sync.
	BSNRZL	Bit sync data stream into frame sync.

SOURCE	MNEMONIC	DESCRIPTION
Frame Synchronizer ▲	KEY 0 through KEY 9 BLANK	Keyboard switch outputs.
	$\overline{\text{SETUPMOM}}$	Setup momentary.
	$\overline{\text{WD1MOM}}$	Word momentary
	CMRSTSTRB1	Computer reset strobe to internal simulator.
	LOCAL MODE	Local mode.
	STEP MODE	Step mode.
	LOCENTER	LOCAL ENTER.
	$\overline{\text{CURSRITE}}$	Cursor right.
	$\overline{\text{CURSLEFT}}$	Cursor left.
	$\overline{\text{XTHRU}}$	Select throughput mode.
	FSRST	Frame sync reset.
	ERRNGE	Error range.
	EXTIN1	Selects external input one.
	EXTIN2	Selects external input two.
	BITSYNC	Selects bit sync input.
	CN+2	Bit wide pulse occurring two bits after CN pulse.
	EXTNRZL1	Serial data stream from external one input.
	EXTCLK1	0° clock from external one input.
	EXTNRZL2	Serial data stream from external two input.
	EXTCLK2	0° from external two input.
▼	BSNRZL	Serial data stream from internal bit sync.
Frame Synchronizer	BSCLK	0° clock from internal bit sync.

SOURCE	MNEMONIC	DESCRIPTION
Frame Synchronizer	SIMNRZL	Serial data stream from internal simulator.
	0° CLKFS	0° clock from internal simulator
	SIMINPUT	Selects internal simulator input.
	$\overline{\text{CN + 4}}$	Bit wide pulse four bits after CN pulse.
	SETUP 1 through SETUP 16	Sixteen bit setup bus to rear panel to load external module stores.
	SETUP STRB	Strobe which enters setup bus content into external module stores.
	CMRSTSTRB	Computer reset strobe. Used to reset frame sync and/or simulator from computer interface.
	$\overline{\text{FSSRCHLD}}$	Frame sync search lamp drive.
	FVFYLD	Frame sync verify lamp drive.
	FLCKLD	Frame sync lock lamp drive.
	FCHKLD	Frame sync check lamp drive.
	N430 through N433, N435, N436	Drive status word bits 1-4 representing number of errors in frame sync pattern.
	FRSEARCH	Frame search. Status signal.
	FRVERIFY	Frame verify. Status signal
	FRLOCK	Frame lock. Status signal.
	FRCHECK	Frame check. Status signal.
	$\overline{\text{SLIP}}$	Indicates CP and CN not aligned.
	FSSTRAT	Frame sync strategy. Sets adaptive, non-adaptive mode.
Frame Synchronizer	ADAPT	Indicates frame sync is in adaptive mode.

SOURCE	MNEMONIC	DESCRIPTION
Frame Synchronizer	DATAINFS	Clock input frame sync. Selected clock input to front panel test point.
	LOCDATA1 through LOCDATA8	Local data. Next data to be entered into 711 stores from keyboard.
	CURSOR1 through CURSOR8	Cursor. Enable local data stores 1 through 8 and drive next data display cursor.
	SETDISP1 through SETDISP8	Set display bus. Drives present data display, use to examine 711 store content.
	LOCMOD0 through LOCMOD2	Three-bit local module address. Setup from keyboard, drives module address display.
	$\overline{\text{CURS1}}$	Cursor 1. Enables local module address stores and drives module display cursor.
	LOCGPT0, LOCGPT1	Local group tens. Two bit tens position junction address. Set up from keyboard, drives function tens display.
	$\overline{\text{CURS2}}$	Cursor 2. Enables function address tens position store and drives function address tens position display cursor.
	LOCGPU0 through LOCGPU3	Local group units. Four-bit units position function address. Set up from keyboard, drives function address units display.
	$\overline{\text{CURS3}}$	Cursor 3. Enables function address units position store.
	$\overline{\text{MBIT}}$	Mid bit. Forty nanosecond pulse occurring at mid-bit time.
Frame Synchronizer	$\overline{\text{BBIT}}$	Beginning bit. Forty namosecond pulse occurring at beginning of each bit time.

SOURCE	MNEMONIC	DESCRIPTION
Frame Synchronizer	$\overline{\text{PWRONRST}}$	Power on reset.
↑	$\overline{\text{FCCP}}$	Frame code complement pulse.
	FSRCH	Frame sync in search mode.
	$\overline{\text{CN-2}}$	Bit wide pulse occurring two bits before CN.
	CN + 1	Bit wide pulse occurring one bit after CN.
	$\overline{\text{CPWIN}}$	NAND condition of correlation pulse and window.
	CN+2DLY	CN+2 delay. Bit wide pulse occurring 2-1/2 bits after CN.
	FVFY	Frame sync in verify mode.
	FCHK	Frame sync in check mode.
	$\overline{\text{SET1}}$ through $\overline{\text{SET16}}$	Setup bus which loads all 711 stores
	SEGD	Segment D. Drives error range 100 multiplier indicator.
	SEGG	Segment G. Drives error range 10 multiplier indicator.
	SEGA	Segment A. Drives error range 1 multiplier indicator.
	ERRDUNITS A through G	Error display units segments, drive seven segment error display units.
	ERRDTENSEG A through G	Error display tens segments, drive seven segment error display tens.
	MSRG	Main shift register stage 6. Delayed version of serial input data to frame sync.
↓		
Frame Synchronizer	FLCK	Frame sync in lock mode.

SOURCE	MNEMONIC	DESCRIPTION
Frame Synchronizer	$\overline{\text{CDRWIN}}$	NAND condition of correlation and window.
	KEYMSB	Most significant bit of BCD conversion of number selected on keyboard.
	KEYDATA2, 3	Second and third bits of BCD conversion of number selected on keyboard.
	KEYLSB	Least significant bit of BCD conversion of number selected on keyboard.
	KEYSTRB	Keystrobe. Occurs each time keyboard button is pressed.
	CN+3	Bit wide pulse occurring three bits after CN.
Frame Synchronizer	RDY	Ready. AND condition of 711 power on and computer selcted.

APPENDIX B

Sample Worksheets

PROGRAMMER:_____ DATE:_____

FORMAT WORKSHEET

PROGRAM:_____
BIT RATE:_____
BIT RATE MULT:_____
OUTPUT CODE:_____
WORD SIZE:_____

DATA ALIGN:_____
DATA WDS/FR:_____
SUBCOM WDS/FR:_____

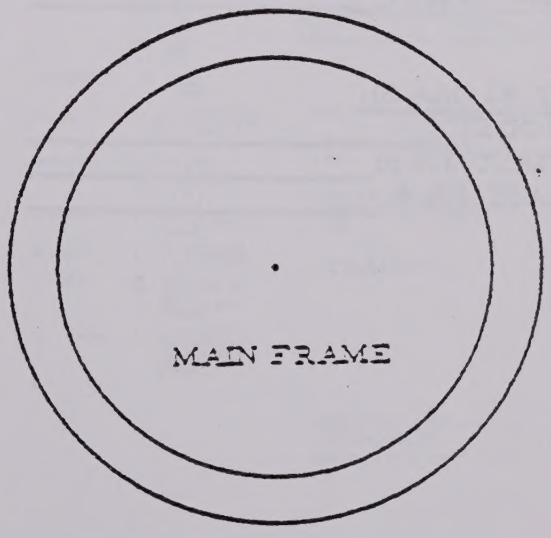
SIMULATOR (MA 4 & 5):

FUNCTION	SIM WD	WORD WD	LOCATION FR	BINARY DATA 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	FBT 1
	A																		
	B																		
	C																		
	D																		
	E																		
	F																		
	G																		
	H																		

MAIN FRAME (MA 1):
FIRST WD #:_____
BITS/FR:_____
ALT/WD:_____

SF #1 (MA 2):
MODE:_____
FIRST FR #:_____
LAST FR #:_____

SF #2 (MA 3):
MODE:_____
FIRST FR #:_____
LAST FR #:_____



PROGRAMMER:_____ DATE:_____

FORMAT WORKSHEET

PROGRAM:_____
BIT RATE:_____
BIT RATE MULT:_____
OUTPUT CODE:_____
WORD SIZE:_____

DATA ALIGN:_____
DATA WDS/FR:_____
SUBCOM WDS/FR:_____

SIMULATOR (MA 4 & 5):

FUNCTION	SLM WD	WORD WD	LOCATION FR	BINARY DATA 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	FBT 1
	A																		
	B																		
	C																		
	D																		
	E																		
	F																		
	G																		
	H																		

MAIN FRAME (MA 1):
FIRST WD #:_____
BITS/FR:_____
ALT/WD:_____

SF #1 (MA 2):
MODE:_____
FIRST FR #:_____
LAST FR #:_____

SF #2 (MA 3):
MODE:_____
FIRST FR #:_____
LAST FR #:_____

Format Worksheet

(Module Address Assigned on a System Basis)

BASIC UNIT

FRAME SYNCHRONIZER (MODULE ADDRESS 1)

MA	DA

	8	7	6	5	4	3	2	1
0	PATN 4		PATN 3		PATN 2		PATN 1(LSB)	
1	8		7		6		5	
2	12		11		10		9	
3	16		15		14		13	
4	20		19		18		17	
5	24		23		22		21	
6	28		27		26		25	
7	32		31		30		29	
8	2^5	PATN LENGTH		2^0	PATN 33			
9	PATN TYPE		WINDOW		ADAPT	ASM	INPUT	
10	2^3	VFY ERRS	2^0	2^3	VFY PATNS		2^0	
11	2^3	CHK ERRS	2^0	2^3	CHK PATNS		2^0	
12	2^{15}	BITS PER FRAME					2^8	
13	2^7	(BINARY)					2^0	
14								
15								
16	LSBF	OUTPUT	2^4	WD LENGTH			2^0	
17	LSBO	ALT MODE	2^4	ALT WD LENGTH			2^0	
18	MSD	ALT WD LOCATION						
19	(BCD)	LSD						
20	MSD	DATA WORDS PER						
21	FRAME (BCD)	LSD						
22	2^2	1ST WD NR	2^0	2^2	1ST FR NR	2^0	EXTSTRT	
23	THRU	VWL ON	POD DEL		PARITY ON	ODD	FBT	STRP
24								
25								
26								
27								
28								
29								
30								
31	VFY	LO VFY	SIM PRST	FS RST	VWL CLR			

PATN(N) 0X - DON'T CARE
10 - 0
11 - 1

PATN TYPE: 00 - NORMAL
01 - FAC
10 - FCC
11 - AUTO POL CONTROL

WINDOW: 00 - 1 BIT
01 - 3 BITS
10 - 5 BITS
11 - ILLEGAL

ADAPT: 0 - OFF
1 - ON

ASM (AUX SRCH MODE): 0-BEST PATTERN IN SRCH
1-PROGRAMMABLE ERRORS (VFY)

LSBF: 0 - INPUT MSB FIRST
1 - INPUT LSB FIRST

LSBO: 0 - OUTPUT MSB ALIGNED
1 - OUTPUT LSB ALIGNED

OUTPUT 00 - DATA ONLY
01 - FS PATN
10 - STATUS

ALT MODE: 00 - NO ALT LNGTH
01 - ONE ALT LNGTH
10 - REPEATING ALT LNGTH WORDS. IN THIS MODE, INSTR NR 18 INDICATES HOW OFTEN THE ALT LNGTH REPEATS, AND INSTR NR 19 INDICATES WHERE THE ALT LNGTH STARTS. BOTH IN BCD.

EXT STRT: 00 - FR RATE EXTERNAL START
01 - SFI RATE EXTERNAL START
10 - SFI RATE EXTERNAL START
11 - NO EXTERNAL START

THRU: 1-THRUPUT MODE ON (SER-TO-PAR CONVERSION WITHOUT SYNC)

VWL ON: 1-VWL OPTION ENABLED

POD DEL: POD DELETE. USED WITH POD (MA 0, DA 2) AS FOLLOWS:

POD	POD DEL	PORT 2 PARALLEL DATA OUTPUT
0	0	WORD DELETED
0	1	WORD OUTPUT
1	0	WORD OUTPUT
1	1	WORD DELETED

PARITY ON: 1-PARITY ON, CHECK FOR ERRORS
0-PARITY OFF, GENERATE PARITY BIT

PARITY ODD 1-ODD PARITY
0-EVEN PARITY

PARITY FBT: 1-PARITY TRANSMITTED FIRST
0-PARITY TRANSMITTED LAST

PARITY STRP: 1-STRIP PARITY BIT FROM THE PARALLEL DATA OUTPUT
0-OUTPUT PARITY BIT WITH DATA WORD

SUBFRAME SYNCHRONIZER (162) (MODULE ADDRESS 2&3)

MA	DA

	8	7	6	5	4	3	2	1
0	MODE							
1						2^2	1ST FR NR.	2^0
2	MSD	FINAL FR						
3	NUMBER (BCD)	LSD						
4	8	7	URC	PATN		3	2	1 (FBT)
5	16	15	URC	PATN		11	10	9
6	24	23	URC	PATN		19	18	17
7	32	31	URC	PATN		27	26	25
8	2^3	VFY PATNS	2^0	2^3	CHK PATNS		2^0	
9	2^3	VFY ERRS	2^0	2^3	CHK ERRS		2^0	
10								
11								
12								
13								
14								
15								
16	2^{15}	1ST SEGMENT						2^8
17	2^7	LOC - BIT (BIN)						2^0
18	2^{15}	2ND SEGMENT						2^8
19	2^7	LOC						2^0
20	2^{15}	3RD SEGMENT						2^8
21	2^7	LOC						2^0
22	2^{15}	4TH SEGMENT						2^8
23	2^7	LOC						2^0
24						2^3	1ST SEGM LENGTH	2^0
25						2^3	2ND SEGM LENGTH	2^0
26						2^3	3RD SEGM LENGTH	2^0
27						2^3	4TH SEGM LENGTH	2^0
28								
29								
30								
31								

MODE: 00 - OFF
01 - SFID
10 - URC
11 - FCC

IN IO MODE, INSTRS 5,6,7,9,18-23 AND 25-27 DO NOT APPLY. THE FOLLOWING INSTRS ARE REDEFINED.

	8	7	6	5	4	3	2	1
1	ICNT 2^8			COUNT UP	MSB FIRST	2^2	1ST FR COUNT	2^0
4	2^7	2^6	INITIAL IO COUNT				2^1	2^0
16	2^{15}	2^{14}	1ST IO PATN BIT				2^9	2^8
17	2^7	2^6	LOCATION (BIN)				2^1	2^0
24						2^3	IO PATN LENGTH	2^0

* VFY: 0 - NORMAL (NO VERIFY)
1 - VERIFY SETUP STORES ON DATA OUTPUT BUS

* LO VFY: 0 - NORMAL
1 - STORES LOADED AND VERIFIED ON DATA BUS

*SIM PRST 0 - NO ACTION
1 - RESET SIM

*FS RST 0 - NO ACTION
1 - RESET FS

VWL CLR 1-CAUSES VWL RAM TO BE CLEARED (REQ'D PRIOR TO VWL SETUP). GENERATES PULSE ONLY-CANNOT BE EXAMINED.

**INPUT 00 - EXT 1
01 - EXT 2
10 - EXT 3
11 - INT SIM

*THESE BITS CANNOT BE EXAMINED VIA FRONT PANEL OR VIA COMPUTER AND CAN BE LOADED ONLY BY THE COMPUTER.

**WHEN PROGRAMMING SETUP ENABLE CONTROL IN THE LOCAL OR STEP POSITIONS, INPUT SELECTION IS CONTROLLED DIRECTLY FROM THE FRONT PANEL INPUT SOURCE SWITCHES.

SIMULATOR (MODULE ADDRESS 4)

MA	DA

	8	7	6	5	4	3	2	1
0	ON	INT CLK				2^2	SR MULTIP	2^0
1	MSD	BIT RATE						
2	(BCD)	LSD						
3	OUTPUT CODE				2^3	COMMON LENGTH		2^0
4	COMMON WORD	COMPL ALL			2^3	A WORD LENGTH		2^0
5	SUBCOM WORDS				2^3	C WORD LENGTH		2^0
6	2^3	1ST IO BIT LOC	2^0	2^3	IO WORD LENGTH			2^0
7	2^7	2^6	INITIAL IO COUNT				2^1	2^0
8	IO UP	IO MSB	IORST EOSF	ICNT	2^8	PR LNGTH	PR	RST
9	MSD	WORDS PER FRAME						
10	(BCD)	LSD						
11	MSD	FRAMES PER SUBFRAME						1
12	(BCD)	LSD						
13	A	B	C	D	E	F	G	H
14								
15								
16	MSD	A LOCATION						
17	(WORD) (BCD)	LSD						
18	MSD	B LOCATION						
19	(WORD)	LSD						
20	MSD	C LOCATION						
21	(WORD)	LSD						
22	MSD	C LOCATION						
23	(FRAME)	LSD						
24	MSD	D LOCATION						
25	(WORD)	LSD						
26	MSD	D LOCATION						
27	(FRAME)	LSD						
28	MSD	E LOCATION						
29	(WORD)	LSD						
30	MSD	E LOCATION						
31	(FRAME)	LSD						

SR MULTIP: 000 - $x10^0$
001 - $x10^1$
010 - $x10^2$
011 - $x10^3$
100 - $x10^4$
101 - $x10^5$
110 - $x10^6$

BIT RATE: X.XXX

OUTPUT CODE: 0000 - NRZL
0001 - NRZM
0010 - NRZS
0011 - RZ
0100 - BI0L
0101 - BI0M
0110 - BI0S
0111 - DMM
1000 - DMS

COMMON WORD: 00 - F WORD
01 - G WORD
10 - H WORD

COMPL ALL: 1 - ALL WORDS COMPLEMENT EVERY N FRAMES FOR N FRAMES DURATION

SUBCOM WORDS: 0000 - NO SUBCOM
1XXX - C WD S/C
X1XX - D WD S/C
XX1X - E WD S/C
XXX1 - F WD S/C

IO RST EOSF: 0 - NO RST ON IO
1 - RST IO AT END OF SUBFRAME

PR LENGTH: 0 - 11 BIT GENERATOR
1 - 16 BIT GENERATOR

PR PRESET 00 - NO PRST
01 - PRST AT END OF FRAME
10 - PRST AT END OF SUBFRAME

COMPL DATA WDS: 0 - NO COMPLEMENT
1 - COMPLEMENT RESPECTIVE DATA WORDS ONE FRAME EVERY N FRAMES

SIMULATOR (MODULE ADDRESS 5)

MA	DA

	8	7	6	5	4	3	2	1
0	MSD	F LOCATION						
1	(WORD)	LSD						
2	MSD	F LOCATION						
3	(FRAME)	LSD						
4	MSD	G LOCATION						
5	(WORD)	LSD						
6	MSD	H LOCATION						
7	(WORD)	LSD						
8	FBT	2	A WORD			6	7	8
9	9	10	DATA			14	15	16
10	FBT	2	B WORD			6	7	8
11	9	10	DATA			14	15	16
12	FBT	2	C WORD			6	7	8
13	9	10	DATA			14	15	16
14	FBT	2	D WORD			6	7	8
15	9	10	DATA			14	15	16
16	FBT	2	E WORD			6	7	8
17	9	10	DATA			14	15	16
18	FBT	2	F WORD			6	7	8
19	9	10	DATA			14	15	16
20								
21								
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								

VARIABLE WORD LENGTH (MODULE ADDRESS 0)

	8	7	6	5	4	3	2	1
0	(THOU) 2^3	2^2	2^1	VWL LOCATION 2^0	2^3	2^2	(HUND) 2^1	2^0
1	(TENS) 2^3	2^2	2^1	VWL LOCATION 2^0	2^3	2^2	(UNITS) 2^1	2^0
2	POD			VW LENGTH 2^4	2^3	2^2	2^1	2^0

*VWL LOCATION - BCD LOCATION OF VWL POSITION TO BE LOADED

VW LENGTH - BINARY VALUE OF VWL

POD - (SEE POD DEL BIT IN MA1, DA2)

(NOTE: WHEN USING CARD READER, INSTRUCTIONS 0-2 MAY BE REPEATED UP TO 10 TIMES ON ONE PROGRAMMING CARD)

*CANNOT BE DISPLAYED OR COMPUTER VERIFIED.

MA=MODULE ADDRESS (3 BITS), E.G., FR SYNC = 001, SF SYNC NO. 1 = 010, SIMULATOR = 100, ETC.

DA=DEVICE (OR GROUP) ADDRESS (5 BITS)